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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gadfb-x0

Table 1-1. List of Ordering Part Numbers

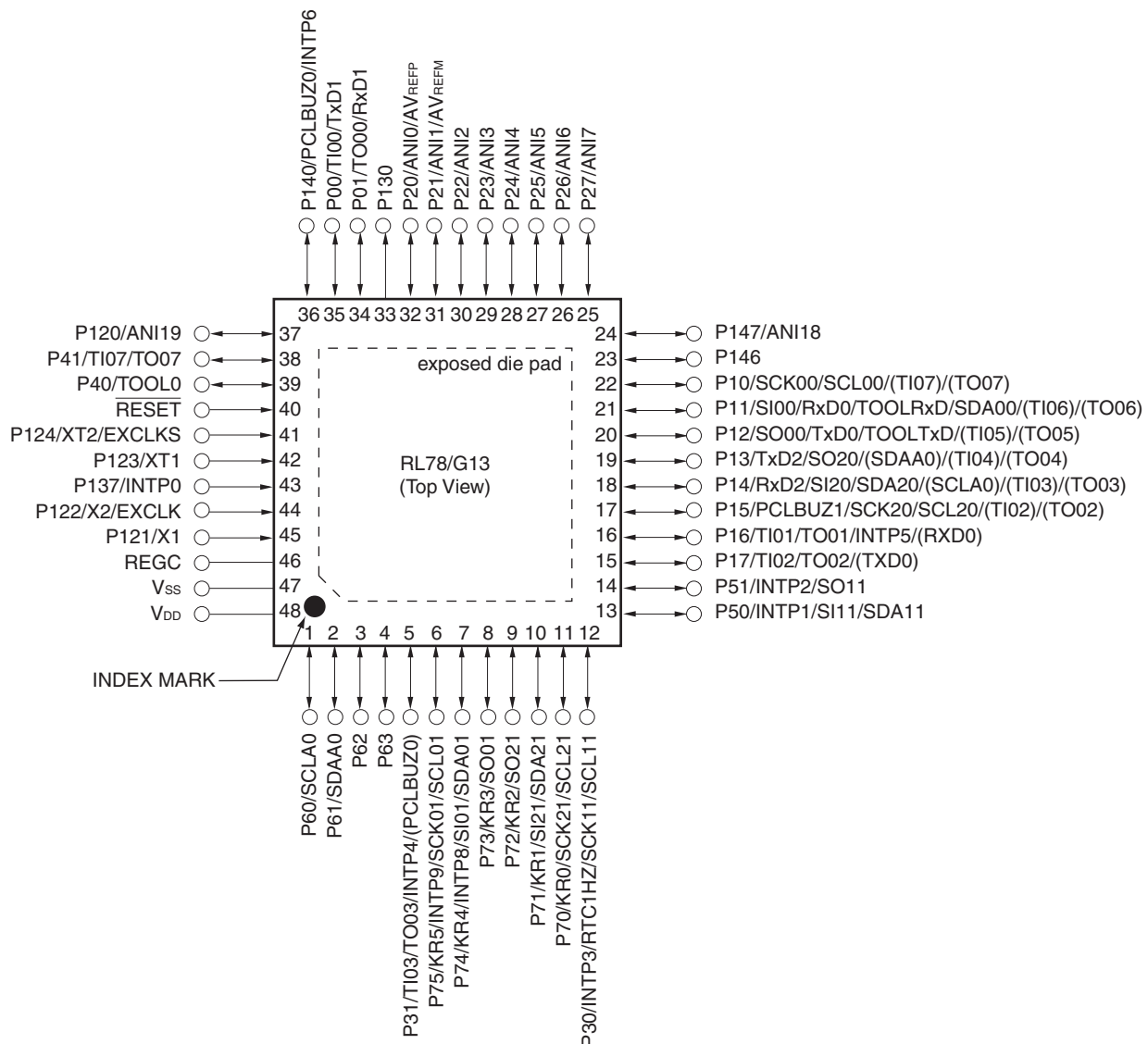
(7/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A D G	R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAF#V0, R5F100JLAF#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAF#X0, R5F100JLAF#X0 R5F100JCDAFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDAFA#V0, R5F100JGDFA#V0, R5F100JHDAFA#V0, R5F100JJDFA#V0, R5F100JKDAFA#V0, R5F100JLDAFA#V0 R5F100JCDAFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDAFA#X0, R5F100JGDFA#X0, R5F100JHDAFA#X0, R5F100JJDFA#X0, R5F100JKDAFA#X0, R5F100JLDAFA#X0 R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0, R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0, R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0
		Not mounted	A D	R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAF#V0, R5F101JLAF#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAF#X0, R5F101JLAF#X0 R5F101JCDAFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDAFA#V0, R5F101JGDFA#V0, R5F101JHDAFA#V0, R5F101JJDFA#V0, R5F101JKDAFA#V0, R5F101JLDAFA#V0 R5F101JCDAFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDAFA#X0, R5F101JGDFA#X0, R5F101JHDAFA#X0, R5F101JJDFA#X0, R5F101JKDAFA#X0, R5F101JLDAFA#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



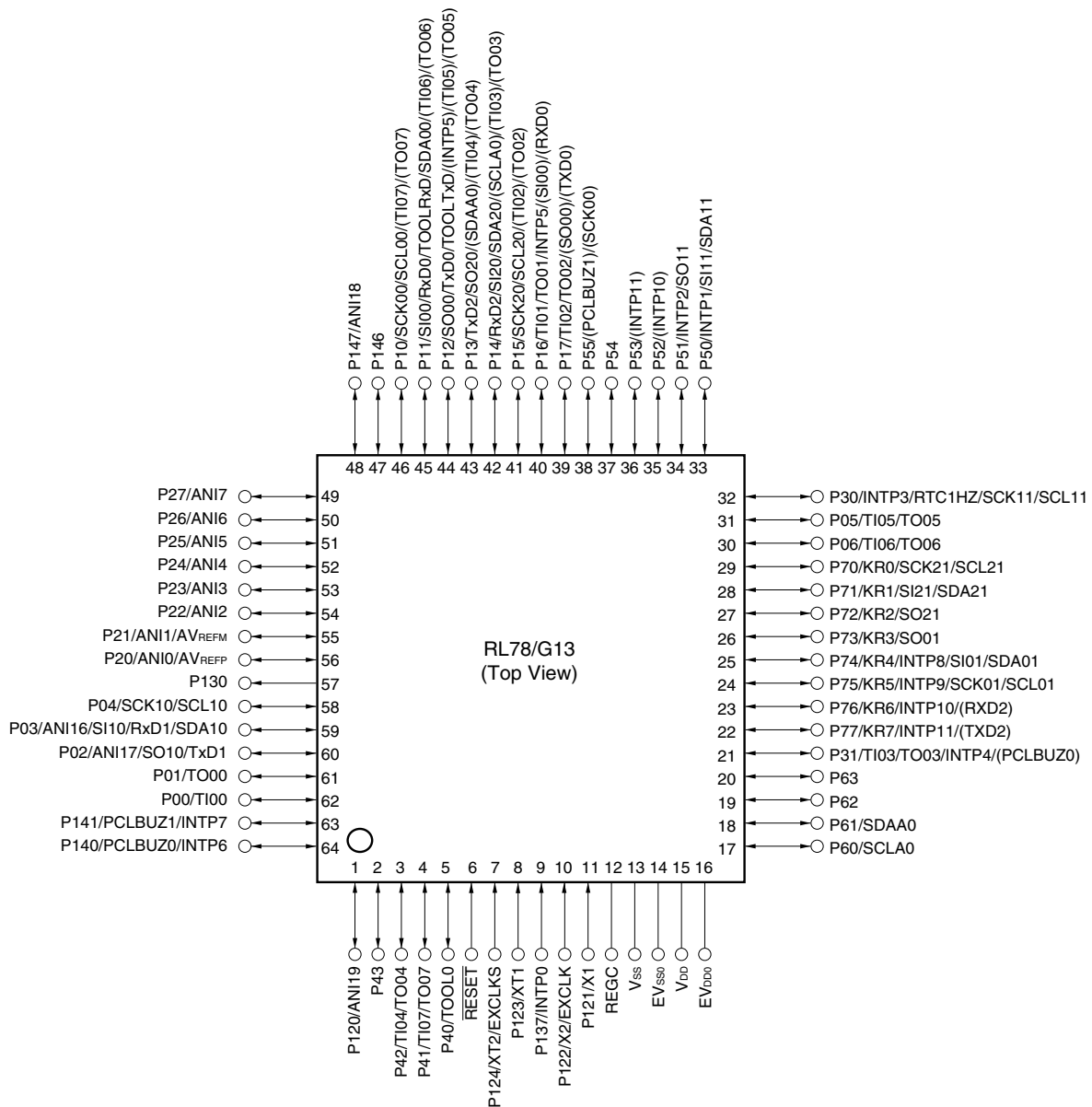
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to Vss.

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

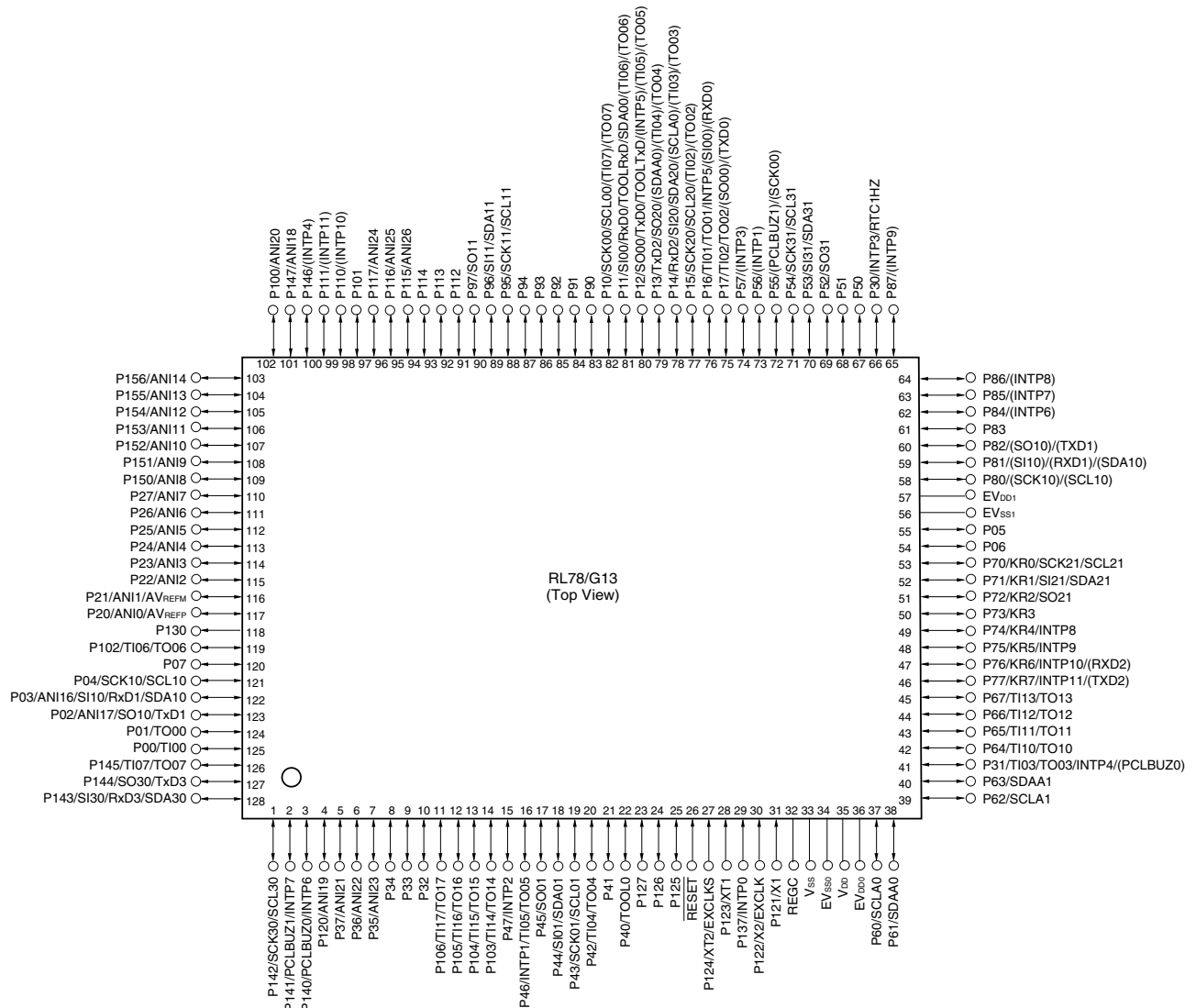


- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.14 128-pin products

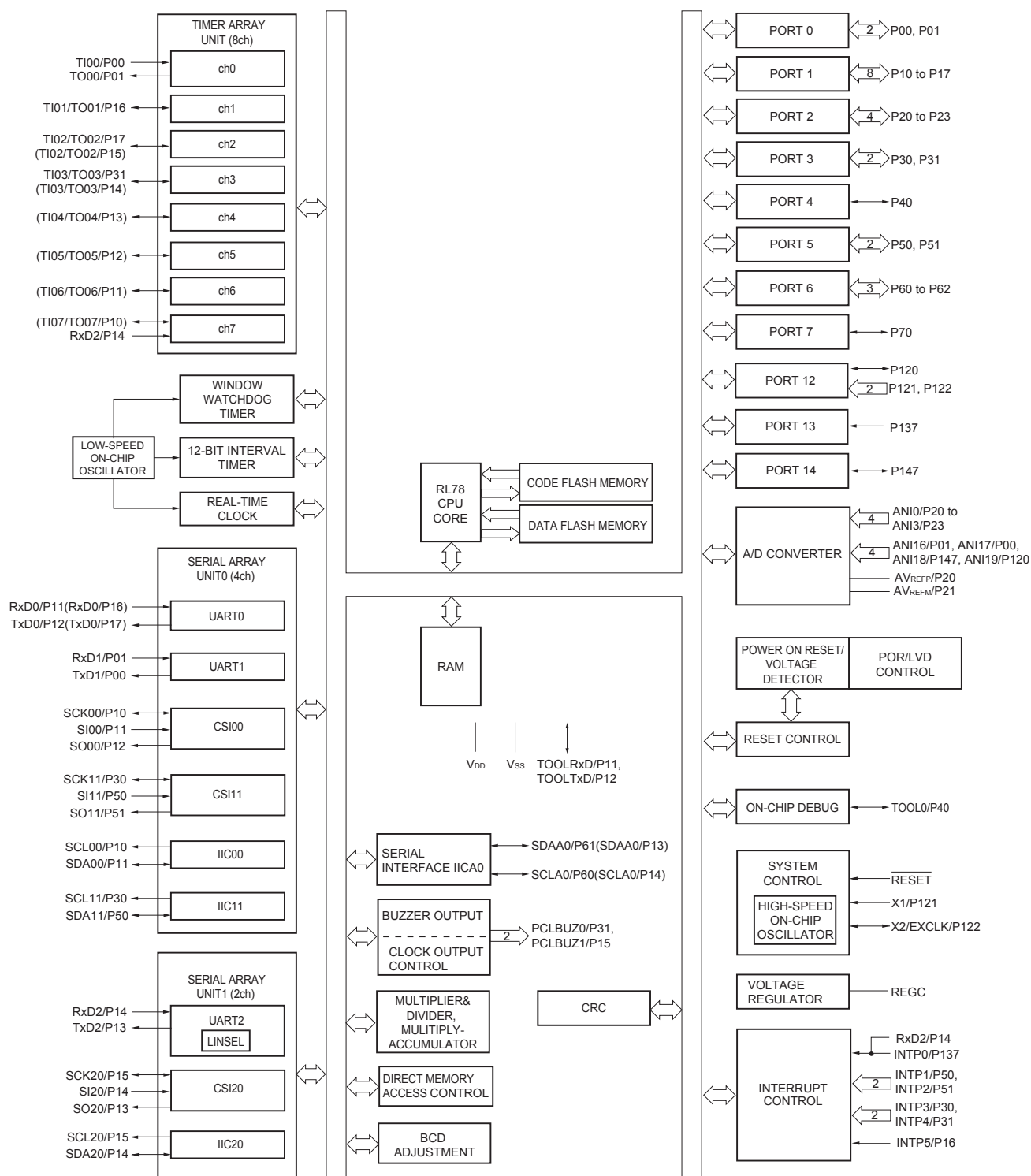
- 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.5 32-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products**(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V) (1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current ^{Note 1}	I _{DD1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V		2.6	mA
						V _{DD} = 3.0 V		2.6	mA
					Normal operation	V _{DD} = 5.0 V		6.1	mA
						V _{DD} = 3.0 V		6.1	mA
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		4.8	mA
						V _{DD} = 3.0 V		4.8	mA
				f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.5	mA
						V _{DD} = 3.0 V		3.5	mA
			LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.5	mA
						V _{DD} = 2.0 V		1.5	mA
			LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.5	mA
						V _{DD} = 2.0 V		1.5	mA
			HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		3.9	mA
						Resonator connection		4.1	mA
				f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		3.9	mA
						Resonator connection		4.1	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		2.5	mA
						Resonator connection		2.5	mA
				f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		2.5	mA
						Resonator connection		2.5	mA
			LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	mA
						Resonator connection		1.4	mA
				f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.4	mA
						Resonator connection		1.4	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C	Normal operation	Square wave input		5.4	μA
						Resonator connection		5.5	μA
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C	Normal operation	Square wave input		5.5	μA
						Resonator connection		5.6	μA
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C	Normal operation	Square wave input		5.6	μA
						Resonator connection		5.7	μA
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C	Normal operation	Square wave input		5.9	μA
						Resonator connection		6.0	μA
				f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C	Normal operation	Square wave input		6.6	μA
						Resonator connection		6.7	μA

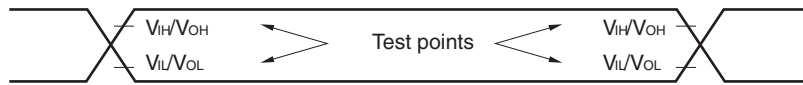
(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate ^{Note 1}		2.4 V ≤ E _{VDD0} ≤ 5.5 V		f _{MCK} /6 ^{Note 2}		f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		5.3		1.3		0.6	Mbps
		1.8 V ≤ E _{VDD0} ≤ 5.5 V		f _{MCK} /6 ^{Note 2}		f _{MCK} /6		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		5.3		1.3		0.6	Mbps
		1.7 V ≤ E _{VDD0} ≤ 5.5 V		f _{MCK} /6 ^{Note 2}		f _{MCK} /6 ^{Note 2}		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}		5.3		1.3		0.6	Mbps
		1.6 V ≤ E _{VDD0} ≤ 5.5 V	—			f _{MCK} /6 ^{Note 2}		f _{MCK} /6	bps
		Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} ^{Note 3}	—			1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when E_{VDD0} < V_{DD}.

2.4 V ≤ E_{VDD0} < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ E_{VDD0} < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ E_{VDD0} < 1.8 V : MAX. 0.6 Mbps

3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V_{DD} ≤ 5.5 V)

16 MHz (2.4 V ≤ V_{DD} ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V_{DD} ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V_{DD} ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(5) During communication at same potential (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

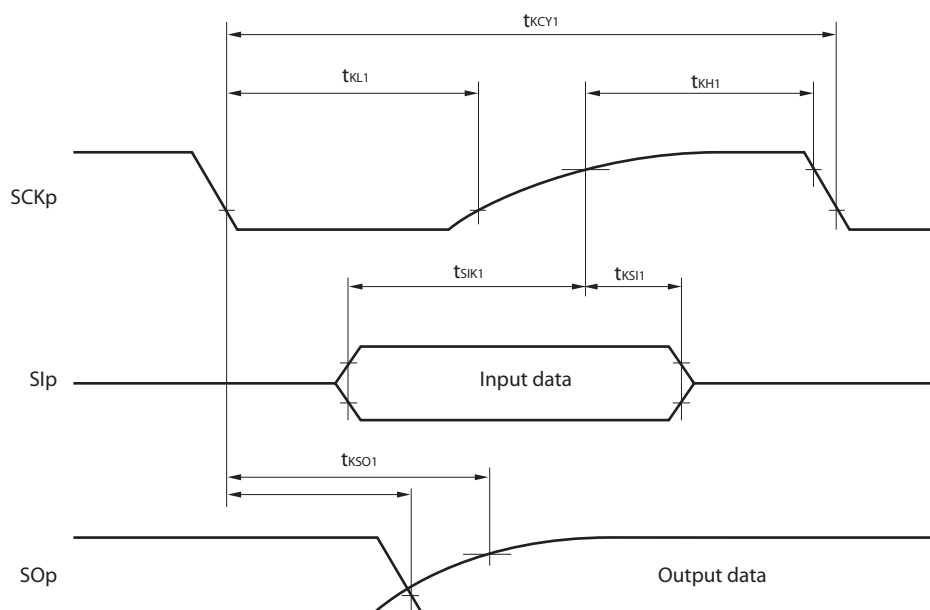
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

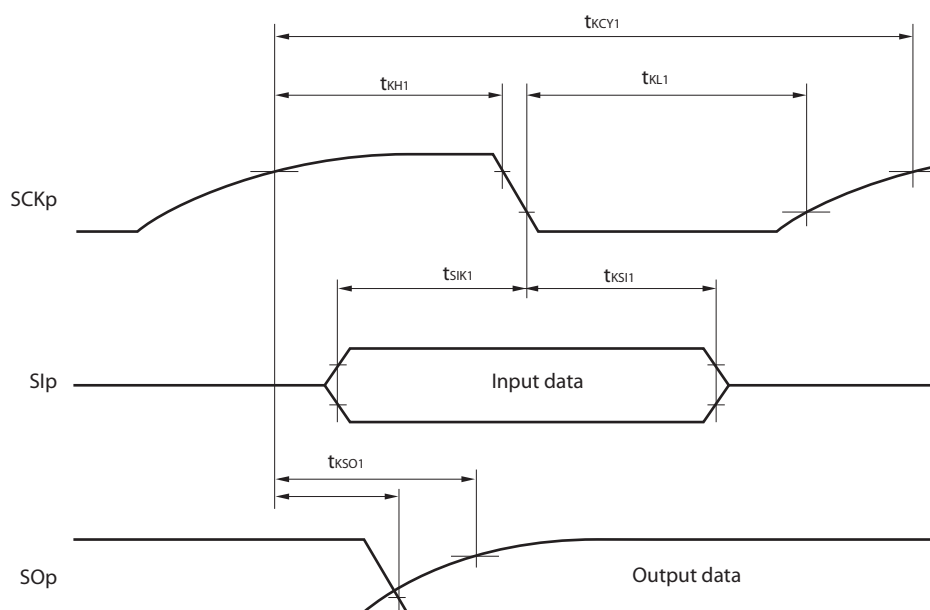
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	14/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	12/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	20/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	16/ f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	24 MHz < f _{MCK}	48/ f _{MCK}		—		—		ns
			20 MHz < f _{MCK} ≤ 24 MHz	36/ f _{MCK}		—		—		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/ f _{MCK}		—		—		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/ f _{MCK}		—		—		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/ f _{MCK}		16/ f _{MCK}		—		ns
			f _{MCK} ≤ 4 MHz	10/ f _{MCK}		10/ f _{MCK}		10/ f _{MCK}		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Hold time when SCLA0 = “L”	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	
Hold time when SCLA0 = “H”	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		250		250		ns	
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	3.45	0	3.45	μs	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	

(Notes, Caution and Remark are listed on the next page.)

<R>

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
Conversion time	t _{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI14	0			V _{DD}	V
		ANI16 to ANI26	0			EV _{DD0}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 4}				V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 4}				V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C	100,000			
		Retained for 20 years T _A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

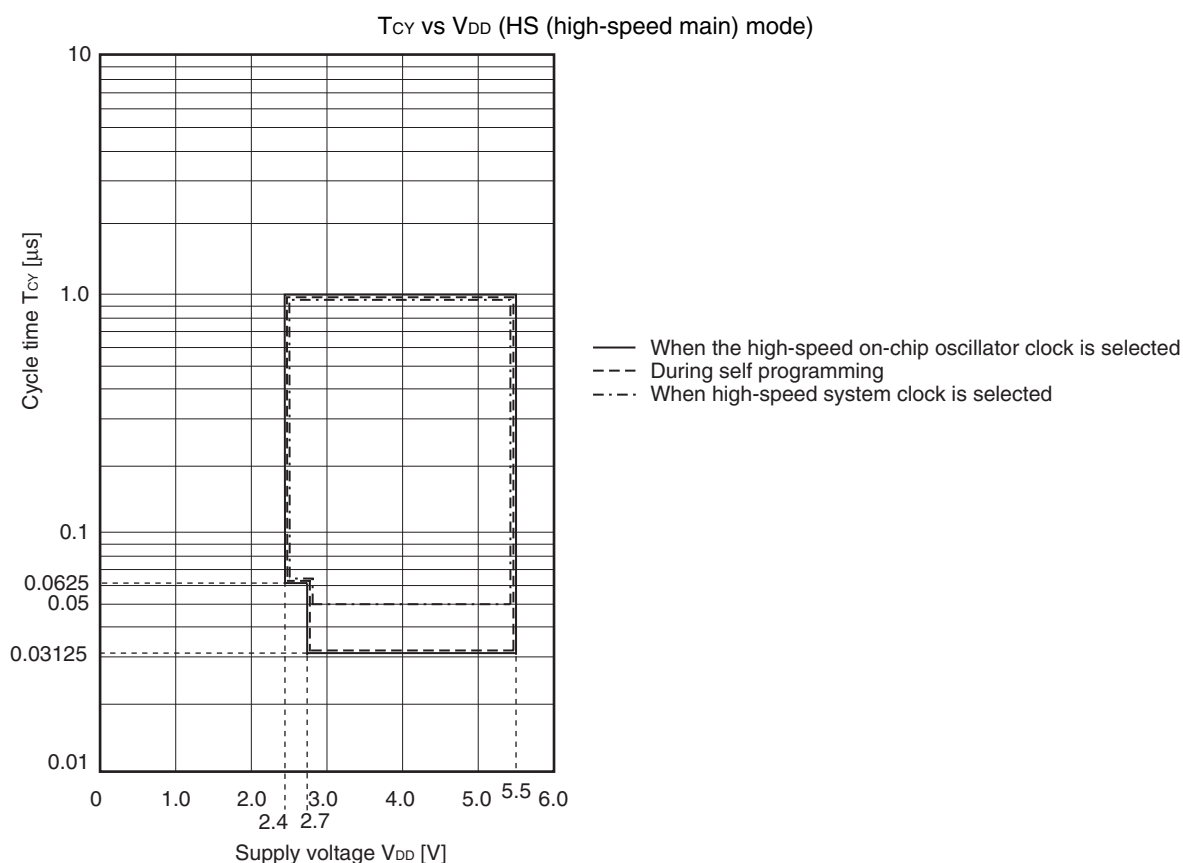
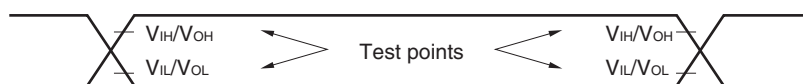
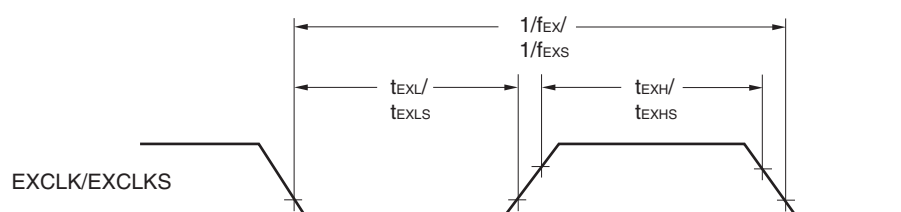
2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

Minimum Instruction Execution Time during Main System Clock Operation**AC Timing Test Points****External System Clock Timing**

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$) ^{Note}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$) ^{Note}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output ^{Note}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

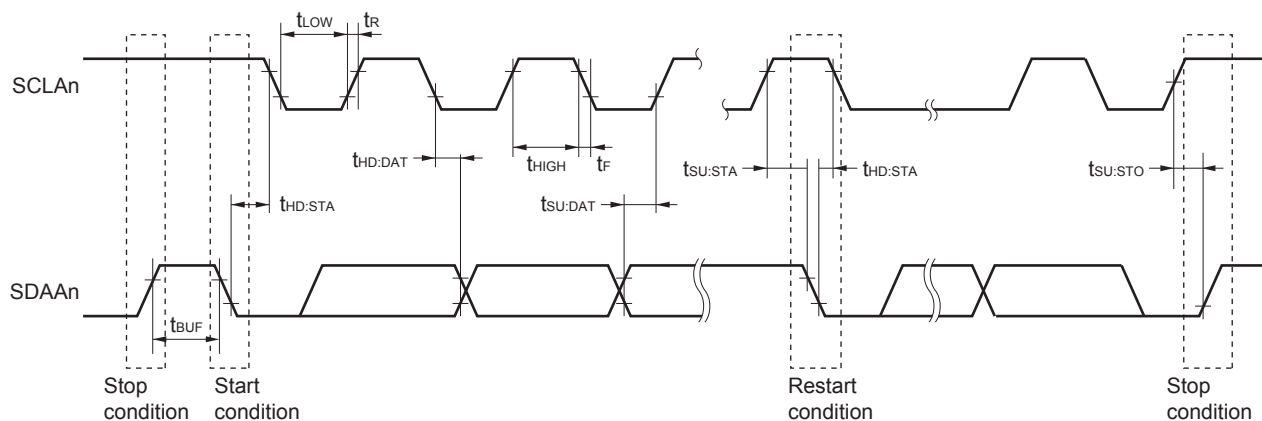
Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

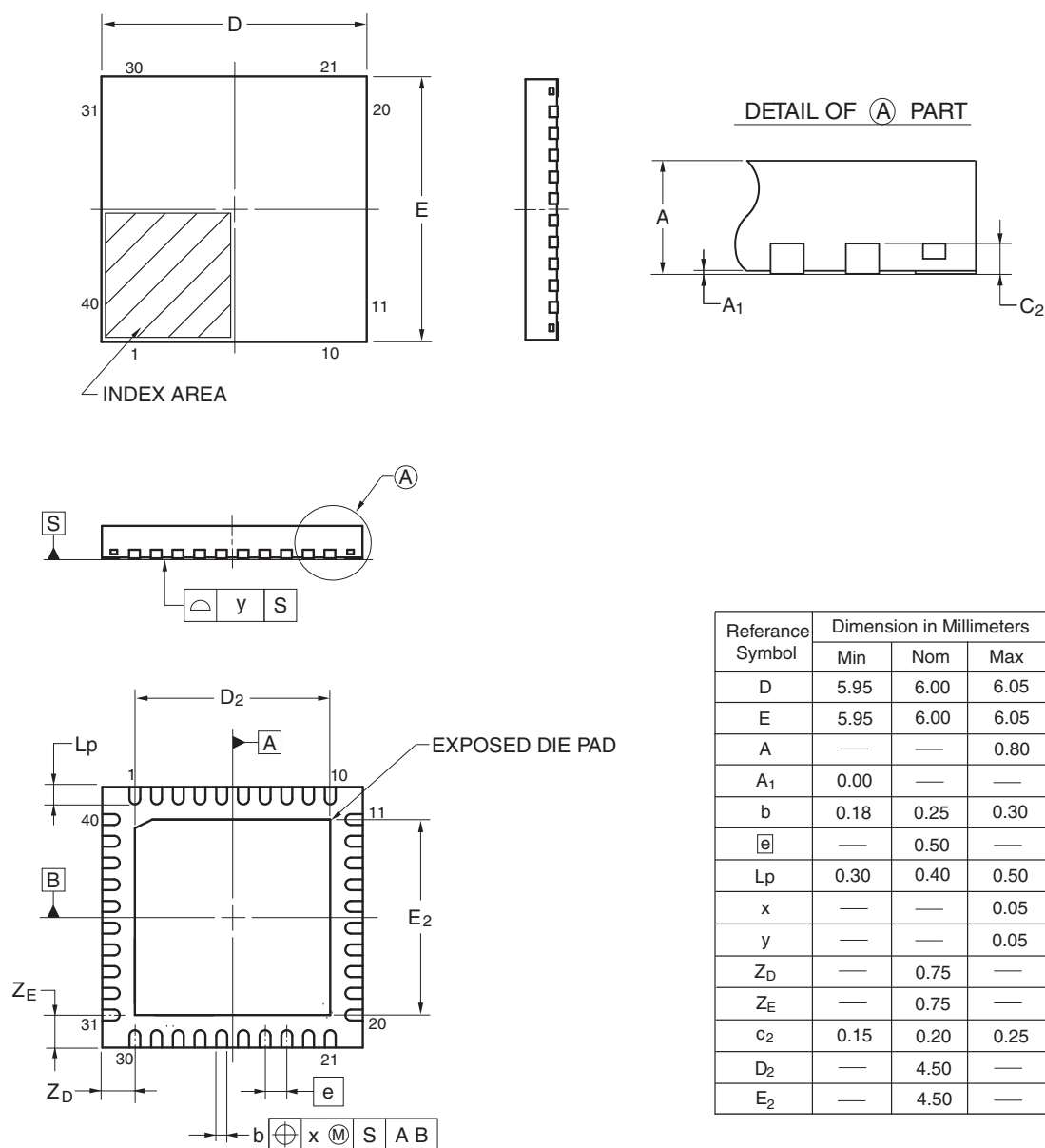
IICA serial transfer timing

**Remark** n = 0, 1

4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,
 R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,
 R5F101EHDNA
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,
 R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



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R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,
 R5F100LKAFB, R5F100LLAFB
 R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB,
 R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
 R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,
 R5F100LKDFB, R5F100LLDFB
 R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LDFB, R5F101LGDFB, R5F101LHDFB,
 R5F101LJDFB, R5F101LKDFB, R5F101LLDFB
 R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB,
 R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

