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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gadna-w0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gadna-w0</a>

Table 1-1. List of Ordering Part Numbers

(6/12)

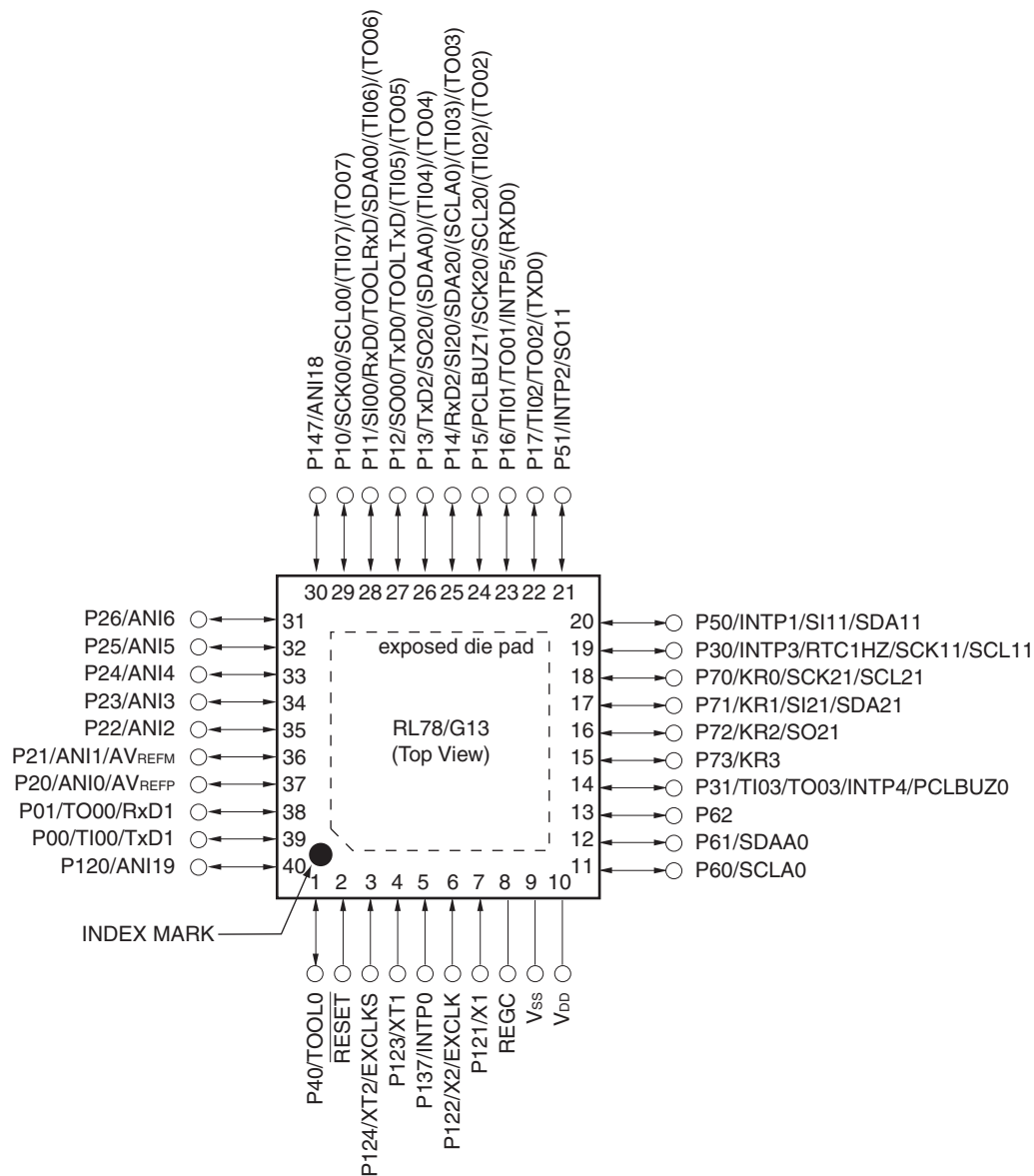
Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
		Not mounted	D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Not mounted	A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



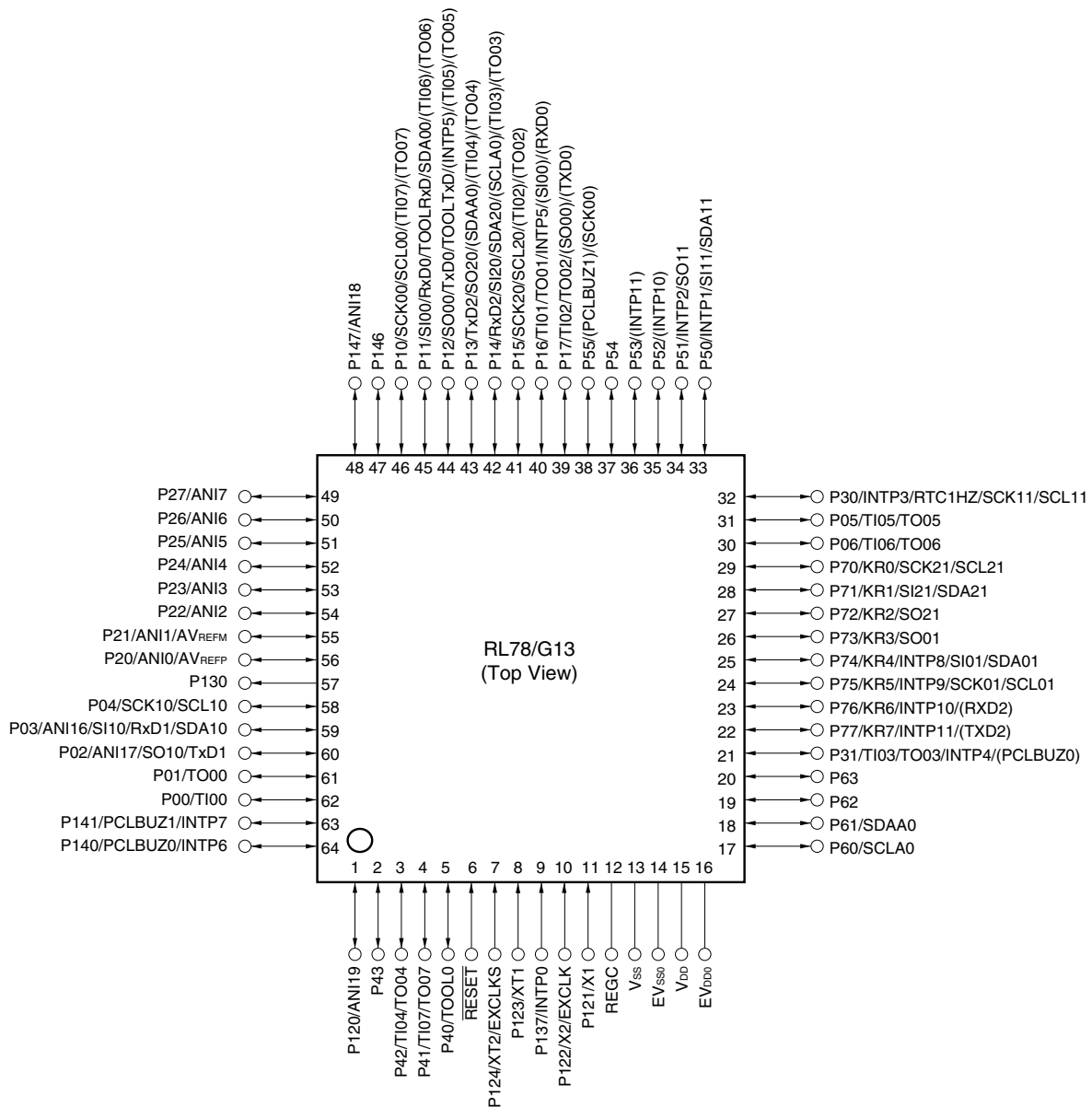
**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to Vss.

## 1.3.11 64-pin products

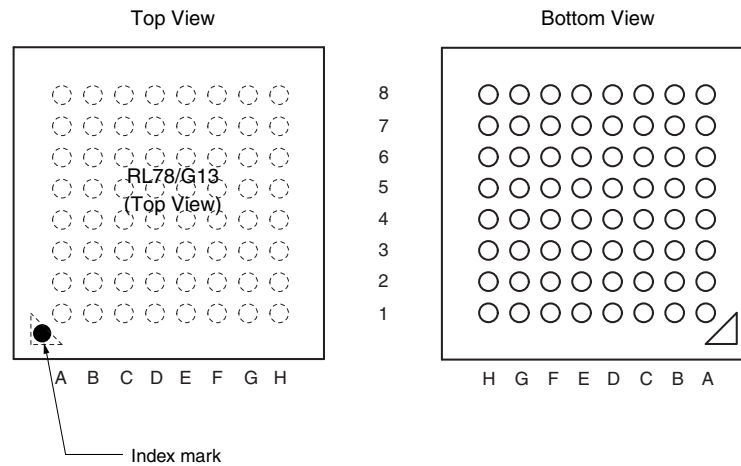
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



- Cautions**
1. Make EV<sub>SS0</sub> pin the same potential as V<sub>SS</sub> pin.
  2. Make V<sub>DD</sub> pin the potential that is higher than EV<sub>DD0</sub> pin.
  3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
  2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD0</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS0</sub> pins to separate ground lines.
  3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05	C1	P51/INTP2/SO11	E1	P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)	G1	P146
A2	P30/INTP3/RTC1HZ/SCK11/SCL11	C2	P71/KR1/SI21/SDA21	E2	P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)	G2	P25/ANI5
A3	P70/KR0/SCK21/SCL21	C3	P74/KR4/INTP8/SI01/SDA01	E3	P15/SCK20/SCL20/(TI02)/(TO02)	G3	P24/ANI4
A4	P75/KR5/INTP9/SCK01/SCL01	C4	P52/(INTP10)	E4	P16/TI01/TO01/INTP5/(SI00)/(RxD0)	G4	P22/ANI2
A5	P77/KR7/INTP11/(TxD2)	C5	P53/(INTP11)	E5	P03/ANI16/SI10/RxD1/SDA10	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/TI07/TO07	G6	P02/ANI17/SO10/TxD1
A7	P60/SCLA0	C7	V <sub>SS</sub>	E7	RESET	G7	P00/TI00
A8	EV <sub>DD0</sub>	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/INTP1/SI11/SDA11	D1	P55/(PCLBUZ1)/(SCK00)	F1	P10/SCK00/SCL00/(TI07)/(TO07)	H1	P147/ANI18
B2	P72/KR2/SO21	D2	P06/TI06/TO06	F2	P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)	H2	P27/ANI7
B3	P73/KR3/SO01	D3	P17/TI02/TO02/(SO00)/(TxD0)	F3	P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)	H3	P26/ANI6
B4	P76/KR6/INTP10/(RxD2)	D4	P54	F4	P21/ANI1/AV <sub>REFM</sub>	H4	P23/ANI3
B5	P31/TI03/TO03/INTP4/(PCLBUZ0)	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10	H5	P20/ANI0/AV <sub>REFP</sub>
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V <sub>DD</sub>	D7	REGC	F7	P01/TO00	H7	P140/PCLBUZ0/INTP6
B8	EV <sub>SS0</sub>	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

**Cautions** 1. Make EV<sub>SS0</sub> pin the same potential as V<sub>SS</sub> pin.

2. Make V<sub>DD</sub> pin the potential that is higher than EV<sub>DD0</sub> pin.

3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks** 1. For pin identification, see 1.4 Pin Identification.

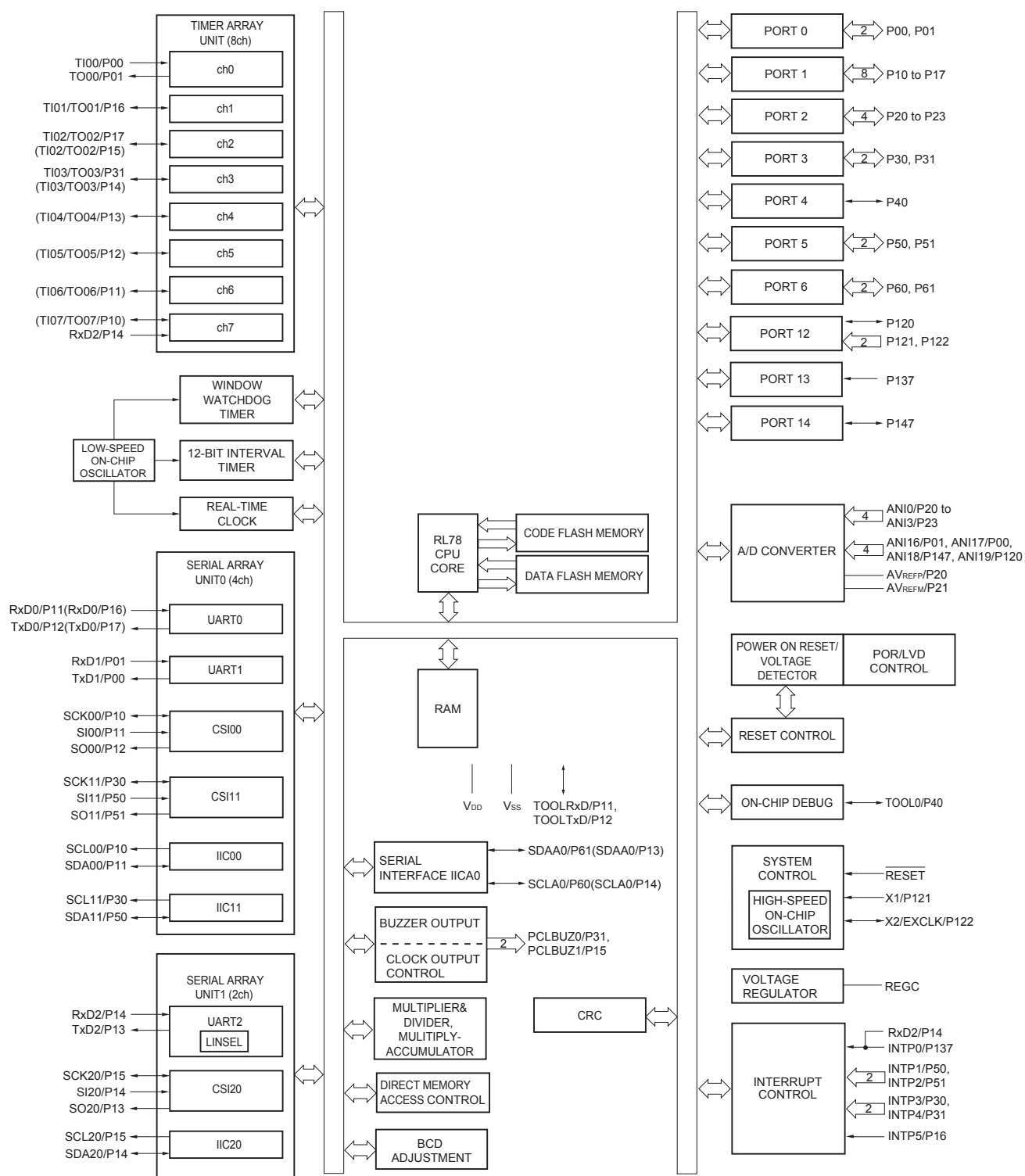
2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD0</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS0</sub> pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.4 Pin Identification

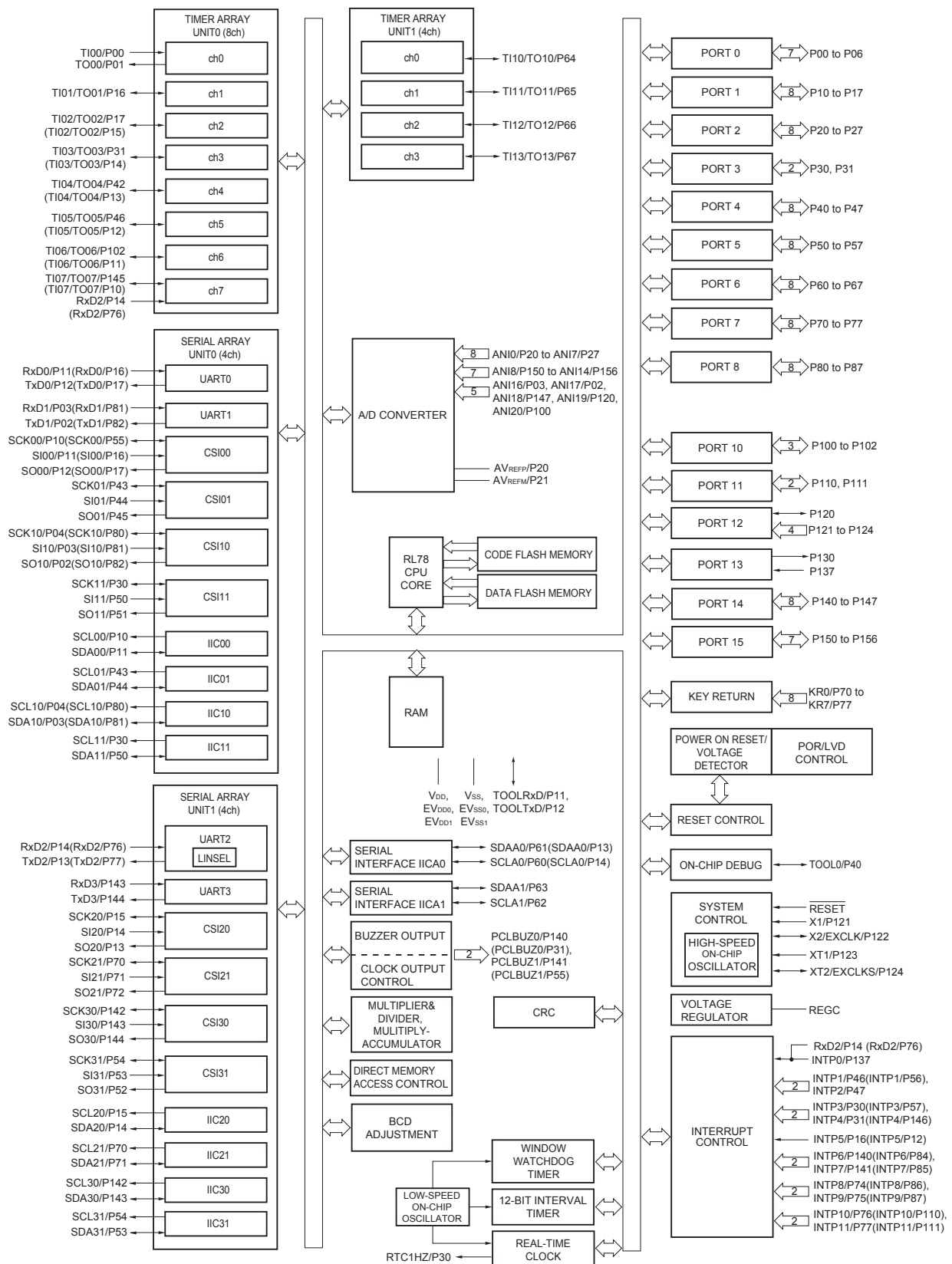
ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI26:	Analog input	RESET:	Reset
AV <sub>REFM</sub> :	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AV <sub>REFP</sub> :	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EV <sub>DD0</sub> , EV <sub>DD1</sub> :	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EV <sub>SS0</sub> , EV <sub>SS1</sub> :	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30,	
KR0 to KR7:	Key return	SDA31:	Serial data input/output
P00 to P07:	Port 0	SI00, SI01, SI10, SI11,	
P10 to P17:	Port 1	SI20, SI21, SI30, SI31:	Serial data input
P20 to P27:	Port 2	SO00, SO01, SO10,	
P30 to P37:	Port 3	SO11, SO20, SO21,	
P40 to P47:	Port 4	SO30, SO31:	Serial data output
P50 to P57:	Port 5	TI00 to TI07,	
P60 to P67:	Port 6	TI10 to TI17:	Timer input
P70 to P77:	Port 7	TO00 to TO07,	
P80 to P87:	Port 8	TO10 to TO17:	Timer output
P90 to P97:	Port 9	TOOL0:	Data input/output for tool
P100 to P106:	Port 10	TOOLRxD, TOOLTxD:	Data input/output for external device
P110 to P117:	Port 11	TxD0 to TxD3:	Transmit data
P120 to P127:	Port 12	V <sub>DD</sub> :	Power supply
P130, P137:	Port 13	V <sub>SS</sub> :	Ground
P140 to P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
P150 to P156:	Port 15	XT1, XT2:	Crystal oscillator (subsystem clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

## 1.5.4 30-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.13 100-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.



[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—
RAM (KB)		2 to 16 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)									
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)									
		30.5 μs (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)									
Instruction set		<ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)		31 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)		34 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 11)		38 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 13)		48 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	—		—		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3 <sup>Note2</sup> ), 8 channels (PWM outputs: 7 <sup>Note2, Note3</sup> )		5 channels (PWM outputs: 4 <sup>Note2</sup> ), 8 channels (PWM outputs: 7 <sup>Note2</sup> ) <sup>Note3</sup>						8 channels (PWM outputs: 7 <sup>Note2</sup> )	
	RTC output	1 channel • 1 Hz (subsystem clock: f <sub>SUB</sub> = 32.768 kHz)									

**Notes** 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

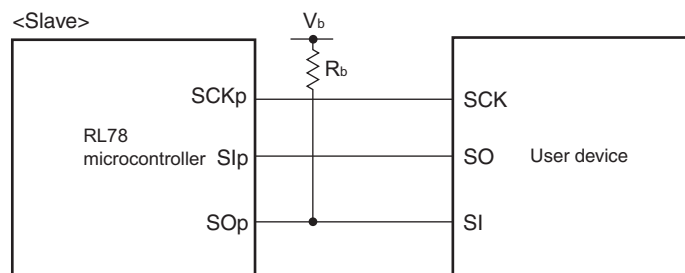
R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H

R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage
  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t <sub>SU:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
Data hold time (transmission)	t <sub>HD:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	ns

**Notes** 1. The value must also be equal to or less than f<sub>MCK</sub>/4.2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.3. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(3) When reference voltage (+) = V<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V<sub>SS</sub> (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T<sub>A</sub> = –40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V, Reference voltage (+) = V<sub>DD</sub>, Reference voltage (–) = V<sub>SS</sub>)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>		1.2	±10.5	LSB
Conversion time	t <sub>CONV</sub>	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	17		39	μs
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	57		95	μs
Conversion time	t <sub>CONV</sub>	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	17		39	μs
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±0.85	%FSR
Full-scale error <sup>Notes 1, 2</sup>	E <sub>FS</sub>	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±0.85	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±6.5	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±2.5	LSB
Analog input voltage	V <sub>AIN</sub>	ANI0 to ANI14	0			V <sub>DD</sub>	V
		ANI16 to ANI26	0			EV <sub>DD0</sub>	V
		Internal reference voltage (2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V, HS (high-speed main) mode)	V <sub>BGR</sub> <sup>Note 4</sup>				V
		Temperature sensor output voltage (2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V, HS (high-speed main) mode)	V <sub>TMPS25</sub> <sup>Note 4</sup>				V

**Notes** 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

## 3.3 DC Characteristics

## 3.3.1 Pin characteristics

(T<sub>A</sub> = -40 to +105°C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-3.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-10.0	mA
			2.4 V ≤ EV <sub>DD0</sub> < 2.7 V		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-30.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-19.0	mA
			2.4 V ≤ EV <sub>DD0</sub> < 2.7 V		-10.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-60.0	mA
	I <sub>OH2</sub>	Per pin for P20 to P27, P150 to P156	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V		-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V		-1.5	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>DD</sub> pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 7	f <sub>IH</sub> = 32 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.62	3.40	mA	
					V <sub>DD</sub> = 3.0 V		0.62	3.40	mA	
				f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.50	2.70	mA	
					V <sub>DD</sub> = 3.0 V		0.50	2.70	mA	
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.44	1.90	mA	
					V <sub>DD</sub> = 3.0 V		0.44	1.90	mA	
				HS (high-speed main) mode Note 7	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.31	2.10	mA
						Resonator connection		0.48	2.20	mA
					f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.31	2.10	mA
						Resonator connection		0.48	2.20	mA
			f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V		Square wave input		0.21	1.10	mA	
					Resonator connection		0.28	1.20	mA	
			f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V		Square wave input		0.21	1.10	mA	
					Resonator connection		0.28	1.20	mA	
			Subsystem clock operation		f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = −40°C	Square wave input		0.28	0.61	μA
						Resonator connection		0.47	0.80	μA
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +25°C	Square wave input		0.34	0.61	μA	
					Resonator connection		0.53	0.80	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +50°C	Square wave input		0.41	2.30	μA	
					Resonator connection		0.60	2.49	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +70°C	Square wave input		0.64	4.03	μA	
					Resonator connection		0.83	4.22	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +85°C	Square wave input		1.09	8.04	μA	
					Resonator connection		1.28	8.23	μA	
			f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +105°C	Square wave input		5.50	41.00	μA		
				Resonator connection		5.50	41.00	μA		
	I <sub>DD3</sub> <sup>Note 6</sup>	STOP mode <sup>Note 8</sup>	T <sub>A</sub> = −40°C					0.19	0.52	μA
			T <sub>A</sub> = +25°C					0.25	0.52	μA
			T <sub>A</sub> = +50°C					0.32	2.21	μA
			T <sub>A</sub> = +70°C					0.55	3.94	μA
			T <sub>A</sub> = +85°C					1.00	7.95	μA
			T <sub>A</sub> = +105°C					5.00	40.00	μA

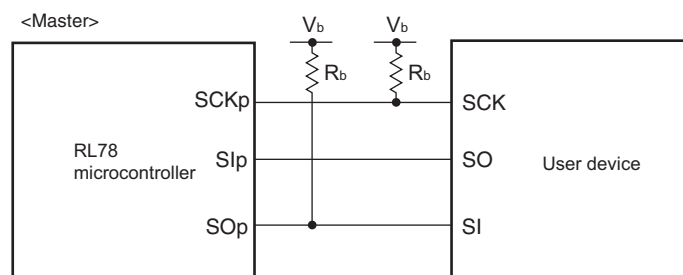
(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

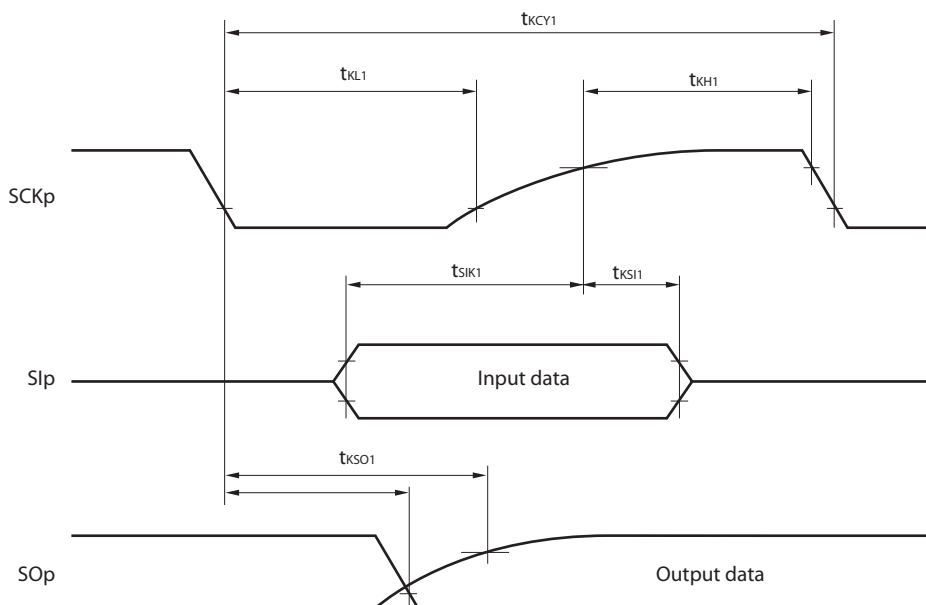
- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**CSI mode connection diagram (during communication at different potential)**

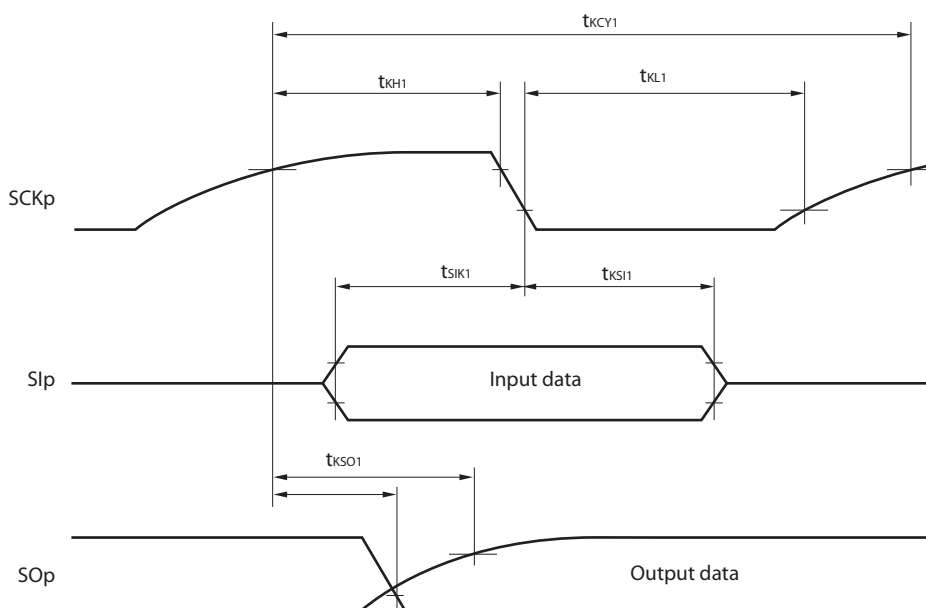
- Remarks**
1.  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[\text{F}]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**

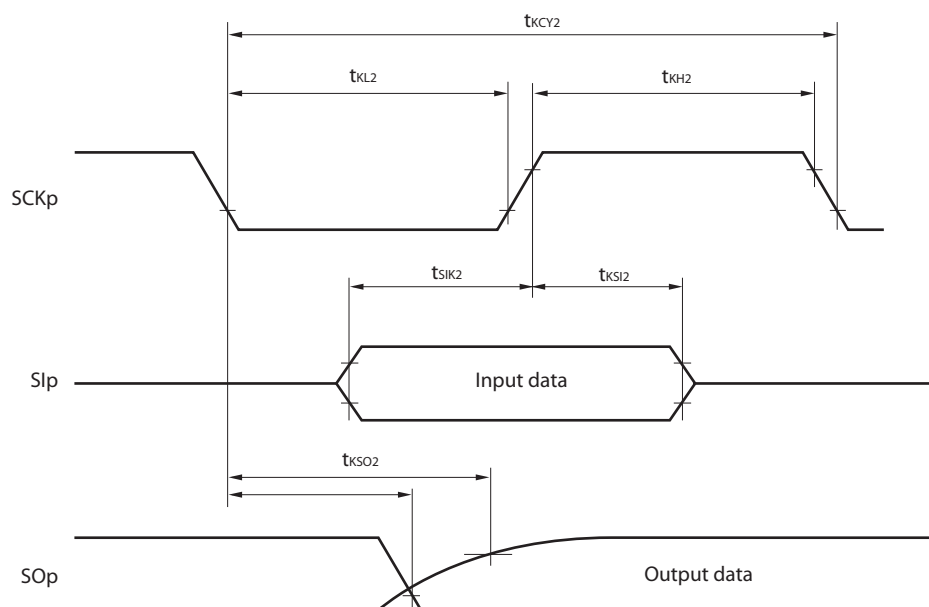


**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

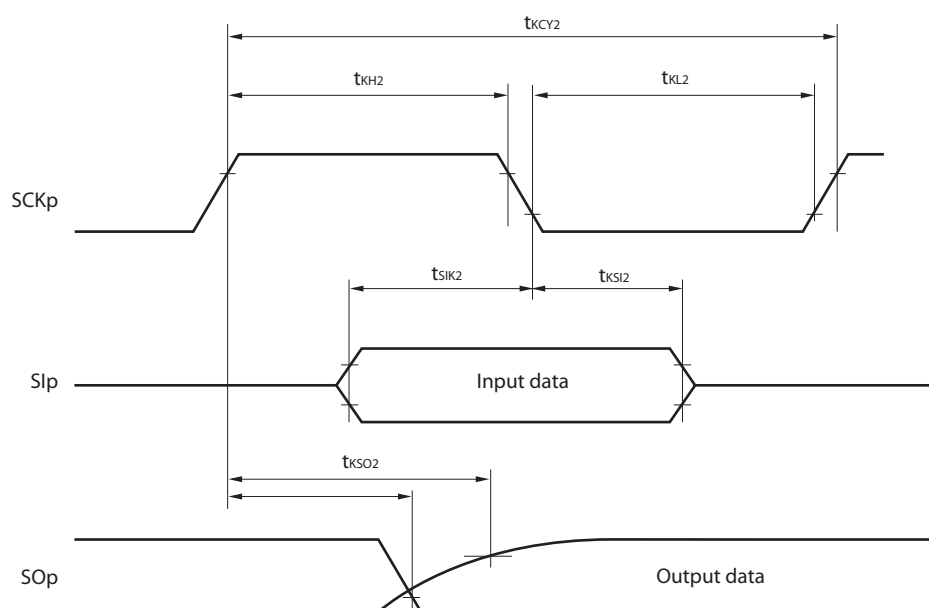


- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.

## 3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode: f <sub>CLK</sub> ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f <sub>CLK</sub> ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t <sub>SU:STA</sub>		4.7		0.6		μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>		4.0		0.6		μs
Hold time when SCLA0 = “L”	t <sub>LOW</sub>		4.7		1.3		μs
Hold time when SCLA0 = “H”	t <sub>HIGH</sub>		4.0		0.6		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of tHD:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

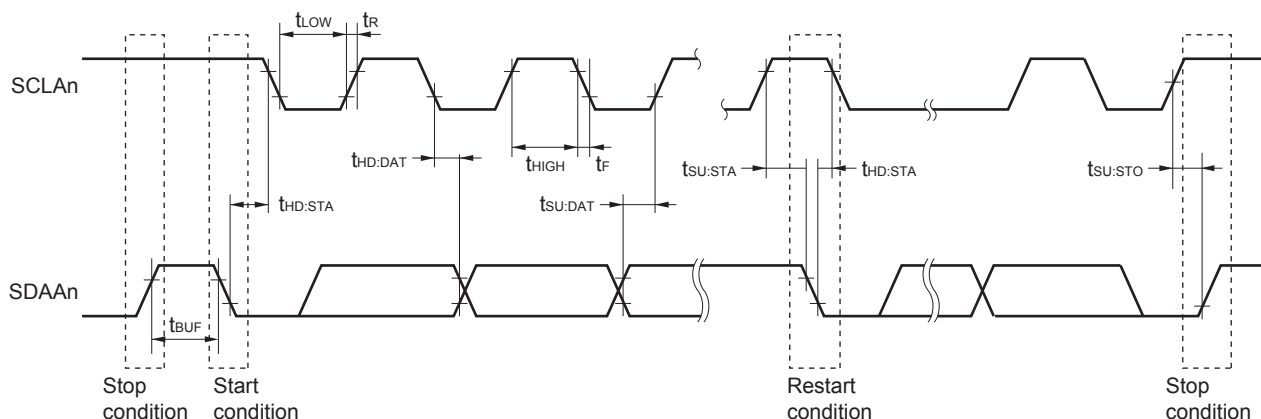
**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: Cb = 400 pF, Rb = 2.7 kΩ

Fast mode: Cb = 320 pF, Rb = 1.1 kΩ

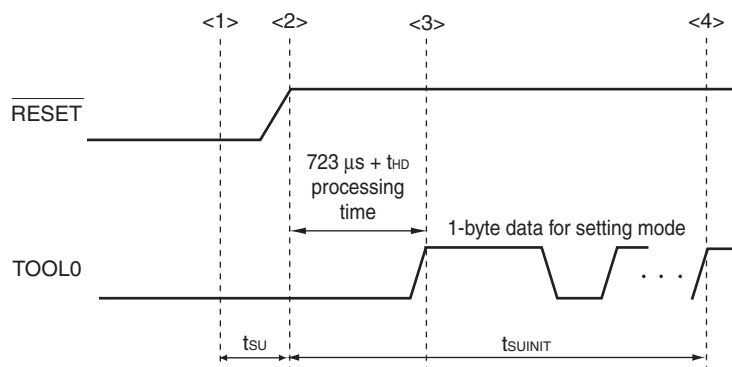
IICA serial transfer timing

**Remark** n = 0, 1

## 3.10 Timing of Entry to Flash Memory Programming Modes

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset must be released before the external reset is released.	1			ms



&lt;1&gt; The low level is input to the TOOL0 pin.

&lt;2&gt; The external reset is released (POR and LVD reset must be released before the external reset is released.).

&lt;3&gt; The TOOL0 pin is set to the high level.

&lt;4&gt; Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	118	Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		118	Modification of table and note in 2.6.3 POR circuit characteristics
		119	Modification of table in 2.6.4 LVD circuit characteristics
		120	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		120	Renamed to 2.6.5 Power supply voltage rising slope characteristics
		122	Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes
		123	Modification of caution 1 and description
		124	Modification of table and remark 3 in Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )
		126	Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics
		126	Modification of table in 3.2.2 On-chip oscillator characteristics
		127	Modification of note 3 in 3.3.1 Pin characteristics (1/5)
		128	Modification of note 3 in 3.3.1 Pin characteristics (2/5)
		133	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2)
		135	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2)
		137	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2)
		139	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2)
		140	Modification of (3) Peripheral Functions (Common to all products)
		142	Modification of table in 3.4 AC Characteristics
		143	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		143	Modification of figure of AC Timing Test Points
		143	Modification of figure of External System Clock Timing
		145	Modification of figure of AC Timing Test Points
		145	Modification of description, note 1, and caution in (1) During communication at same potential (UART mode)
		146	Modification of description in (2) During communication at same potential (CSI mode)
		147	Modification of description in (3) During communication at same potential (CSI mode)
		149	Modification of table, note 1, and caution in (4) During communication at same potential (simplified I <sup>2</sup> C mode)
		151	Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		152 to 154	Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		155	Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		156	Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		157, 158	Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		160, 161	Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)