



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gcafb-50

Table 1-1. List of Ordering Part Numbers

(7/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A	R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAF A#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAF A#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAFA#X0, R5F100JLAFA#X0 D R5F100JC DFA#V0, R5F100JD DFA#V0, R5F100JE DFA#V0, R5F100JF DFA#V0, R5F100JG DFA#V0, R5F100JH DFA#V0, R5F100JJ DFA#V0, R5F100JK DFA#V0, R5F100JL DFA#V0 R5F100JC DFA#X0, R5F100JD DFA#X0, R5F100JE DFA#X0, R5F100JF DFA#X0, R5F100JG DFA#X0, R5F100JH DFA#X0, R5F100JJ DFA#X0, R5F100JK DFA#X0, R5F100JL DFA#X0 G R5F100JCGFA#V0, R5F100JD GFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0, R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JD GFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0, R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0
		Not mounted	A	R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAF A#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JK AFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAF A#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JK AFA#X0, R5F101JLAFA#X0 D R5F101JC DFA#V0, R5F101JD DFA#V0, R5F101JE DFA#V0, R5F101JF DFA#V0, R5F101JG DFA#V0, R5F101JH DFA#V0, R5F101JJ DFA#V0, R5F101JK DFA#V0, R5F101JL DFA#V0 R5F101JC DFA#X0, R5F101JD DFA#X0, R5F101JE DFA#X0, R5F101JF DFA#X0, R5F101JG DFA#X0, R5F101JH DFA#X0, R5F101JJ DFA#X0, R5F101JK DFA#X0, R5F101JL DFA#X0

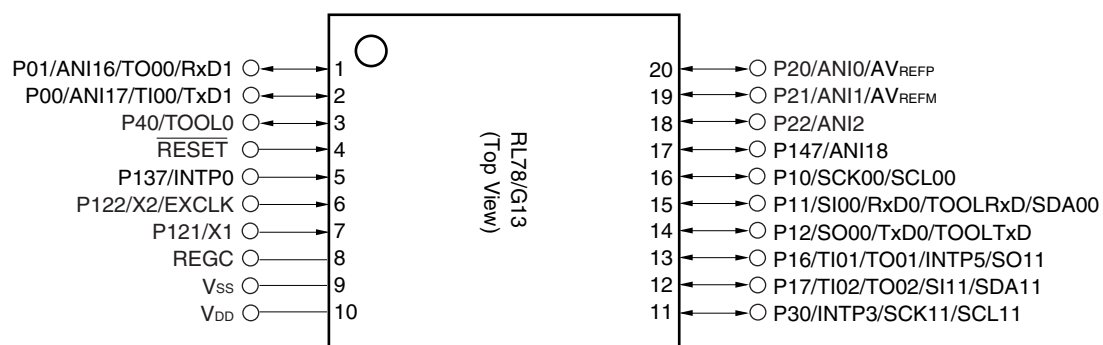
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

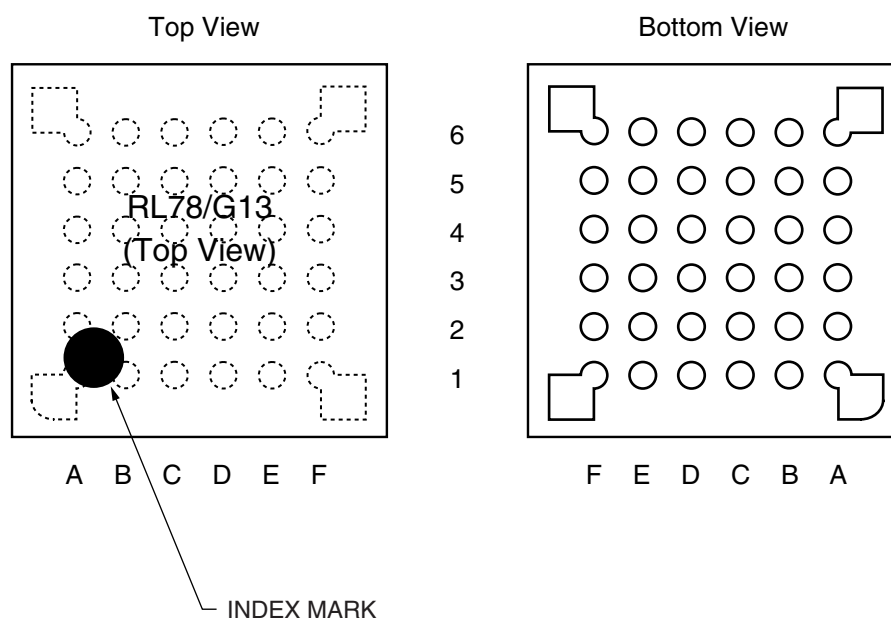


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remark For pin identification, see 1.4 Pin Identification.

1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	P60/SCLA0	V _{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V _{SS}	REGC	RESET	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV _{REFP}	P21/ANI1/ AV _{REFM}	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

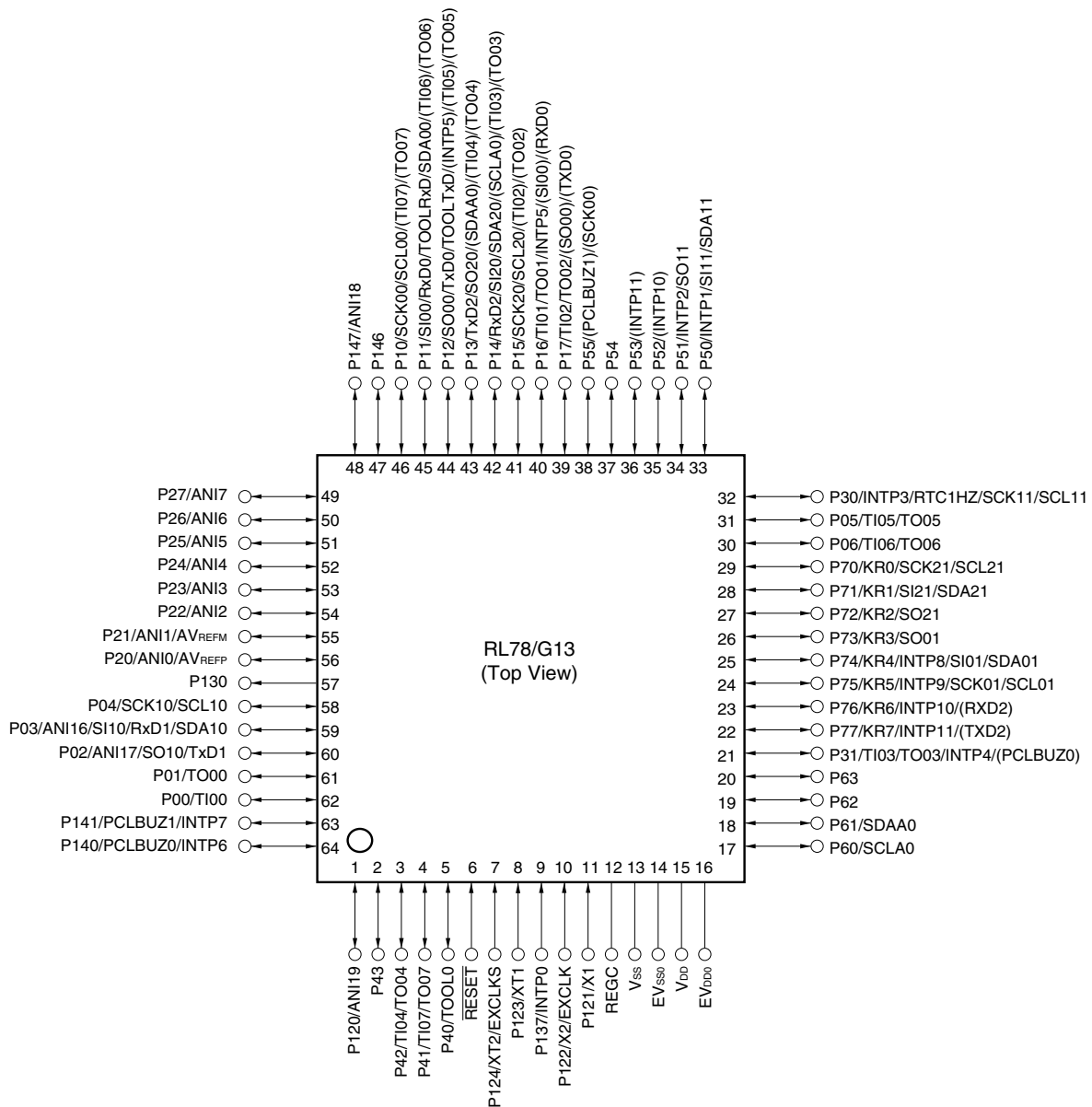
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



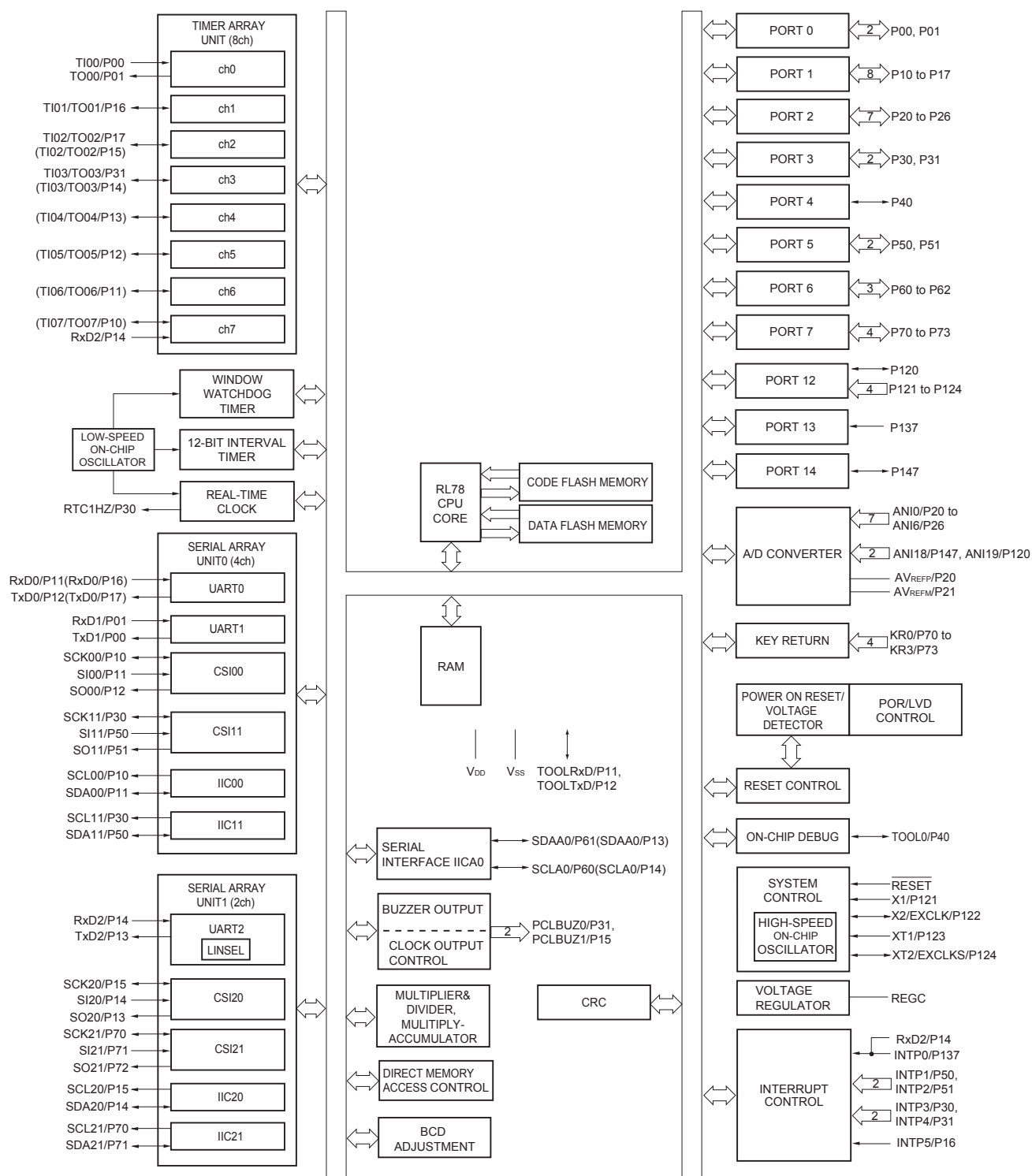
- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.4 Pin Identification

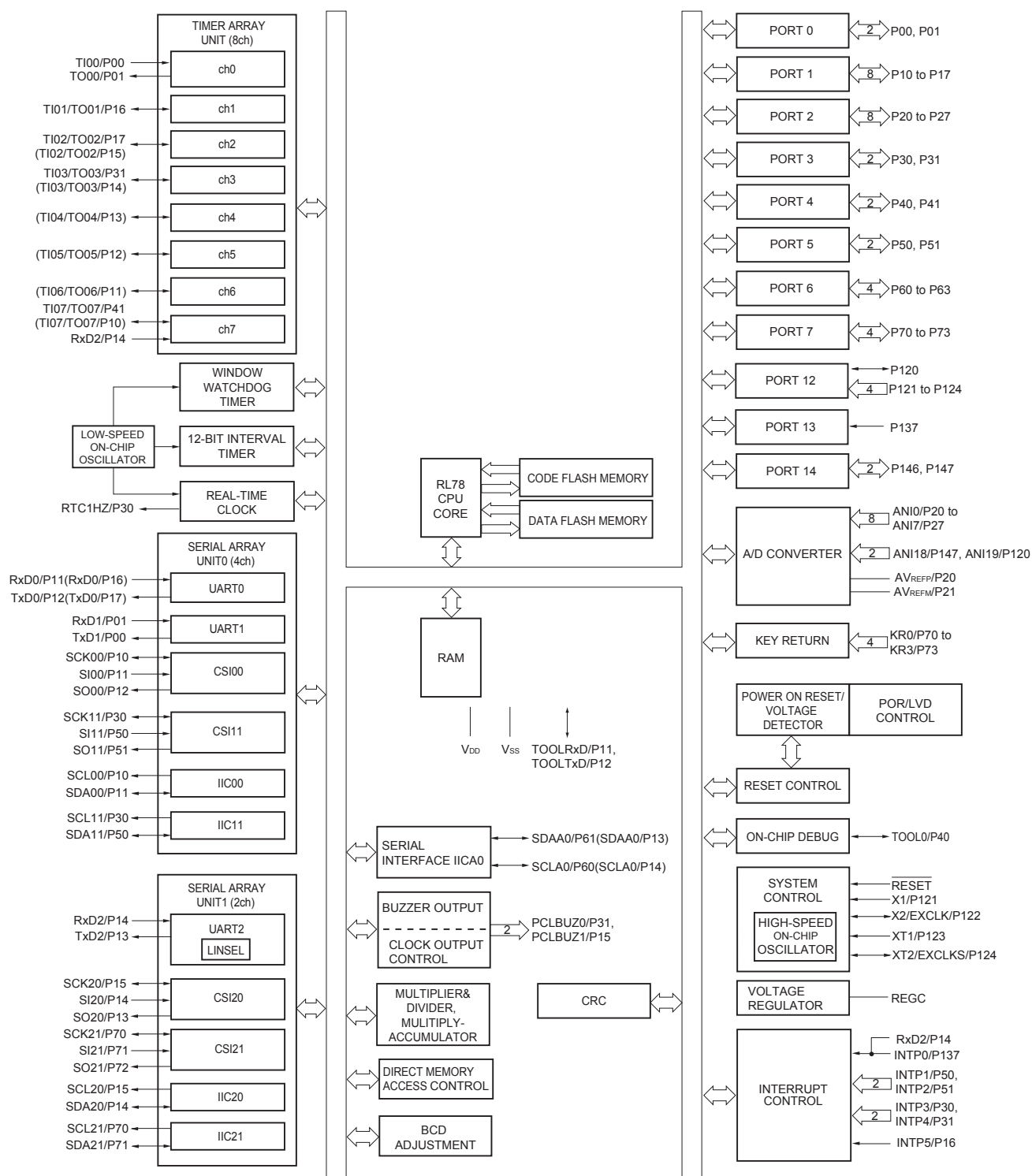
ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI26:	Analog input	RESET:	Reset
AVREFM:	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EVDD0, EVDD1:	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EVSS0, EVSS1:	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30,	
KR0 to KR7:	Key return	SDA31:	Serial data input/output
P00 to P07:	Port 0	SI00, SI01, SI10, SI11,	
P10 to P17:	Port 1	SI20, SI21, SI30, SI31:	Serial data input
P20 to P27:	Port 2	SO00, SO01, SO10,	
P30 to P37:	Port 3	SO11, SO20, SO21,	
P40 to P47:	Port 4	SO30, SO31:	Serial data output
P50 to P57:	Port 5	TI00 to TI07,	
P60 to P67:	Port 6	TI10 to TI17:	Timer input
P70 to P77:	Port 7	TO00 to TO07,	
P80 to P87:	Port 8	TO10 to TO17:	Timer output
P90 to P97:	Port 9	TOOL0:	Data input/output for tool
P100 to P106:	Port 10	TOOLRxD, TOOLTxD:	Data input/output for external device
P110 to P117:	Port 11	TxD0 to TxD3:	Transmit data
P120 to P127:	Port 12	V _{DD} :	Power supply
P130, P137:	Port 13	V _{SS} :	Ground
P140 to P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
P150 to P156:	Port 15	XT1, XT2:	Crystal oscillator (subsystem clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

1.5.7 40-pin products



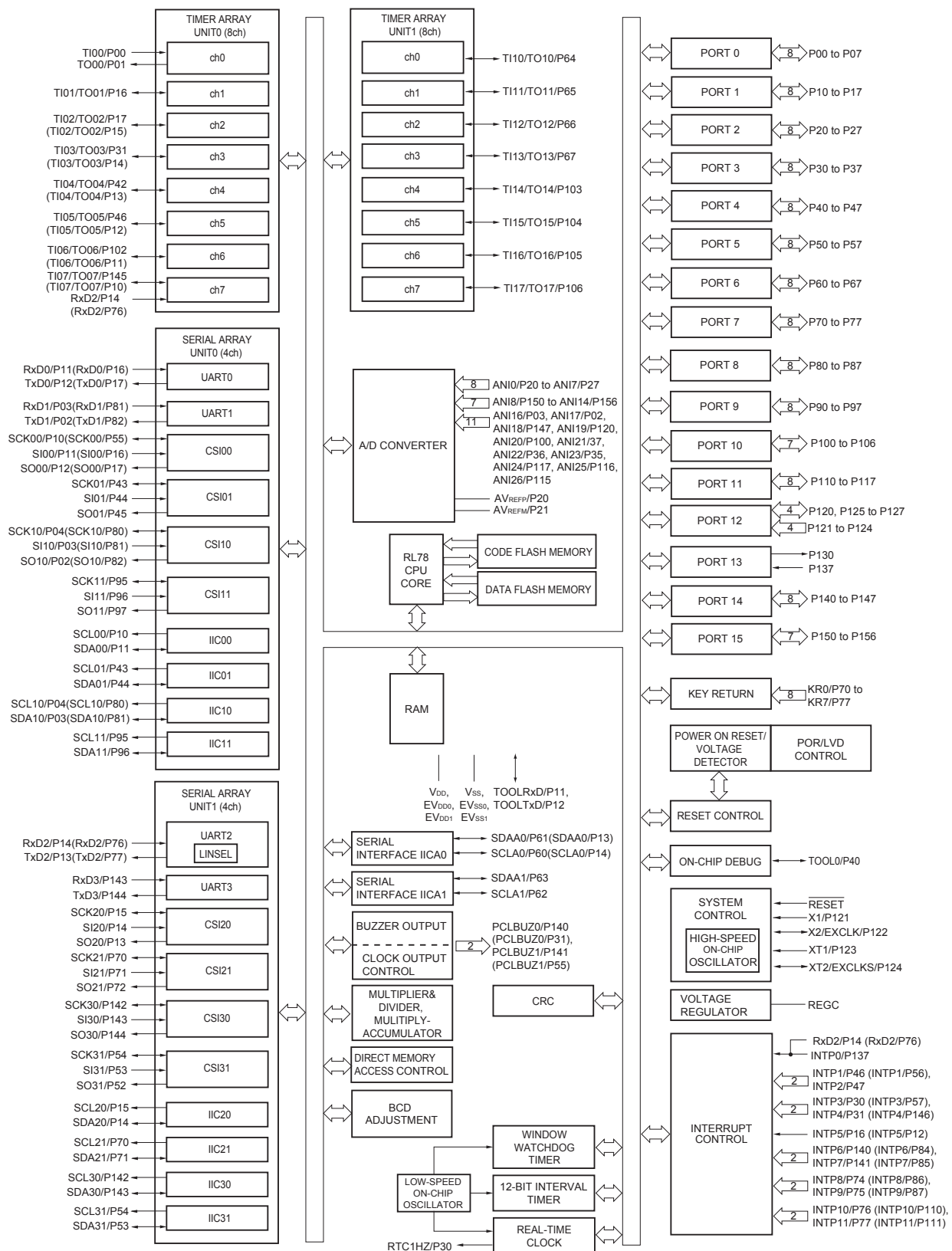
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.8 44-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output	—		1		1		2		2		2	
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)											
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface	[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I ² C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I ² C bus	—	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller	2 channels											
Vectored interrupt sources	Internal	23	24		24		27		27		27	
	External	3	5		5		6		6		6	
Key interrupt	—											
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector	• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function	Provided											
Power supply voltage	V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)											
Operating ambient temperature	T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)											

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products]					
		- CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel					
	I ² C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		- Reset by RESET pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access					
Power-on-reset circuit		- Power-on-reset: 1.51 V (TYP.) - Power-down-reset: 1.50 V (TYP.)					
Voltage detector		- Rising edge : 1.67 V to 4.06 V (14 stages) - Falling edge : 1.63 V to 3.98 V (14 stages)					
On-chip debug function		Provided					
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)					
Operating ambient temperature		T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)					

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R>

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV _{DD0}	EV _{DD0}	V
	V _{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	2.2	EV _{DD0}	V
			TTL input buffer 3.3 V ≤ EV _{DD0} < 4.0 V	2.0	EV _{DD0}	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	1.5	EV _{DD0}	V
	V _{IH3}	P20 to P27, P150 to P156	0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63	0.7EV _{DD0}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	0.2EV _{DD0}	V
	V _{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EV _{DD0} < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	0	0.32	V
	V _{IL3}	P20 to P27, P150 to P156	0		0.3V _{DD}	V
	V _{IL4}	P60 to P63	0		0.3EV _{DD0}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -10.0 mA	EV _{DD0} - 1.5		V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -3.0 mA	EV _{DD0} - 0.7		V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -2.0 mA	EV _{DD0} - 0.6		V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -1.5 mA	EV _{DD0} - 0.5		V
			1.6 V ≤ EV _{DD0} < 5.5 V, I _{OH1} = -1.0 mA	EV _{DD0} - 0.5		V
	V _{OH2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OH2} = -100 μA	V _{DD} - 0.5		V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 20 mA		1.3	V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 8.5 mA		0.7	V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 3.0 mA		0.6	V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 1.5 mA		0.4	V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 0.6 mA		0.4	V
			1.6 V ≤ EV _{DD0} < 5.5 V, I _{OL1} = 0.3 mA		0.4	V
	V _{OL2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OL2} = 400 μA		0.4	V
	V _{OL3}	P60 to P63	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 15.0 mA		2.0	V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 5.0 mA		0.4	V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 3.0 mA		0.4	V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 2.0 mA		0.4	V
			1.6 V ≤ EV _{DD0} < 5.5 V, I _{OL3} = 1.0 mA		0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(5) During communication at same potential (simplified I²C mode) (1/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(2/3)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSH1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 - 12		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 - 18		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		t _{KCY2} /2 - 50		ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 20		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 30		1/f _{MCK} + 30		1/f _{MCK} + 30		ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KS12}		1/f _{MCK} + 31		1/f _{MCK} + 31		1/f _{MCK} + 31		ns
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		2/f _{MCK} + 120		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		2/f _{MCK} + 214		2/f _{MCK} + 573		2/f _{MCK} + 573	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		2/f _{MCK} + 573		2/f _{MCK} + 573		2/f _{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with EV_{DD0} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

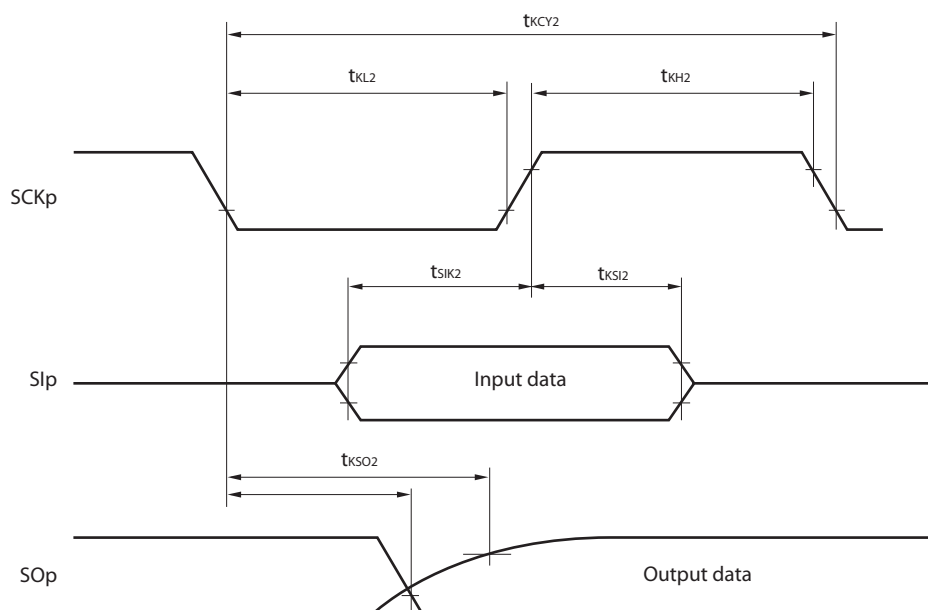
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

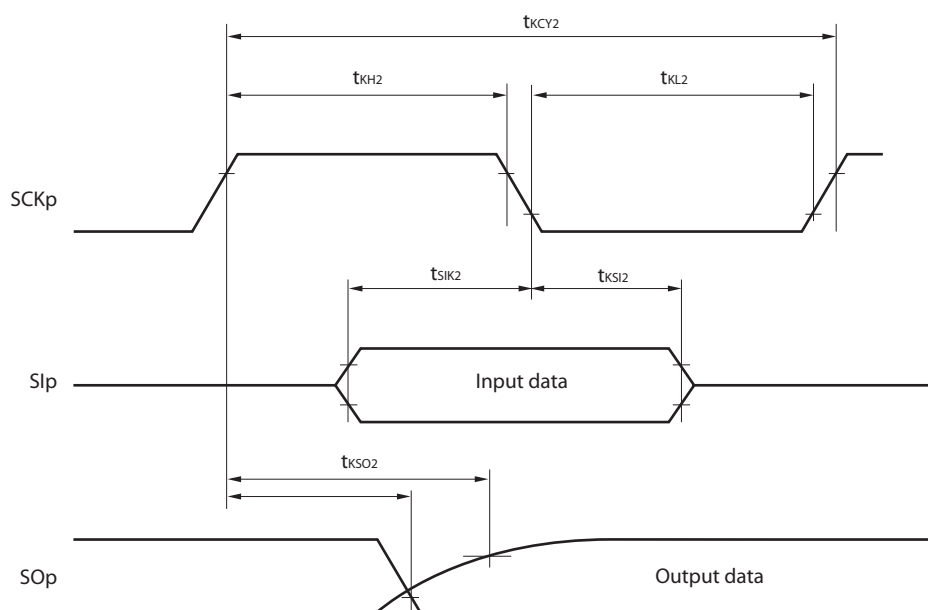
Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
 Use other CSI for communication at different potential.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	$0.8\text{EV}_{\text{DD0}}$	EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	2.2	EV_{DD0}	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	2.0	EV_{DD0}	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	1.5	EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P156	0.7V_{DD}		V_{DD}	V
	V_{IH4}	P60 to P63	$0.7\text{EV}_{\text{DD0}}$		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	$0.2\text{EV}_{\text{DD0}}$	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	0	0.32	V
	V_{IL3}	P20 to P27, P150 to P156	0		0.3V_{DD}	V
	V_{IL4}	P60 to P63	0		$0.3\text{EV}_{\text{DD0}}$	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V_{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0} , even in the N-ch open-drain mode.

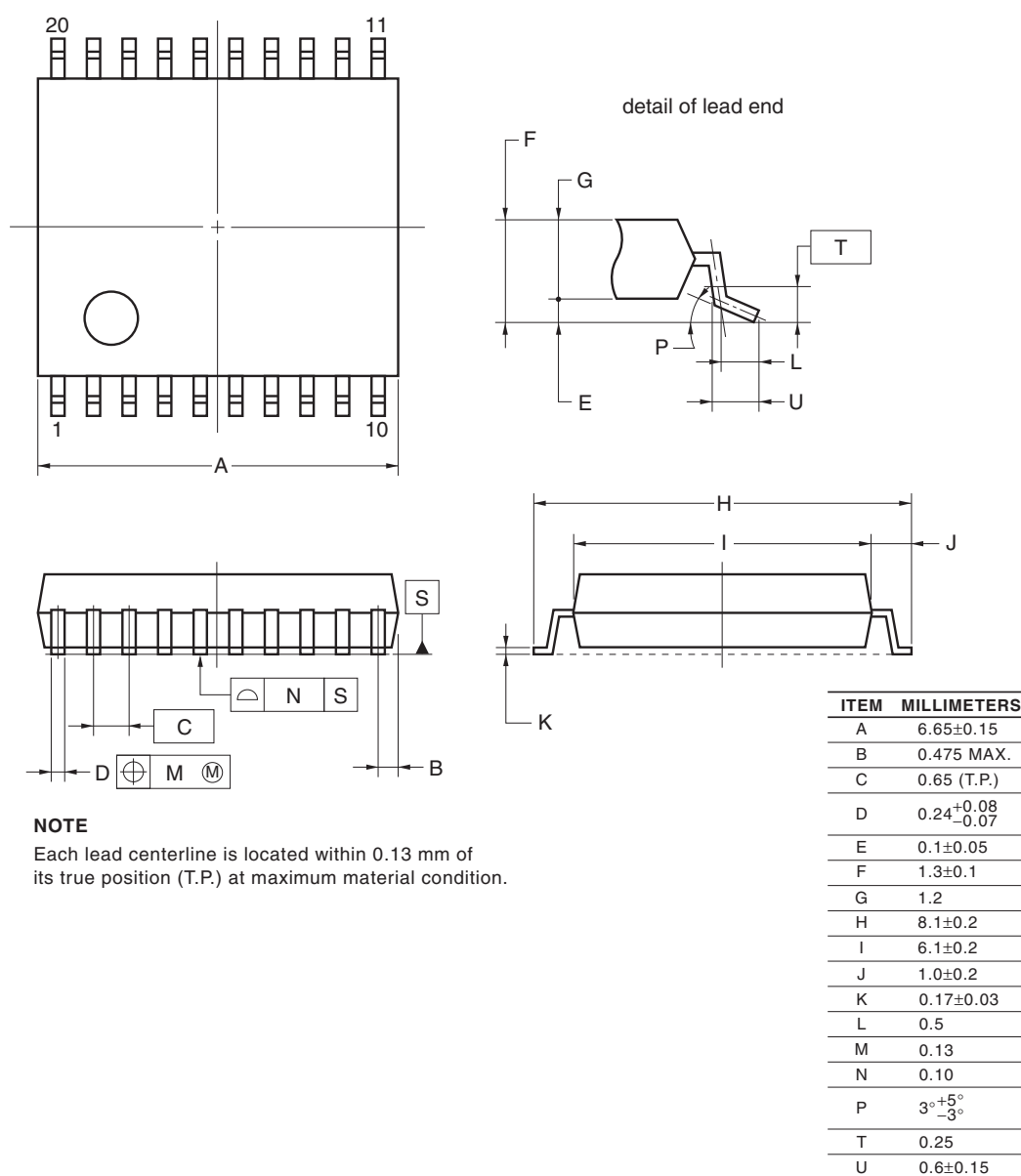
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP
 R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12

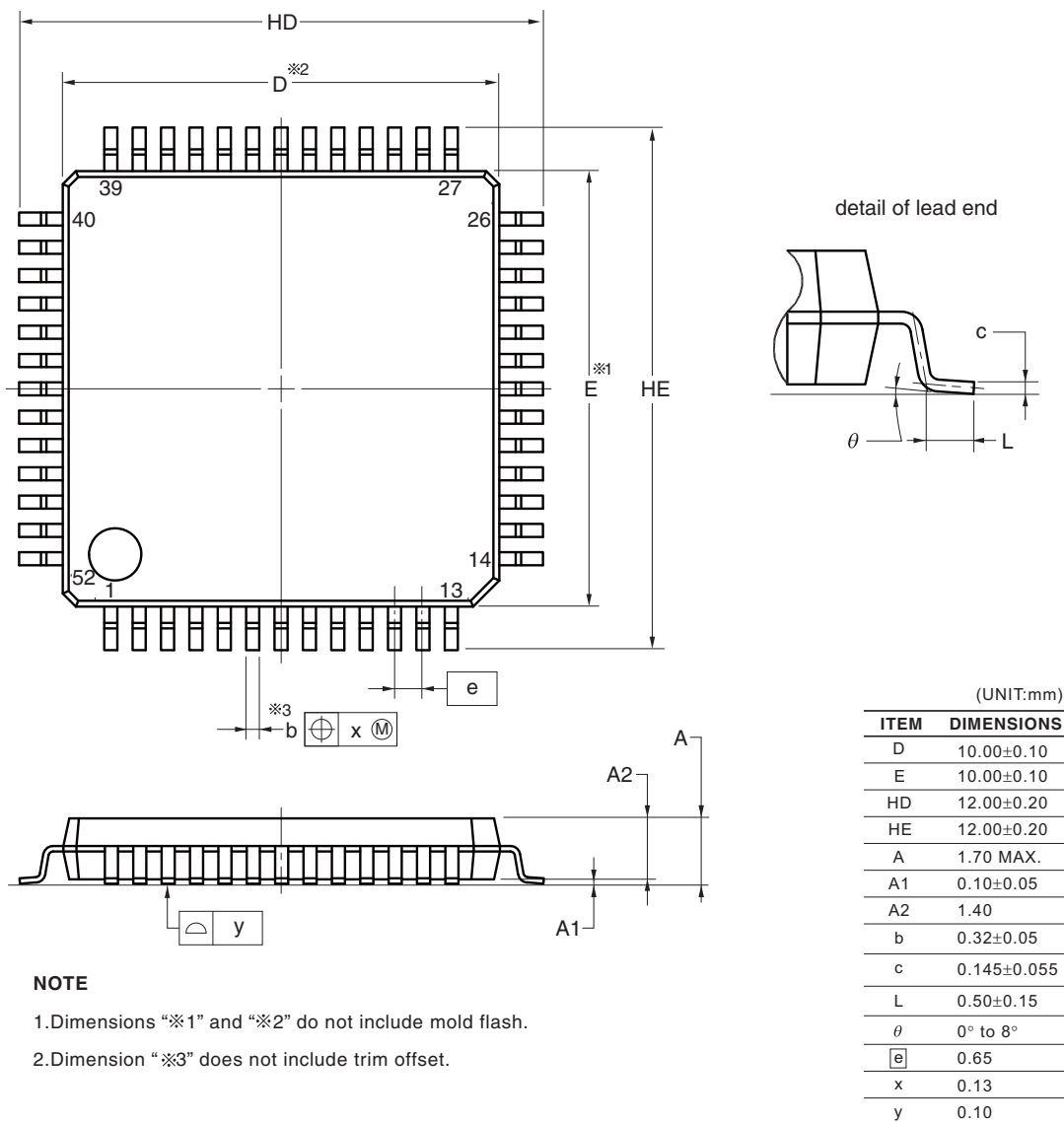


©2012 Renesas Electronics Corporation. All rights reserved.

4.10 52-pin Products

R5F100JCAFA, R5F100JDFA, R5F100JEFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFA, R5F100JKFA, R5F100JLAFA
 R5F101JCAFA, R5F101JDFA, R5F101JEFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFA, R5F101JKFA, R5F101JLAFA
 R5F100JCDA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDA, R5F100JDDFA, R5F100JKDA, R5F100JLDA
 R5F101JCDA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDA, R5F101JDDFA, R5F101JKDA, R5F101JLDA
 R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



© 2012 Renesas Electronics Corporation. All rights reserved.