What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.
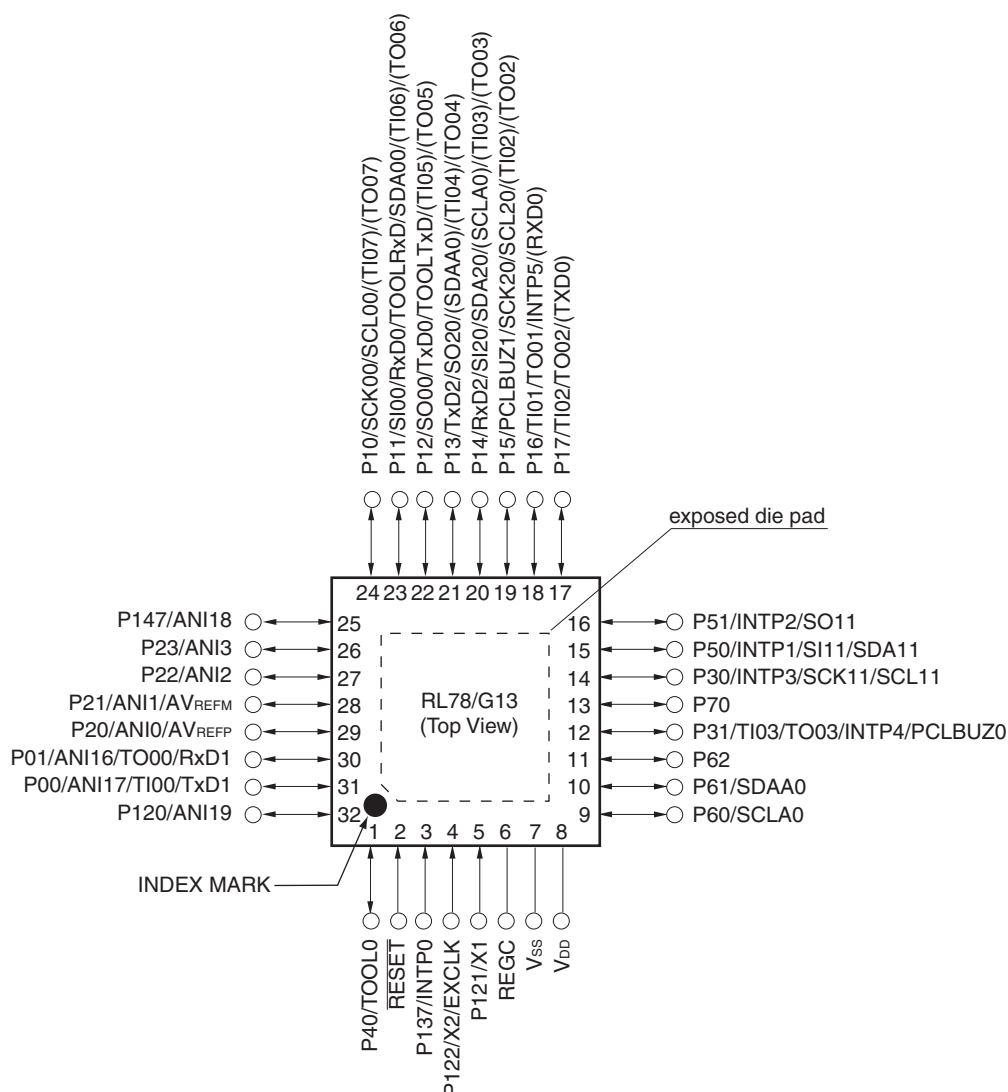
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gedfb-v0

1.3.5 32-pin products
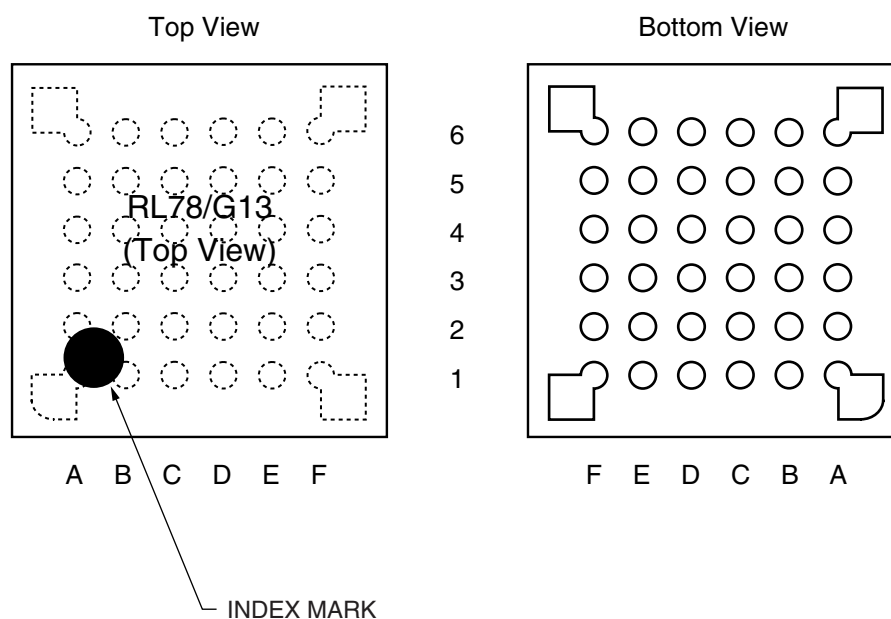
- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

P10/SCK00/SCL00/(TI07)/(TO07)
P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
P16/TI01/TO01/INTP5/(RXD0)
P17/TI02/TO02/(TXD0)

exposed die pad

24	23	22	21	20	19	18	17	

P147/ANI18 — 25
P23/ANI3 — 26
P22/ANI2 — 27
P21/ANI1/AV$_{REFM}$ — 28
P20/ANI0/AV$_{REFP}$ — 29
P01/ANI16/TO00/RxD1 — 30
P00/ANI17/TI00/TxD1 — 31
P120/ANI19 — 32

RL78/G13
(Top View)

16 — P51/INTP2/SO11
15 — P50/INTP1/SI11/SDA11
14 — P30/INTP3/SCK11/SCL11
13 — P70
12 — P31/TI03/TO03/INTP4/PCLBUZ0
11 — P62
10 — P61/SDAA0
9 — P60/SCLA0

INDEX MARK

1 2 3 4 5 6 7 8

P40/TOOL0
RESET
P137/INTP0
P122/X2/EXCLK
P121/X1
REGC
V$_{SS}$
V$_{DD}$

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
   3. It is recommended to connect an exposed die pad to Vss.

1.3.6 36-pin products

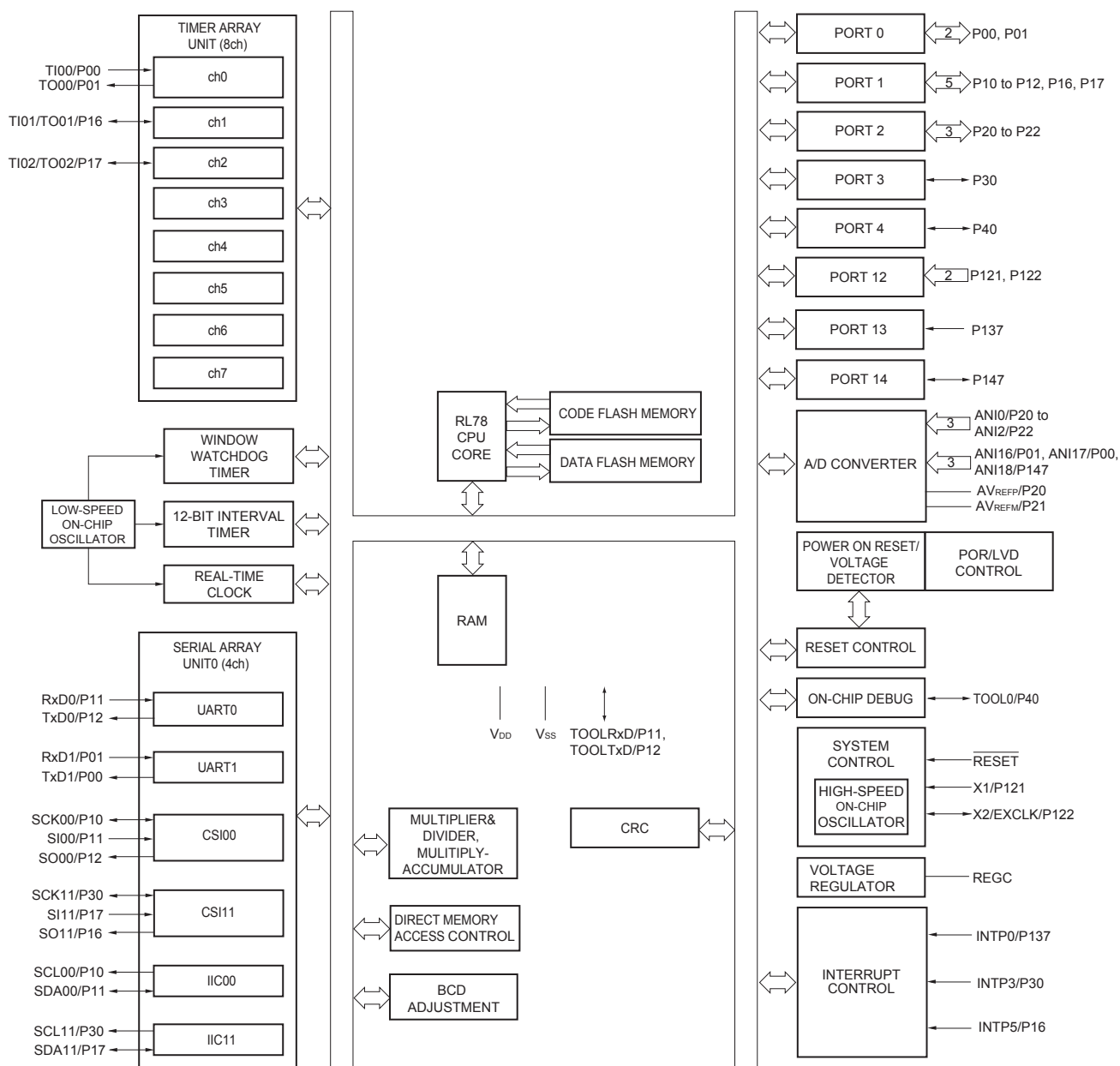- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

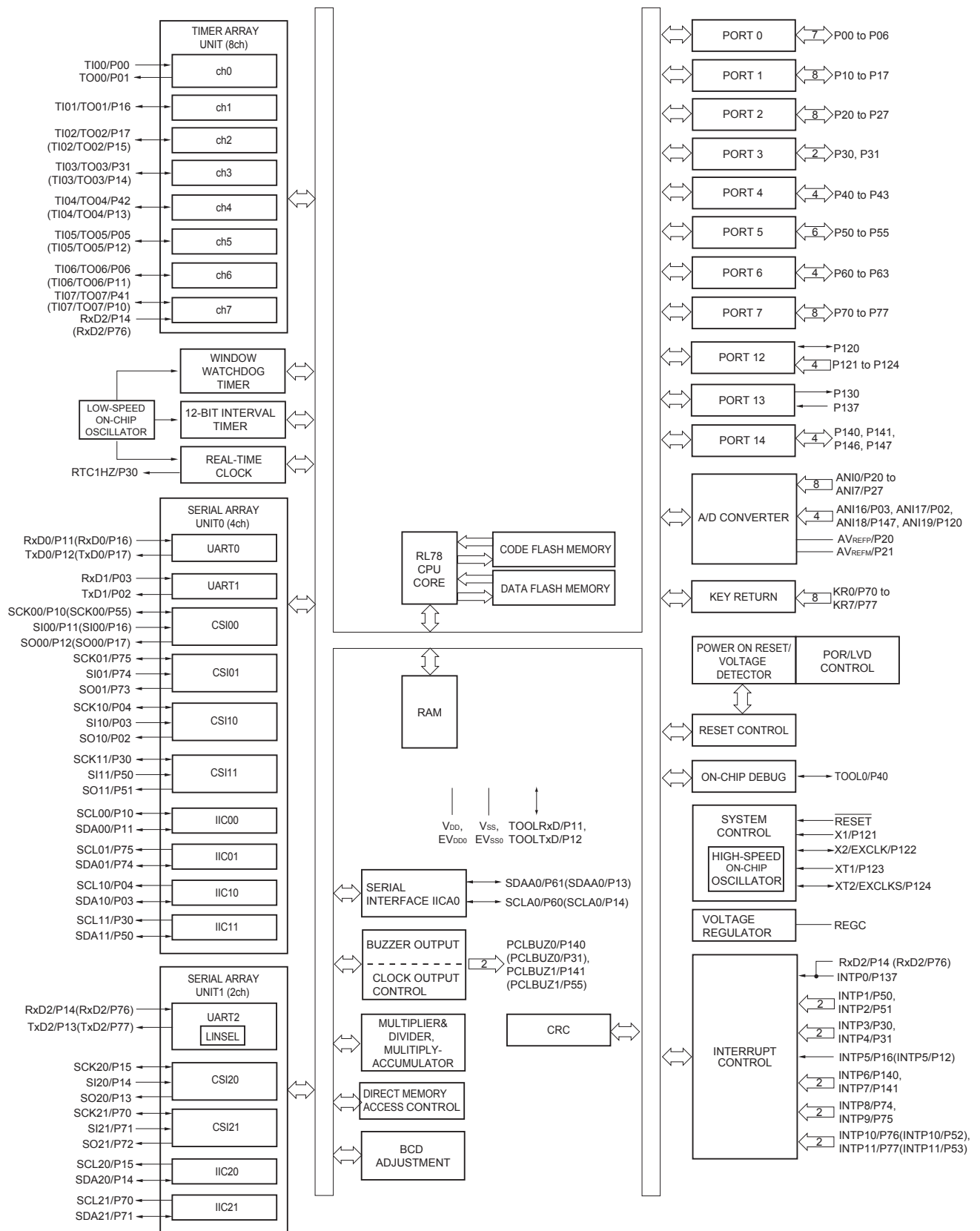Remarks 1. For pin identification, see **1.4 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

	A	B	C	D	E	F	
6	P60/SCLA0	V_{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V_{SS}	REGC	$\overline{\text{RESET}}$	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV_{REFP}	P21/ANI1/ AV_{REFM}	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

1.5 Block Diagram

1.5.1 20-pin products

1.5.11 64-pin products

TIMER ARRAY UNIT (8ch)

TI00/P00 — ch0
TO00/P01 — ch0

TI01/TO01/P16 — ch1

TI02/TO02/P17 (TI02/TO02/P15) — ch2

TI03/TO03/P31 (TI03/TO03/P14) — ch3

TI04/TO04/P42 (TI04/TO04/P13) — ch4

TI05/TO05/P05 (TI05/TO05/P12) — ch5

TI06/TO06/P06 (TI06/TO06/P11) — ch6

TI07/TO07/P41 (TI07/TO07/P10) — ch7
RxD2/P14 (RxD2/P76) — ch7

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR — 12-BIT INTERVAL TIMER

RTC1HZ/P30 — REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16) — UART0
TxD0/P12(TxD0/P17) — UART0

RxD1/P03 — UART1
TxD1/P02 — UART1

SCK00/P10(SCK00/P55) — CSI00
SI00/P11(SI00/P16) — CSI00
SO00/P12(SO00/P17) — CSI00

SCK01/P75 — CSI01
SI01/P74 — CSI01
SO01/P73 — CSI01

SCK10/P04 — CSI10
SI10/P03 — CSI10
SO10/P02 — CSI10

SCK11/P30 — CSI11
SI11/P50 — CSI11
SO11/P51 — CSI11

SCL00/P10 — IIC00
SDA00/P11 — IIC00

SCL01/P75 — IIC01
SDA01/P74 — IIC01

SCL10/P04 — IIC10
SDA10/P03 — IIC10

SCL11/P30 — IIC11
SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)

RxD2/P14(RxD2/P76) — UART2 LINSEL
TxD2/P13(TxD2/P77) — UART2 LINSEL

SCK20/P15 — CSI20
SI20/P14 — CSI20
SO20/P13 — CSI20

SCK21/P70 — CSI21
SI21/P71 — CSI21
SO21/P72 — CSI21

SCL20/P15 — IIC20
SDA20/P14 — IIC20

SCL21/P70 — IIC21
SDA21/P71 — IIC21

RL78 CPU CORE — CODE FLASH MEMORY
RL78 CPU CORE — DATA FLASH MEMORY

RAM

V_{DD}, EV_{DD0} V_{SS}, EV_{SS0} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13)
SERIAL INTERFACE IICA0 — SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL — 2 — PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P141 (PCLBUZ1/P55)

MULTIPLIER& DIVIDER, MULILTIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 7 — P00 to P06
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 4 — P40 to P43
PORT 5 — 6 — P50 to P55
PORT 6 — 4 — P60 to P63
PORT 7 — 8 — P70 to P77
PORT 12 — P120
PORT 12 — 4 — P121 to P124
PORT 13 — P130
PORT 13 — P137
PORT 14 — 4 — P140, P141, P146, P147

A/D CONVERTER — 8 — ANI0/P20 to ANI7/P27
A/D CONVERTER — 4 — ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120
A/D CONVERTER — AV_{REFP}/P20
A/D CONVERTER — AV_{REFM}/P21

KEY RETURN — 8 — KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL — $\overline{RESET}$
HIGH-SPEED ON-CHIP OSCILLATOR — X1/P121
— X2/EXCLK/P122
— XT1/P123
— XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
— RxD2/P14 (RxD2/P76)
— INTP0/P137
— 2 — INTP1/P50, INTP2/P51
— 2 — INTP3/P30, INTP4/P31
— INTP5/P16(INTP5/P12)
— 2 — INTP6/P140, INTP7/P141
— 2 — INTP8/P74, INTP9/P75
— 2 — INTP10/P76(INTP10/P52), INTP11/P77(INTP11/P53)

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 16[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)									
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)									
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		31 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		34 (N-ch O.D. I/O [V_{DD} withstand voltage]: 11)		38 (N-ch O.D. I/O [V_{DD} withstand voltage]: 13)		48 (N-ch O.D. I/O [V_{DD} withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	–		–		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3[Note2]), 8 channels (PWM outputs: 7[Note2][Note3])		5 channels (PWM outputs: 4[Note2]), 8 channels (PWM outputs: 7[Note2])[Note3]						8 channels (PWM outputs: 7[Note2])	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)									

Notes 1.   The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = E to G, J, L):   Start address FF300H
R5F100xE, R5F101xE (x = E to G, J, L):   Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L):   Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L):   Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**

Remarks 1. f$_{IL}$:   Low-speed on-chip oscillator clock frequency

2. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f$_{CLK}$: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T$_A$ = 25°C

Simplified I^{2}C mode connection diagram (during communication at different potential)
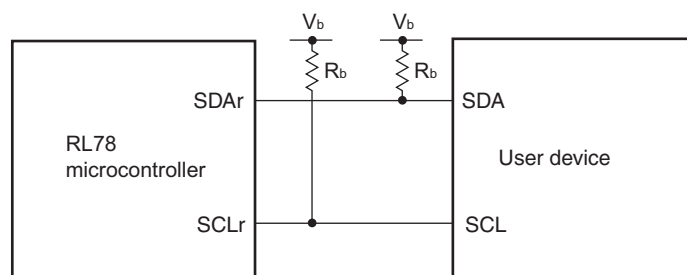
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
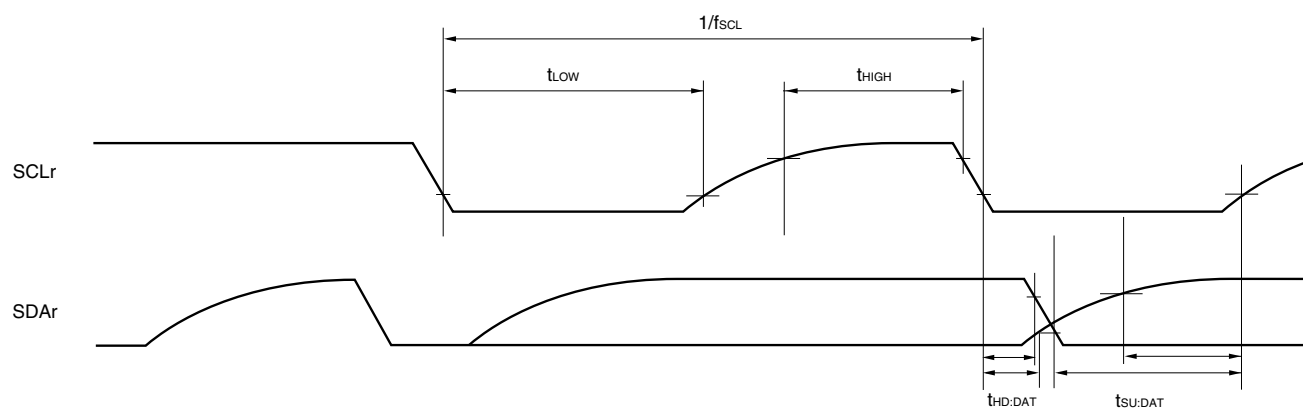
Remarks **1.** R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

    2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

    3. f$_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

    n: Channel number (mn = 00, 01, 02, 10, 12, 13)

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.54	2.90	mA
					V$_{DD}$ = 3.0 V		0.54	2.90	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	2.30	mA
					V$_{DD}$ = 3.0 V		0.44	2.30	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.40	1.70	mA
					V$_{DD}$ = 3.0 V		0.40	1.70	mA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.37	1.17	μA
					Resonator connection		0.56	1.36	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.53	1.97	μA
					Resonator connection		0.72	2.16	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		0.82	3.37	μA
					Resonator connection		1.01	3.56	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +105°C	Square wave input		3.01	15.37	μA
					Resonator connection		3.20	15.56	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	μA
			T$_A$ = +50°C				0.30	1.10	μA
			T$_A$ = +70°C				0.46	1.90	μA
			T$_A$ = +85°C				0.75	3.30	μA
			T$_A$ = +105°C				2.94	15.30	μA

(**Notes** and **Remarks** are listed on the next page.)

RENESAS

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
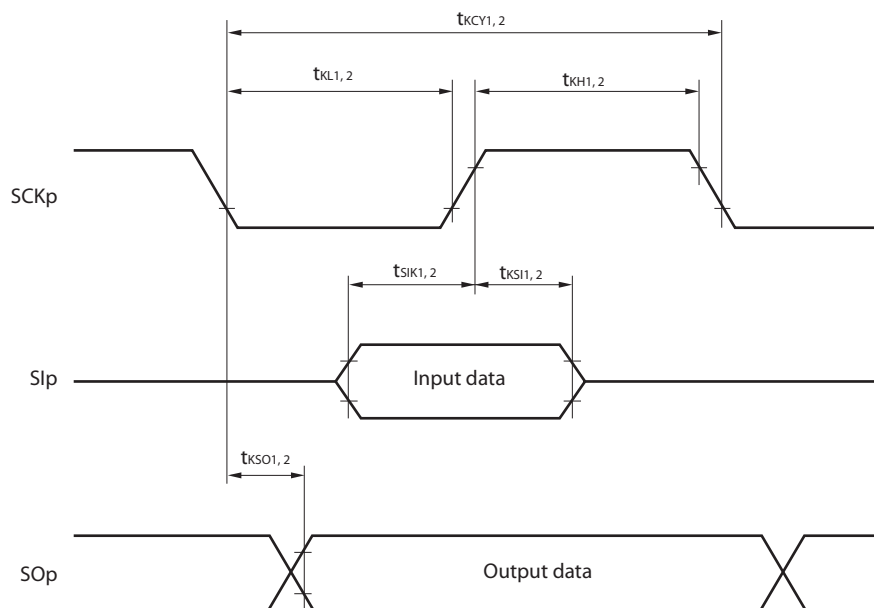
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
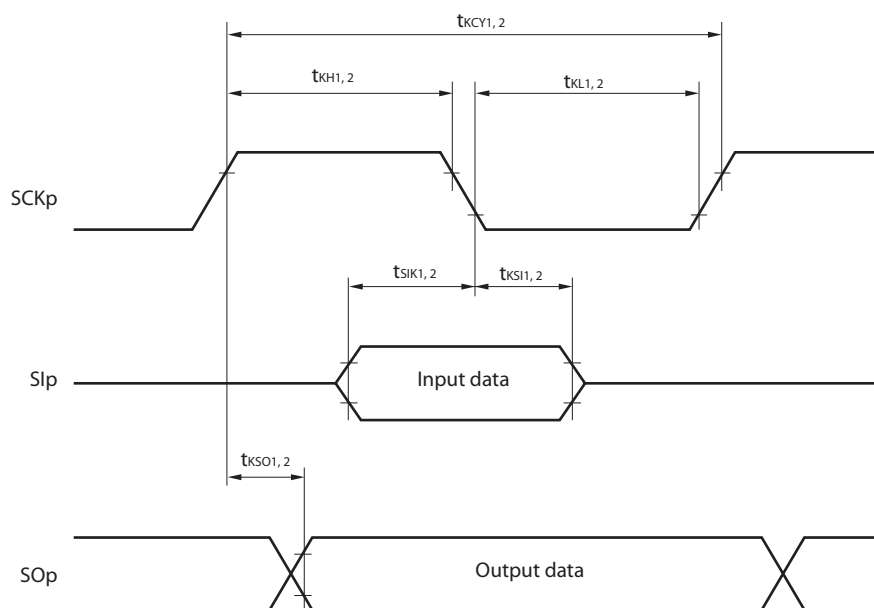
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(4) During communication at same potential (simplified I^{2}C mode)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 ^{Note1}	kHz
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		100 ^{Note1}	kHz
Hold time when SCLr = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 220 ^{Note2}		ns
		2.4 V ≤ EV$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 580 ^{Note2}		ns
Data hold time (transmission)	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

2. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Reception	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps
			2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps
			2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V			f_{MCK}/12 [Notes 1,2]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V $\leq$ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 24		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 36		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]		t$_{KCY2}$/2 − 100		ns
SIp setup time (to SCKp↑) [Note2]	t$_{SIK2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

3.6.5 Power supply voltage rising slope characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

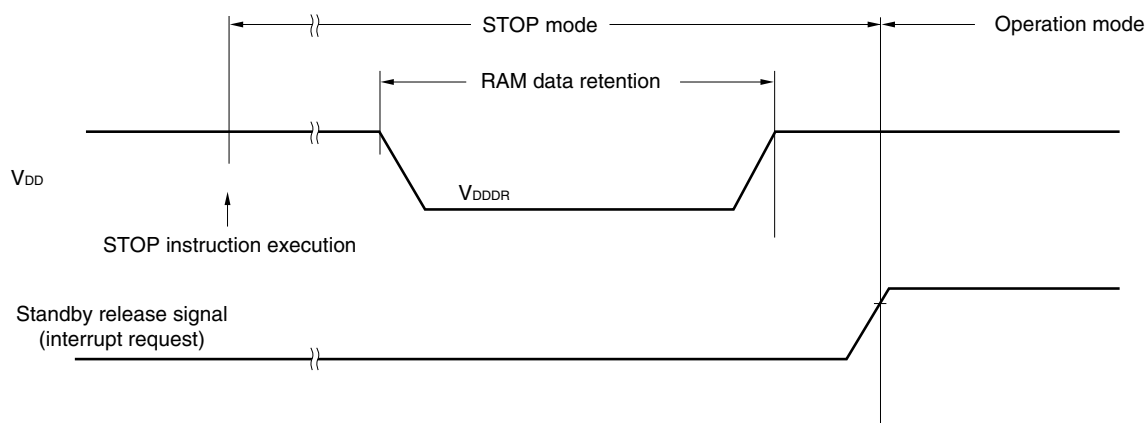| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution **Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

3.7 RAM Data Retention Characteristics

(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.44[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1,2,3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1,2,3		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.The retaining years are until next rewrite after the rewrite.
   2. When using flash memory programmer and Renesas Electronics self programming library.
   3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
   4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms
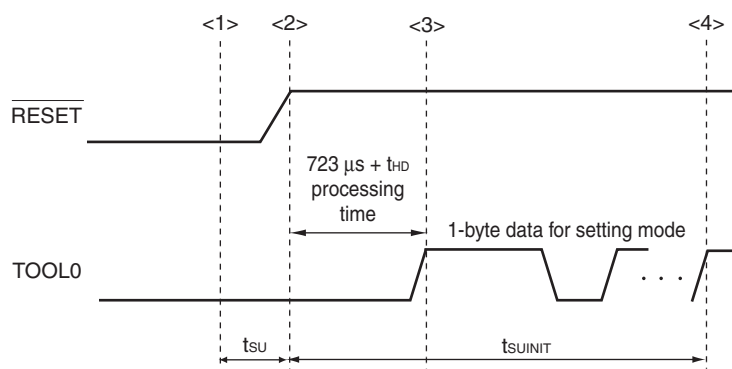
<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

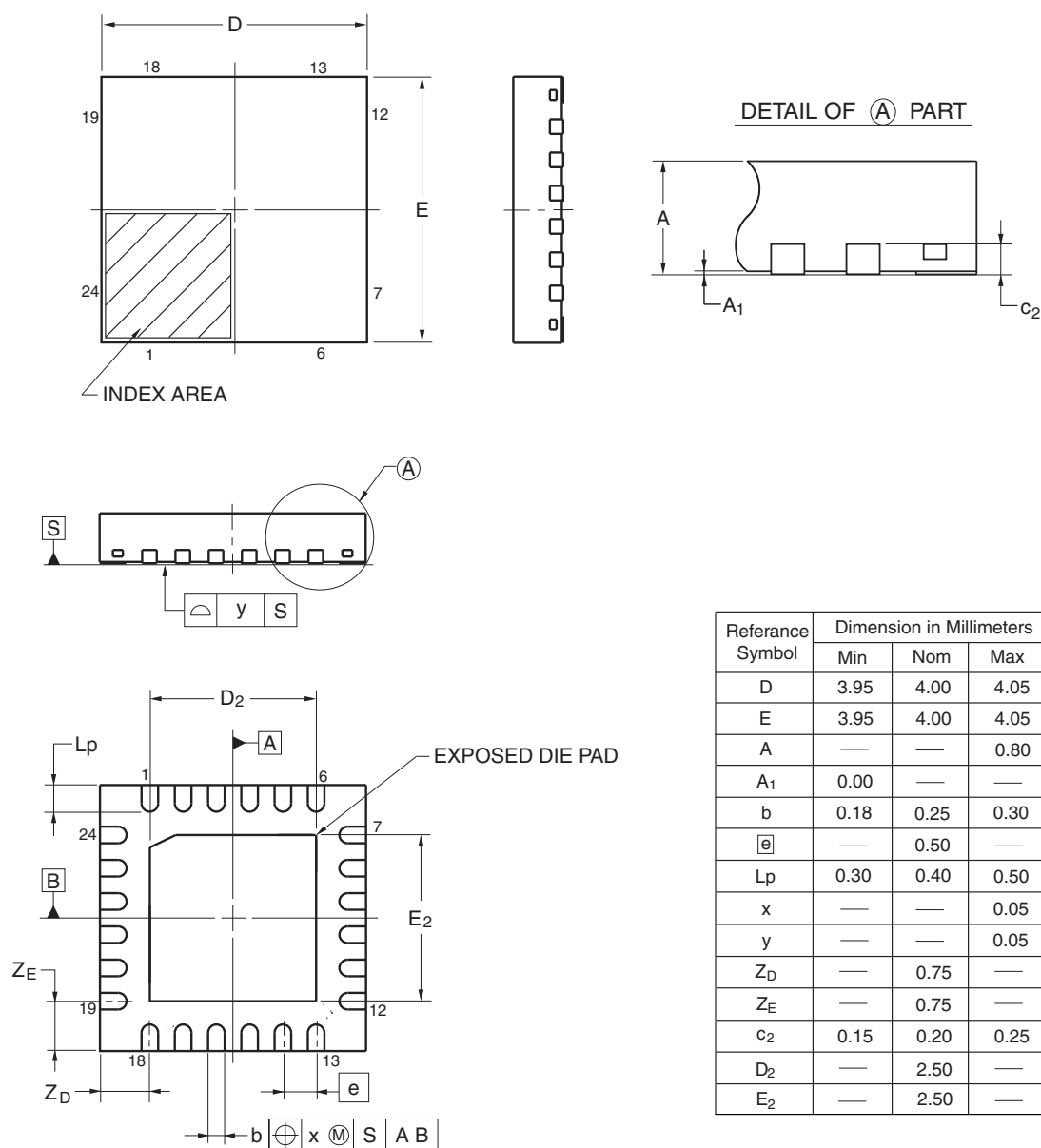t$_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.95	4.00	4.05
E	3.95	4.00	4.05
A	——	——	0.80
A_1	0.00	——	——
b	0.18	0.25	0.30
ⓔ	——	0.50	——
Lp	0.30	0.40	0.50
x	——	——	0.05
y	——	——	0.05
Z_D	——	0.75	——
Z_E	——	0.75	——
c_2	0.15	0.20	0.25
D_2	——	2.50	——
E_2	——	2.50	——

4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAFA,
R5F100LKAFA, R5F100LLAFA
R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAFA,
R5F101LKAFA, R5F101LLAFA
R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LGDFA, R5F100LHDFA, R5F100LJDFA,
R5F100LKDFA, R5F100LLDFA
R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LGDFA, R5F101LHDFA, R5F101LJDFA,
R5F101LKDFA, R5F101LLDFA
R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,
R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.65
x	0.13
y	0.10
ZD	1.125
ZE	1.125

NOTE
Each lead centerline is located within 0.13 mm of
its true position at maximum material condition.
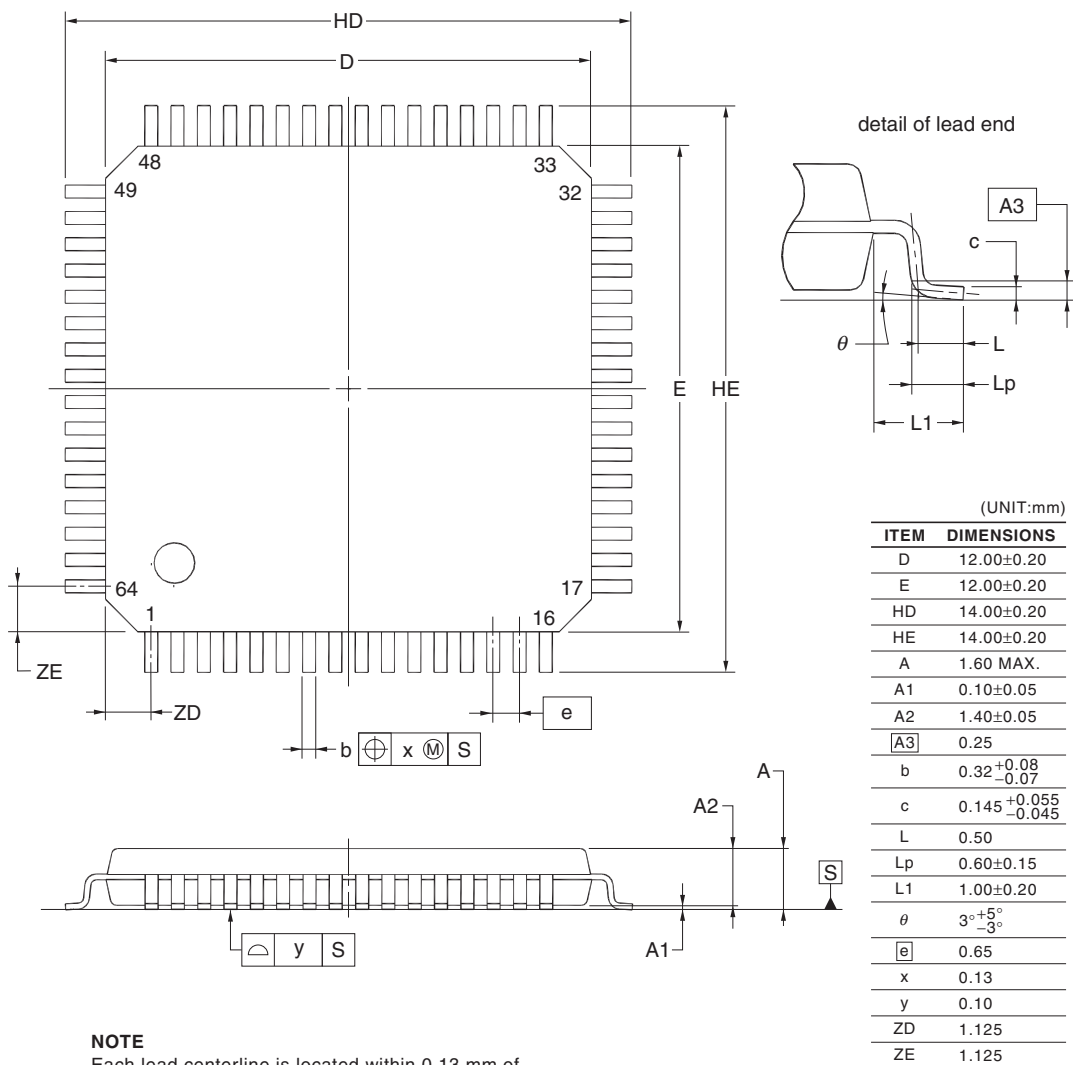
R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,
R5F100LJABG
R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,
R5F101LJABG
R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,
R5F100LJGBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03

INDEX MARK

INDEX MARK

	(UNIT:mm)
ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60