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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100gegfb-x0

Email: info@E-XFL.COM

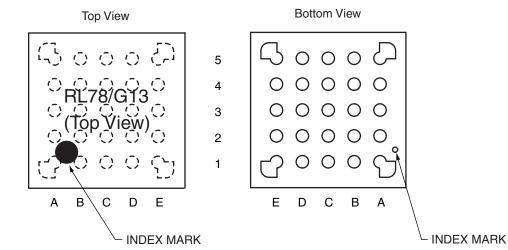
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

RL78/G13 1. OUTLINE

1.3.3 25-pin products

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• 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)



	Α	В	С	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AVREFM	P10/SCK00/ SCL00	4
3	P121/X1	V _{DD}	P20/ANI0/ AV _{REFP}	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	Vss	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	В	С	D	E	

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remark For pin identification, see **1.4 Pin Identification**.

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$ (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V _{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147		0.8EVDDO		EV _{DD0}	V
	V _{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55,	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	2.2		EV _{DD0}	V
			TTL input buffer $3.3 \text{ V} \le \text{EV}_{\text{DD0}} < 4.0 \text{ V}$	2.0		EV _{DD0}	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	1.5		EV _{DD0}	V
	V _{IH3}	P20 to P27, P150 to P156		0.7V _{DD}		V _{DD}	٧
	V _{IH4}	P60 to P63	0.7EV _{DD0}		6.0	٧	
	V _{IH5}	P121 to P124, P137, EXCLK, EXCL	KS, RESET	0.8V _{DD}		V _{DD}	٧
Input voltage, low	V _{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	,	0		0.2EV _{DD0}	V
	V _{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55,	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	0		0.8	V
		P80, P81, P142, P143	TTL input buffer 3.3 V ≤ EV _{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	0		0.32	V
	VIL3	P20 to P27, P150 to P156		0		0.3V _{DD}	٧
	V _{IL4}	P60 to P63		0		0.3EV _{DD0}	٧
	V _{IL5}	P121 to P124, P137, EXCLK, EXCL	KS, RESET	0		0.2V _{DD}	٧

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

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(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

 $(T_A = -40 \text{ to } +85^{\circ}\text{C}, 1.6 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$ Parameter Symbo Conditions HS (high-speed LS (low-speed main) LV (low-voltage main) Unit main) Mode ı Mode Mode MIN. MIN. MAX. MIN. MAX. MAX. Slp setup time tsik2 $2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}$ $1/f_{MCK}+2$ 1/fmck+30 1/fmck+30 ns (to SCKp↑) Note 1 n $1.8~V \leq EV_{DD0} \leq 5.5~V$ 1/fмск+3 1/fмск+30 1/fмcк+30 ns 0 $1.7~V \leq EV_{DD0} \leq 5.5~V$ 1/fмск+4 $1/f_{MCK}+40$ $1/f_{MCK}+40$ ns 0 1/fмск+40 1/fмск+40 $1.6~V \leq EV_{\text{DD0}} \leq 5.5~V$ ns Slp hold time tks12 $1.8~V \leq EV_{DD0} \leq 5.5~V$ 1/fмск+3 1/fмcк+31 1/fмcк+31 ns (from SCKp↑) 1 $1.7~V \leq EV_{DD0} \leq 5.5~V$ 1/fмcк+ 1/fмск+ 1/fмcк+ ns 250 250 250 $1.6~V \leq EV_{\text{DD0}} \leq 5.5~V$ 1/fmck+ 1/fмcк+ ns 250 250 2/f_{MCK+} 2/f_{MCK+} Delay time tks02 C = 30 $2.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$ 2/fmck+ ns pF Note 4 from SCKp↓ to 44 110 110 SOp output Note $2.4 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$ 2/fmck+ 2/fмcк+ 2/fmck+ ns 110 75 110 2/fмск+ $1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$ 2/fмск+ 2/fмск+ ns 110 110 110 $1.7 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$ 2/fmck+ 2/fmck+ 2/fмск+ ns 220 220 220 $1.6 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5$ 2/fмск+ 2/fмск+ ns

- **Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $SCKp\downarrow$ " when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - 4. C is the load capacitance of the SOp output lines.
 - 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

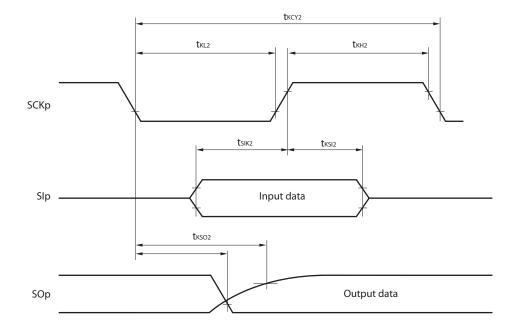
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- **Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 - 2. fmck: Serial array unit operation clock frequency

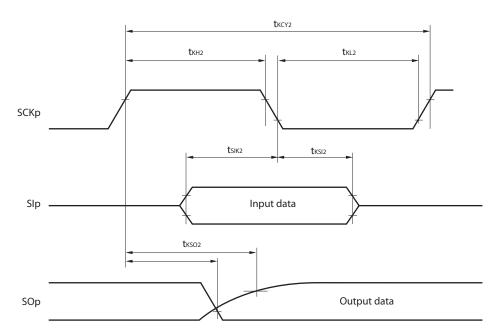
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

 n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)

(Ta = -40 to +85°C, 1.8 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Parameter	Symbol	Conditions	, -	h-speed Mode	,	v-speed Mode	,	-voltage Mode	Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fscL	$\begin{aligned} &4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ &2.7 \; V \leq V_b \leq 4.0 \; V, \\ &C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{aligned}$		1000 Note 1		300 Note 1		300 Note 1	kHz
		eq:second-seco		1000 Note 1		300 Note 1		300 Note 1	kHz
		$ \begin{aligned} &4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ &2.7 \; V \leq V_b \leq 4.0 \; V, \\ &C_b = 100 \; pF, \; R_b = 2.8 \; k\Omega \end{aligned} $		400 Note 1		300 Note 1		300 Note 1	kHz
		$\label{eq:section} \begin{split} 2.7 \ V & \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V & \leq V_b \leq 2.7 \ V, \\ C_b & = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{split}$		400 Note 1		300 Note 1		300 ote 1	kHz
		$\begin{split} &1.8~V \leq EV_{DD0} < 3.3~V,\\ &1.6~V \leq V_b \leq 2.0~V^{\text{Note 2}},\\ &C_b = 100~pF,~R_b = 5.5~k\Omega \end{split}$		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	tLOW	$ \begin{aligned} &4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ &2.7 \; V \leq V_b \leq 4.0 \; V, \\ &C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{aligned} $	475		1550		1550		ns
		eq:second-seco	475		1550		1550		ns
		$ \begin{aligned} &4.0 \; V \leq EV_{DD0} \leq 5.5 \; V, \\ &2.7 \; V \leq V_b \leq 4.0 \; V, \\ &C_b = 100 \; pF, \; R_b = 2.8 \; k\Omega \end{aligned} $	1150		1550		1550		ns
		$\label{eq:section} \begin{split} 2.7 \ V & \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V & \leq V_b \leq 2.7 \ V, \\ C_b & = 100 \ pF, \ R_b = 2.7 \ k\Omega \end{split}$	1150		1550		1550		ns
		$\begin{split} &1.8~V \leq EV_{DD0} < 3.3~V,\\ &1.6~V \leq V_b \leq 2.0~V^{\text{Note 2}},\\ &C_b = 100~pF,~R_b = 5.5~k\Omega \end{split}$	1550		1550		1550		ns
Hold time when SCLr = "H"	tнівн	$ 4.0 \ V \le EV_{DD0} \le 5.5 \ V, $ $ 2.7 \ V \le V_b \le 4.0 \ V, $ $ C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega $	245		610		610		ns
		$2.7 \ V \le EV_{DD0} < 4.0 \ V,$ $2.3 \ V \le V_b \le 2.7 \ V,$ $C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega$	200		610		610		ns
		$ \begin{aligned} & 4.0 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V}, \\ & 2.7 \text{ V} \leq \text{V}_{\text{b}} \leq 4.0 \text{ V}, \\ & C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 2.8 \text{ k}\Omega \end{aligned} $	675		610		610		ns
		$ 2.7 \text{ V} \leq \text{EV}_{\text{DDO}} < 4.0 \text{ V}, \\ 2.3 \text{ V} \leq \text{V}_{\text{b}} \leq 2.7 \text{ V}, \\ C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 2.7 \text{ k}\Omega $	600		610		610		ns
		$\begin{split} &1.8~V \leq EV_{DDO} < 3.3~V,\\ &1.6~V \leq V_b \leq 2.0~V^{\text{Note 2}},\\ &C_b = 100~pF,~R_b = 5.5~k\Omega \end{split}$	610		610		610		ns

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

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2. The maximum value (MAX.) of thd:DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IoH1, IoL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b = 400 \text{ pF}, R_b = 2.7 \text{ k}\Omega$



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

		Reference Voltage					
	Reference voltage (+) = AVREFP	Reference voltage (+) = VDD	Reference voltage (+) = VBGR				
Input channel	Reference voltage (–) = AVREFM	Reference voltage (-) = Vss	Reference voltage (–) = AVREFM				
ANI0 to ANI14	Refer to 2.6.1 (1) .	Refer to 2.6.1 (3) .	Refer to 2.6.1 (4) .				
ANI16 to ANI26	Refer to 2.6.1 (2) .						
Internal reference voltage	Refer to 2.6.1 (1) .		_				
Temperature sensor output							
voltage							

(1) When reference voltage (+)= AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V \leq AVREFP \leq VDD \leq 5.5 V, Vss = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Con	ditions	MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	1.8 V ≤ AV _{REFP} ≤ 5.5 V		1.2	±3.5	LSB
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{REFP} \leq 5.5~V^{\text{Note 4}}$		1.2	±7.0	LSB
Conversion time	tconv	10-bit resolution	$3.6~V \leq V_{DD} \leq 5.5~V$	2.125		39	μS
		Target pin: ANI2 to	$2.7~V \leq V_{DD} \leq 5.5~V$	3.1875		39	μS
		ANI14	$1.8~V \leq V_{DD} \leq 5.5~V$	17		39	μS
			$1.6~V \leq V_{DD} \leq 5.5~V$	57		95	μS
		10-bit resolution	$3.6~V \leq V_{DD} \leq 5.5~V$	2.375		39	μS
		Target pin: Internal	$2.7~V \leq V_{DD} \leq 5.5~V$	3.5625		39	μS
		reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$2.4~V \leq V_{DD} \leq 5.5~V$	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	10-bit resolution	1.8 V ≤ AV _{REFP} ≤ 5.5 V			±0.25	%FSR
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{\text{REFP}} \leq 5.5~V^{\text{Note 4}}$			±0.50	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution	$1.8~V \leq AV_{REFP} \leq 5.5~V$			±0.25	%FSR
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{REFP} \leq 5.5~V^{\text{Note 4}}$			±0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$1.8~V \leq AV_{REFP} \leq 5.5~V$			±2.5	LSB
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{\text{REFP}} \leq 5.5~V^{\text{Note 4}}$			±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$1.8~V \leq AV_{REFP} \leq 5.5~V$			±1.5	LSB
		$AV_{REFP} = V_{DD}^{Note 3}$	$1.6~V \leq AV_{\text{REFP}} \leq 5.5~V^{\text{Note 4}}$			±2.0	LSB
Analog input voltage	VAIN	ANI2 to ANI14		0		AVREFP	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{BGR} Note 5		V
		Temperature sensor outp (2.4 V \leq VDD \leq 5.5 V, HS	•	\	/TMPS25 Note	5	V

(Notes are listed on the next page.)



2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(Ta = -40 to +85°C, VPDR \leq VDD \leq 5.5 V, Vss = 0 V)

	Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection	Supply voltage level	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V
voltage			Power supply fall time	3.90	3.98	4.06	V
		V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V LVD7	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum p	ulse width	tLW		300			μS
Detection d	elay time					300	μS

- Notes 1. Total current flowing into V_{DD} and EV_{DDO}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DDO} or Vss, EVsso. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. During HALT instruction execution by flash memory.
 - 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 4. When high-speed system clock and subsystem clock are stopped.
 - **5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7~V \le V_{DD} \le 5.5~V @ 1~MHz$ to 32~MHz $2.4~V \le V_{DD} \le 5.5~V @ 1~MHz$ to 16~MHz

- **8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - **4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (Ta = -40 to $+105^{\circ}$ C, 2.4 V \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 V, Vss = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply	I _{DD2}	HALT	HS (high-	fih = 32 MHz Note 4	V _{DD} = 5.0 V		0.62	3.40	mA
Current Note 1	Note 2	mode	speed main) mode Note 7		V _{DD} = 3.0 V		0.62	3.40	mA
			mode	fin = 24 MHz Note 4	V _{DD} = 5.0 V		0.50	2.70	mA
					V _{DD} = 3.0 V		0.50	2.70	mA
				fin = 16 MHz Note 4	V _{DD} = 5.0 V		0.44	1.90	mA
					V _{DD} = 3.0 V		0.44	1.90	mA
			HS (high-	$f_{MX} = 20 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.31	2.10	mA
			speed main) mode Note 7	V _{DD} = 5.0 V	Resonator connection		0.48	2.20	mA
				$f_{MX} = 20 \text{ MHz}^{\text{Note 3}},$	Square wave input		0.31	2.10	mA
				V _{DD} = 3.0 V	Resonator connection		0.48	2.20	mA
				$f_{MX} = 10 \text{ MHz}^{Note 3},$	Square wave input		0.21	1.10	mA
				V _{DD} = 5.0 V	Resonator connection		0.28	1.20	mA
				$f_{MX} = 10 \text{ MHz}^{Note 3},$	Square wave input		0.21	1.10	mA
				V _{DD} = 3.0 V	Resonator connection		0.28	1.20	mA
			Subsystem	fsub = 32.768 kHz ^{Note 5}	Square wave input		0.28	0.61	μΑ
			clock operation	T _A = -40°C	Resonator connection		0.47	0.80	μΑ
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.34	0.61	μΑ
				T _A = +25°C	Resonator connection		0.53	0.80	μΑ
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.41	2.30	μΑ
				T _A = +50°C	Resonator connection		0.60	2.49	μΑ
				fsub = 32.768 kHz ^{Note 5}	Square wave input		0.64	4.03	μΑ
				T _A = +70°C	Resonator connection		0.83	4.22	μΑ
				fsub = 32.768 kHz ^{Note 5}	Square wave input		1.09	8.04	μΑ
				T _A = +85°C	Resonator connection		1.28	8.23	μΑ
				fsub = 32.768 kHz ^{Note 5}	Square wave input		5.50	41.00	μΑ
				T _A = +105°C	Resonator connection		5.50	41.00	μΑ
	IDD3 ^{Note 6} ST	STOP	T _A = -40°C				0.19	0.52	μΑ
		mode ^{Note 8}	T _A = +25°C				0.25	0.52	μΑ
			T _A = +50°C				0.32	2.21	μΑ
			T _A = +70°C				0.55	3.94	μΑ
			T _A = +85°C				1.00	7.95	μΑ
			T _A = +105°C				5.00	40.00	μΑ

(Notes and Remarks are listed on the next page.)

- Notes 1. Total current flowing into VDD, EVDDO, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDO, and EVDD1, or Vss, EVSSO, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. During HALT instruction execution by flash memory.
 - 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 4. When high-speed system clock and subsystem clock are stopped.
 - **5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 32 MHz $2.4 \text{ V} \le \text{V}_{DD} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 16 MHz

- 8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - 3. fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - **4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^{\circ}C$

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

 $(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{Vss} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Parameter	Symbol		Condit	ions	HS (high-spee	ed main) Mode	Unit
					MIN.	MAX.	
Transfer rate		Transmission	$4.0 V \leq EV_{DD0} \leq 5.5$			Note 1	bps
			$V,$ $2.7~V \leq V_b \leq 4.0~V$	Theoretical value of the maximum transfer rate $C_b = 50 \ pF, \ R_b = 1.4 \ k\Omega, \ V_b = 2.7 \ V$		2.6 Note 2	Mbps
			$2.7 \text{ V} \leq \text{EV}_{\text{DD0}} < 4.0$			Note 3	bps
			$V,$ $2.3~V \leq V_b \leq 2.7~V$	Theoretical value of the maximum transfer rate $C_b = 50 \ pF, \ R_b = 2.7 \ k\Omega, \ V_b = 2.3 \ V$		1.2 Note 4	Mbps
			2.4 V ≤ EV _{DD0} < 3.3			Note 5	bps
			$V,$ $1.6~V \leq V_b \leq 2.0~V$	Theoretical value of the maximum transfer rate $C_b = 50 \text{ pF}, R_b = 5.5 \text{ k}\Omega, V_b = 1.6 V$		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V \leq EV_{DD0} \leq 5.5 V and 2.7 V \leq V_b \leq 4.0 V

Maximum transfer rate =
$$\frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3}$$
 [bps]

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln{(1 - \frac{2.2}{V_b})}\}}{\frac{1}{(\text{Transfer rate})} \times \text{Number of transferred bits}} \times 100 \, [\%]$$

- * This value is the theoretical value of the relative difference between the transmission and reception sides.
- 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- 3. The smaller maximum transfer rate derived by using fmck/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V \leq EV_{DDO} < 4.0 V and 2.4 V \leq V_b \leq 2.7 V

Maximum transfer rate =
$$\frac{1}{\{-C_b \times R_b \times ln (1 - \frac{2.0}{V_b})\} \times 3}$$
 [bps]

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln{(1 - \frac{2.0}{V_b})}\}}{\frac{1}{(\text{Transfer rate})} \times \text{Number of transferred bits}} \times 100 \, [\%]$$

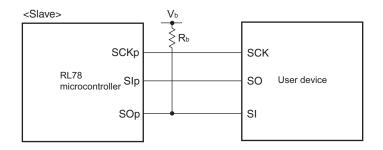
- * This value is the theoretical value of the relative difference between the transmission and reception sides.
- **4.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.



- Notes 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps
 - 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 - **4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (VDD tolerance (for the 20- to 52-pin products)/EVDD tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VH and VIL, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)



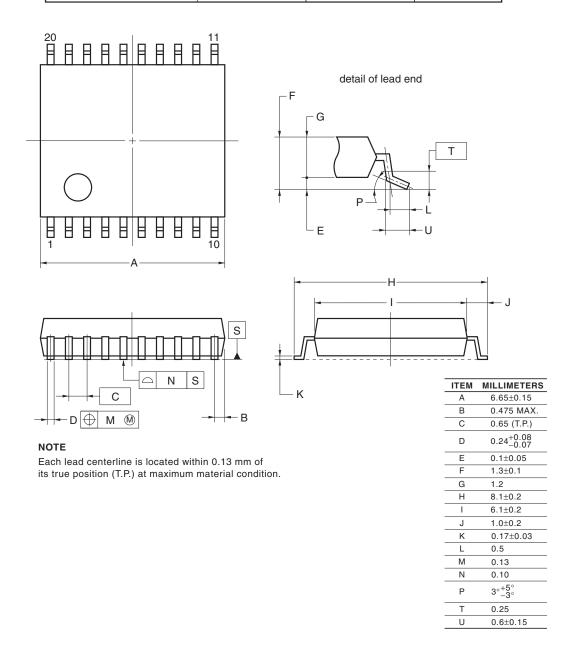
- **Remarks 1.** $R_b[\Omega]$:Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
 - 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02,
 - 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 - 3. fmck: Serial array unit operation clock frequency(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 - **4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12

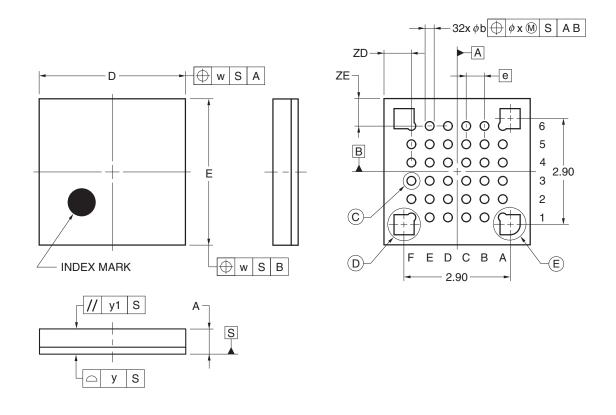


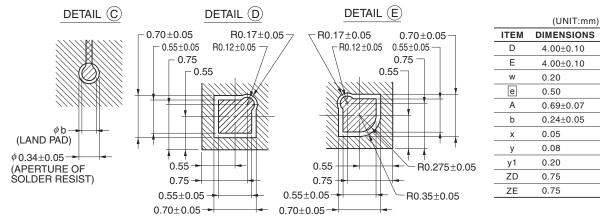
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4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023





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R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GHANA, R5F100GHANA, R5F100GKANA, R5F100GKANA, R5F100GKANA, R5F100GKANA

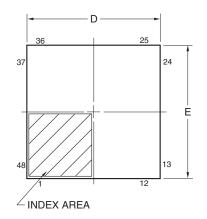
R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GHANA, R5F101GHANA, R5F101GHANA, R5F101GKANA, R5F101GKANA, R5F101GLANA

R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GDNA, R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA

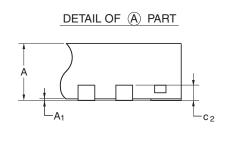
R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA, R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA

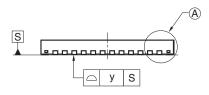
R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GHGNA, R5F100GJGNA

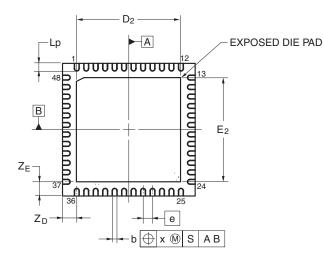
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13











Referance	Dimension in Millimeters			
Symbol	Min	Nom	Max	
D	6.95	7.00	7.05	
Е	6.95	7.00	7.05	
Α			0.80	
A ₁	0.00		_	
b	0.18	0.25	0.30	
е		0.50	_	
Lp	0.30	0.40	0.50	
Х			0.05	
у			0.05	
Z _D		0.75		
Z _E		0.75		
C ₂	0.15	0.20	0.25	
D ₂		5.50	_	
E ₂		5.50	_	

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4.10 52-pin Products

R5F100JCAFA, R5F100JDAFA, R5F100JEAFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJAFA, R5F100JKAFA, R5F100JLAFA

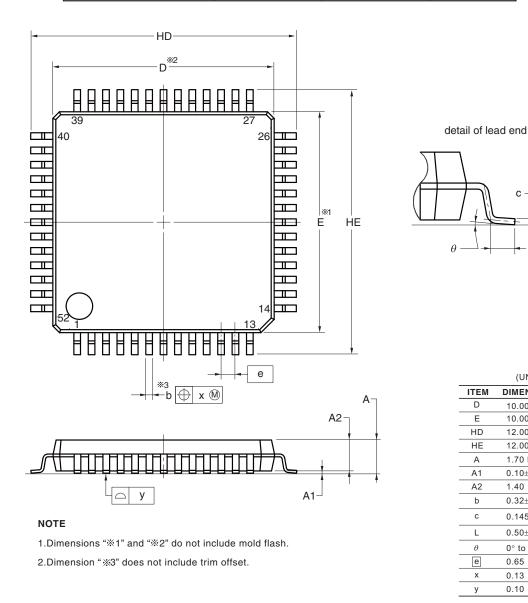
R5F101JCAFA, R5F101JDAFA, R5F101JEAFA, R5F101JFAFA, R5F101JJAFA, R5F101JJAFA, R5F101JJAFA, R5F101JAFA, R5F101JKAFA, R5F101JLAFA

R5F100JCDFA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JDFA, R5F100JPA, R R5F100JKDFA, R5F100JLDFA

R5F101JCDFA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JDFA, R5 R5F101JKDFA, R5F101JLDFA

R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



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(UNIT:mm)

DIMENSIONS

10.00±0.10

10.00±0.10

12.00±0.20

12.00±0.20 1.70 MAX.

 0.10 ± 0.05 1.40

0.32±0.05

 $0.50 {\pm} 0.15$

 0° to 8° 0.65

0.13 0.10

0.145±0.055

		Description	
Rev.	Date	Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I ² C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I ² C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		109	Addition of (1) I ² C standard mode
		111	Addition of (2) I ² C fast mode
		112	Addition of (3) I ² C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)

NOTES FOR CMOS DEVICES

- (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) INPUT OF SIGNAL DURING POWER OFF STATE: Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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