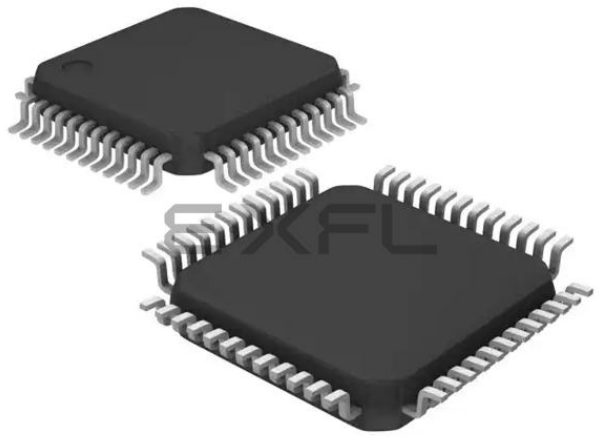
Renesas Electronics America Inc - R5F100GGDFB#50 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ggdfb-50

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0
			G	R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0
			D	R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0
			G	R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	A	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0
			D	R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
			D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
		Not mounted	A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

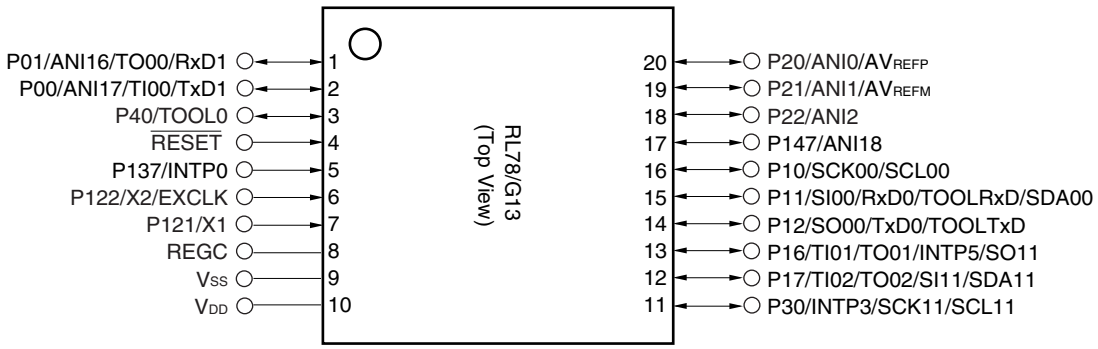
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark For pin identification, see **1.4 Pin Identification**.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	EV_{DD0} = EV_{DD1}	−0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	EV_{SS0} = EV_{SS1}	−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P156	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	−0.3 to EV_{DD0} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V
	V_{AI2}	ANI0 to ANI14	−0.3 to V_{DD} +0.3 and −0.3 to AV_{REF}(+) +0.3 Notes 2, 3	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF}(+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF}(+) : + side reference voltage of the A/D converter.

3. V_{SS} : Reference voltage

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.3		mA
						V_{DD} = 3.0 V		2.3		mA
					Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.1	6.6	mA
						V_{DD} = 3.0 V		4.1	6.6	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.0	4.7	mA
						V_{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	2.1	mA
						V_{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.3	1.8	mA
						V_{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

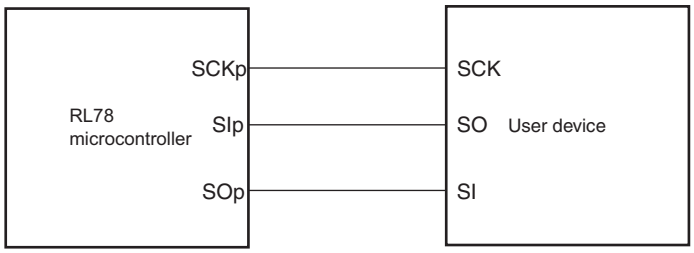
(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

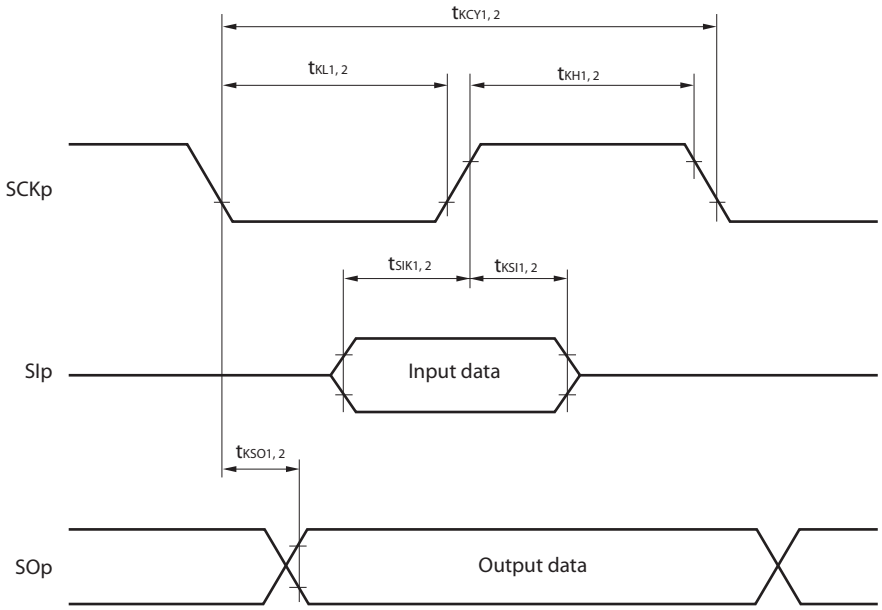
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

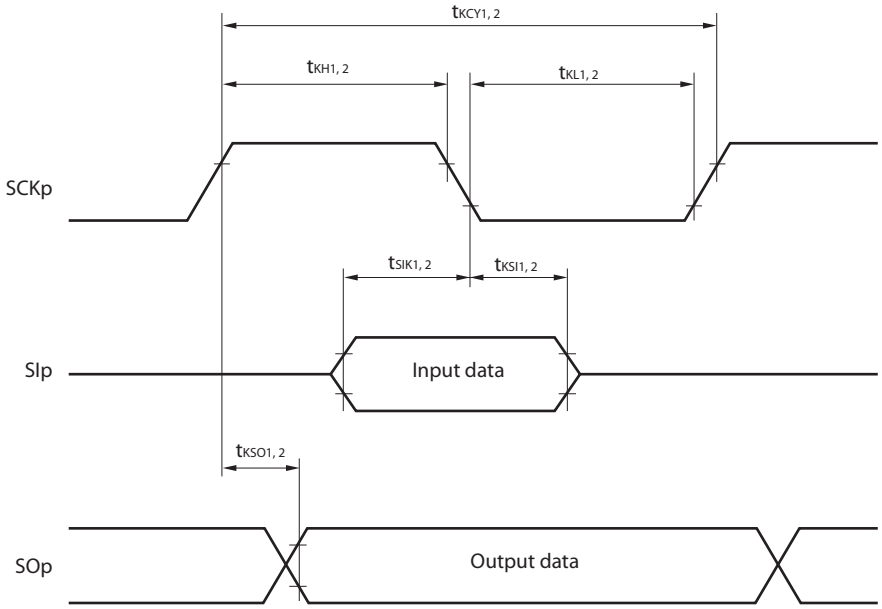
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with $EV_{DD0} \geq V_b$.

6. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

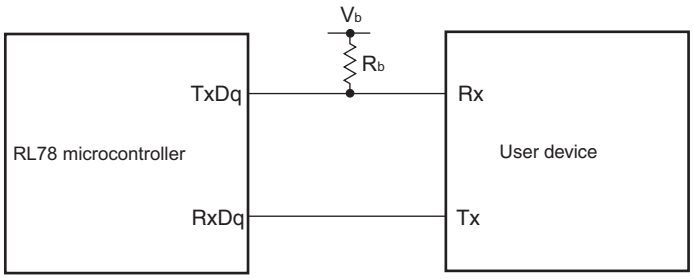
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

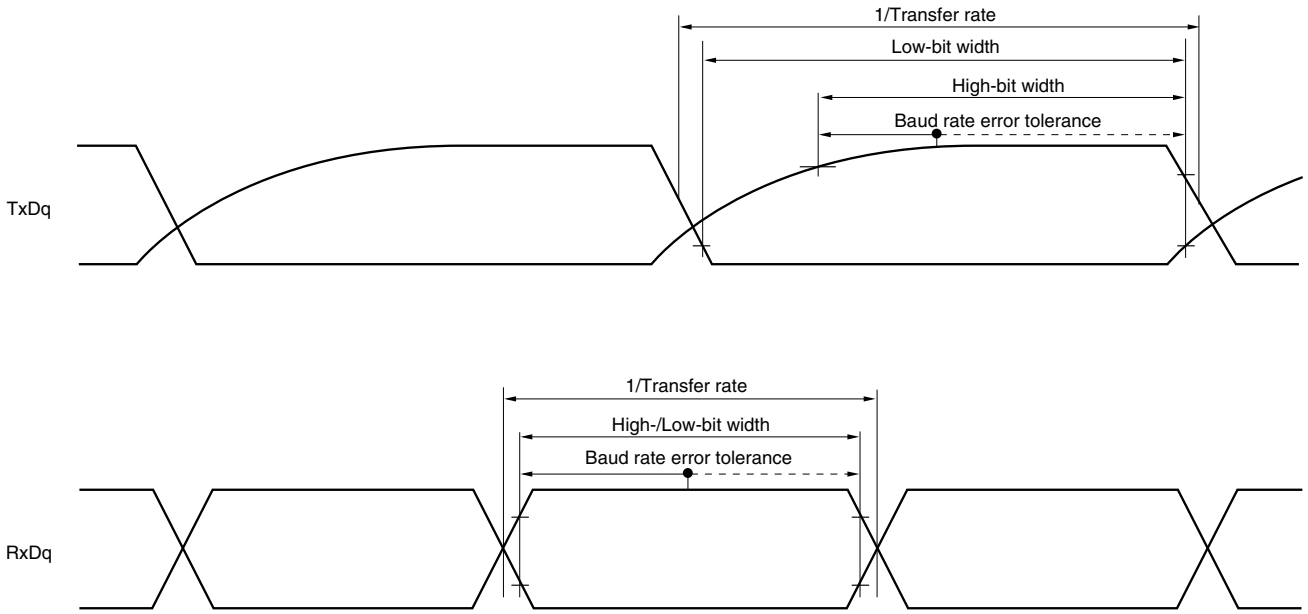
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 1	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	24 MHz < f_{MCK}	14/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	12/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 20 MHz	10/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	48/f_{MCK}		—		—		ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}		—		—		ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}		—		—		ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}		—		—		ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}		16/f_{MCK}		—		ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}		10/f_{MCK}		10/f_{MCK}		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	t_{KCY2}/2 – 12		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 – 18		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		t_{KCY2}/2 – 50		ns
SIp setup time (to SCKp↑) Note 3	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) Note 4	t_{KSI2}		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output Note 5	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with $EV_{DD0} \geq V_b$.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

(2) I^2C fast mode

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: f_{CLK} ≥ 3.5 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR} Note 3, Reference voltage (–) = AV_{REFM} = 0 V Note 4, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} Note 3	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		16/f_{MCK}		ns
				12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 14		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 16		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+40		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+66	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+113	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

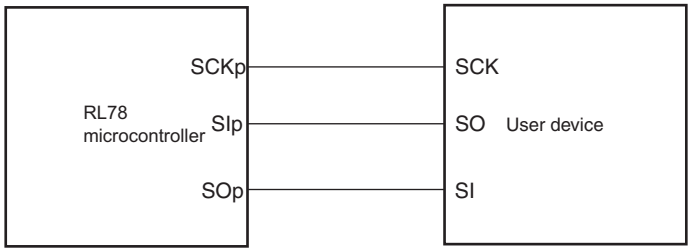
Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)



(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note1	kHz
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note2		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

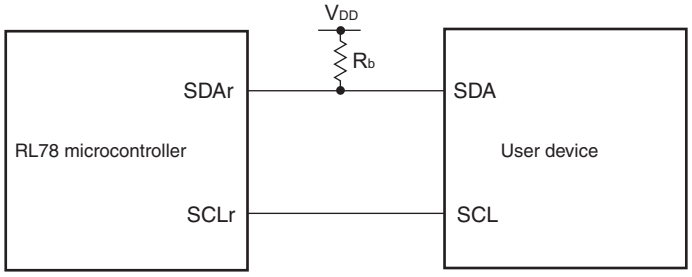
Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

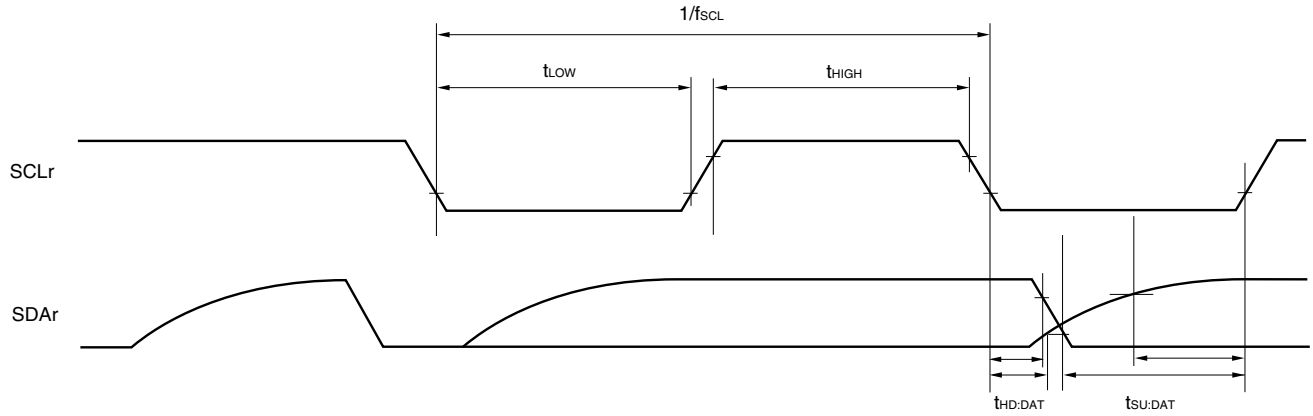
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

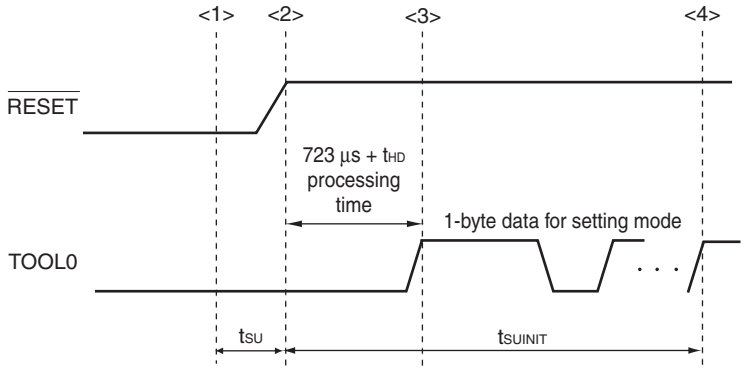
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = “L”	t_{LOW}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	4600		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	4650		ns
Hold time when SCLr = “H”	t_{HIGH}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	620		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	500		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	2700		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1830		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

3.10 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)