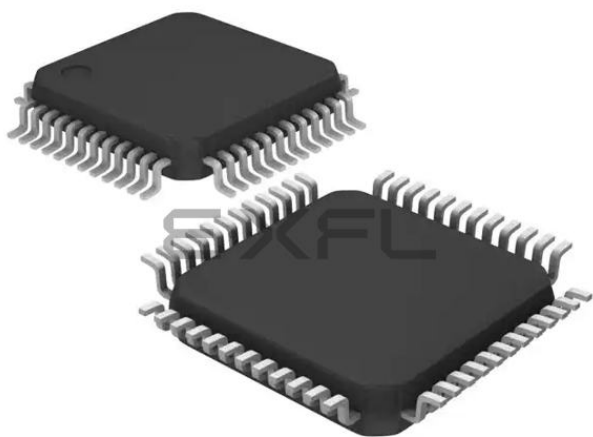




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ghafb-30

Table 1-1. List of Ordering Part Numbers

(2/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	Mounted	A G	R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0 R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0 R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0 R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0
		Not mounted	A	R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0 R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A D G	R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0 R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0 R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDSP#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0 R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDSP#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0 R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0, R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0 R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0, R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0
		Not mounted	A D	R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0 R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0 R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDSP#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0 R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDSP#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	Mounted	A D G	R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0 R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0 R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0 R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0 R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0 R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0
		Not mounted	A D	R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0 R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0 R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0 R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

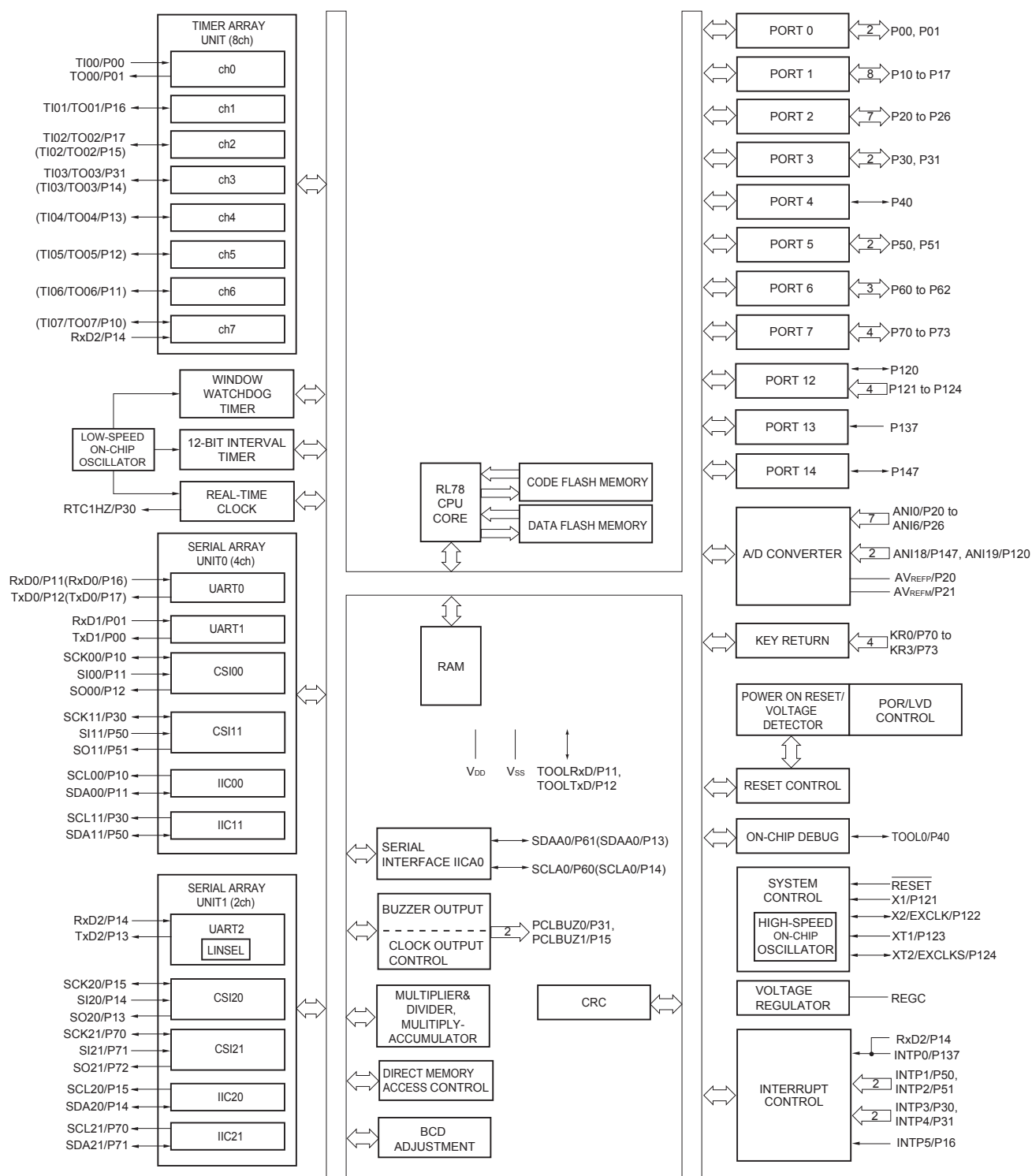
(10/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGFAFA#V0, R5F100MHAFA#V0, R5F100MJFAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGFAFA#X0, R5F100MHAFA#X0, R5F100MJFAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0
			D	R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0
			G	R5F100MFGFA#V0, R5F100MGGFA#V0, R5F100MHGFA#V0, R5F100MJGFA#V0 R5F100MFGFA#X0, R5F100MGGFA#X0, R5F100MHGFA#X0, R5F100MJGFA#X0
		Not mounted	A	R5F101MFAFA#V0, R5F101MGFAFA#V0, R5F101MHAFA#V0, R5F101MJFAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGFAFA#X0, R5F101MHAFA#X0, R5F101MJFAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0
			D	R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0
			G	R5F101MFGFA#V0, R5F101MGGFA#V0, R5F101MHGFA#V0, R5F101MJGFA#V0 R5F101MFGFA#X0, R5F101MGGFA#X0, R5F101MHGFA#X0, R5F101MJGFA#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0
			D	R5F100MFDDB#V0, R5F100MGDFB#V0, R5F100MHDDB#V0, R5F100MJDFB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDDB#X0, R5F100MGDFB#X0, R5F100MHDDB#X0, R5F100MJDFB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0
			G	R5F100MFGFB#V0, R5F100MGGFB#V0, R5F100MHGFB#V0, R5F100MJGFB#V0 R5F100MFGFB#X0, R5F100MGGFB#X0, R5F100MHGFB#X0, R5F100MJGFB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0
			D	R5F101MFDDB#V0, R5F101MGDFB#V0, R5F101MHDDB#V0, R5F101MJDFB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDDB#X0, R5F101MGDFB#X0, R5F101MHDDB#X0, R5F101MJDFB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0
			G	R5F101MFGFB#V0, R5F101MGGFB#V0, R5F101MHGFB#V0, R5F101MJGFB#V0 R5F101MFGFB#X0, R5F101MGGFB#X0, R5F101MHGFB#X0, R5F101MJGFB#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

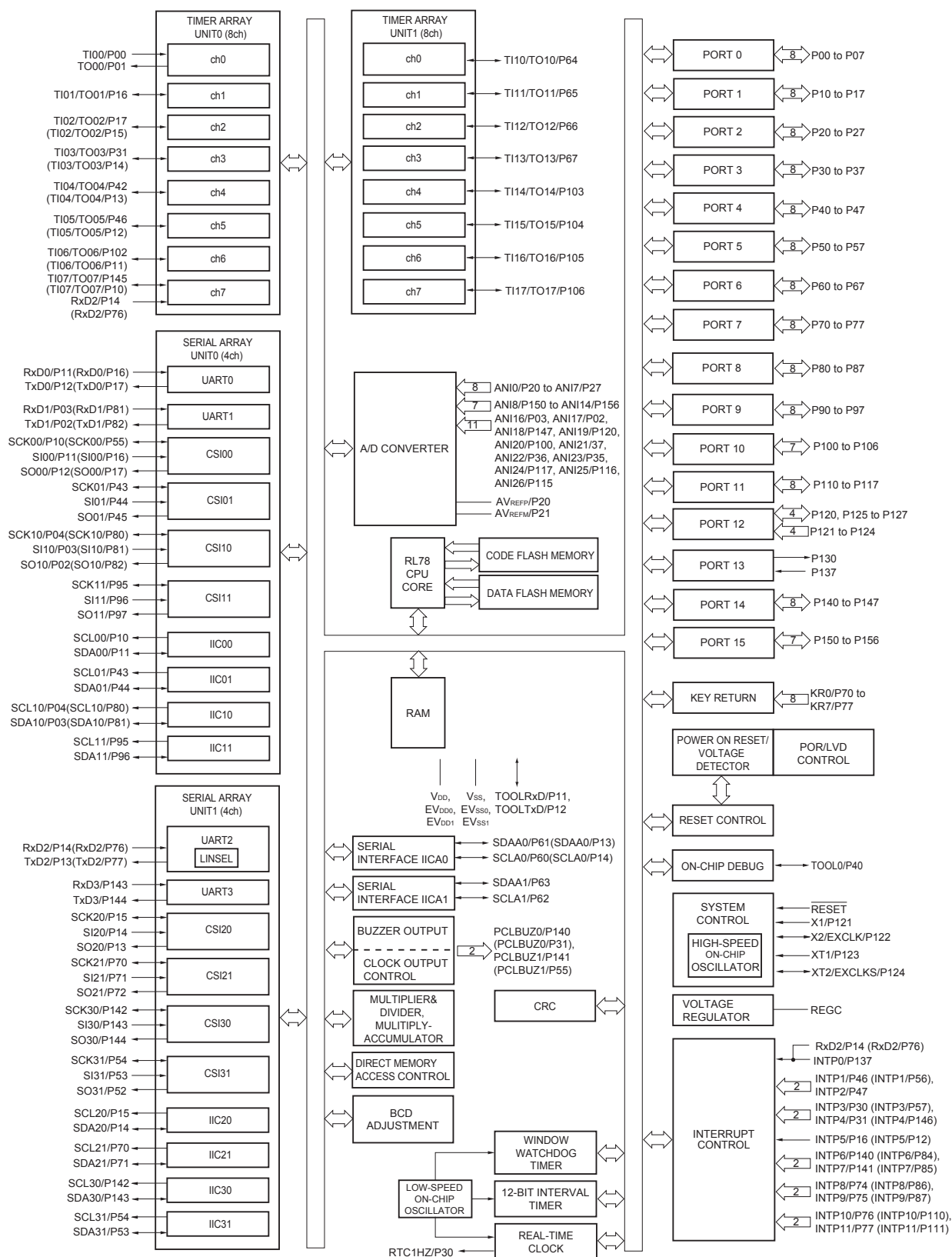
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.5.7 40-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f _x) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V _{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f _x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85 °C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.0		+1.0	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.0		+5.0	%
		-40 to -20 °C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high ^{Note 1}	I _{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-10.0 ^{Note 2}	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-55.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-10.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-5.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		-80.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		-19.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		-10.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		-5.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ EV _{DD0} ≤ 5.5 V		-135.0 ^{Note 4}	mA
	I _{OH2}	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V		-0.1 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		-1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is -100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V) (5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{DD0}		1	μA		
	I _{LIH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}		1	μA		
	I _{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0}		−1	μA		
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R _U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3		mA
						V _{DD} = 3.0 V		2.3		mA
					Normal operation	V _{DD} = 5.0 V		5.2	8.5	mA
						V _{DD} = 3.0 V		5.2	8.5	mA
				f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.1	6.6	mA
						V _{DD} = 3.0 V		4.1	6.6	mA
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	4.7	mA
						V _{DD} = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	2.1	mA
						V _{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	1.8	mA
						V _{DD} = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.62	1.86	mA	
					V _{DD} = 3.0 V		0.62	1.86	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.50	1.45	mA	
					V _{DD} = 3.0 V		0.50	1.45	mA	
					f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.11	mA
						V _{DD} = 3.0 V		0.44	1.11	mA
				LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		290	620	μA
						V _{DD} = 2.0 V		290	620	μA
				LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		440	680	μA
						V _{DD} = 2.0 V		440	680	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	1.08	mA	
					Resonator connection		0.48	1.28	mA	
					f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.21	0.63	mA	
					Resonator connection		0.28	0.71	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.21	0.63	mA	
					Resonator connection		0.28	0.71	mA	
				LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		110	360	μA
						Resonator connection		160	420	μA
					f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		110	360	μA
						Resonator connection		160	420	μA
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.28	0.61	μA	
					Resonator connection		0.47	0.80	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.34	0.61	μA	
					Resonator connection		0.53	0.80	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.41	2.30	μA	
					Resonator connection		0.60	2.49	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.64	4.03	μA	
					Resonator connection		0.83	4.22	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		1.09	8.04	μA	
					Resonator connection		1.28	8.23	μA	
	I _{DD3} Note 6	STOP mode Note 8	T _A = −40°C					0.19	0.52	μA
			T _A = +25°C					0.25	0.52	μA
			T _A = +50°C					0.32	2.21	μA
			T _A = +70°C					0.55	3.94	μA
			T _A = +85°C					1.00	7.95	μA

(Notes and Remarks are listed on the next page.)

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

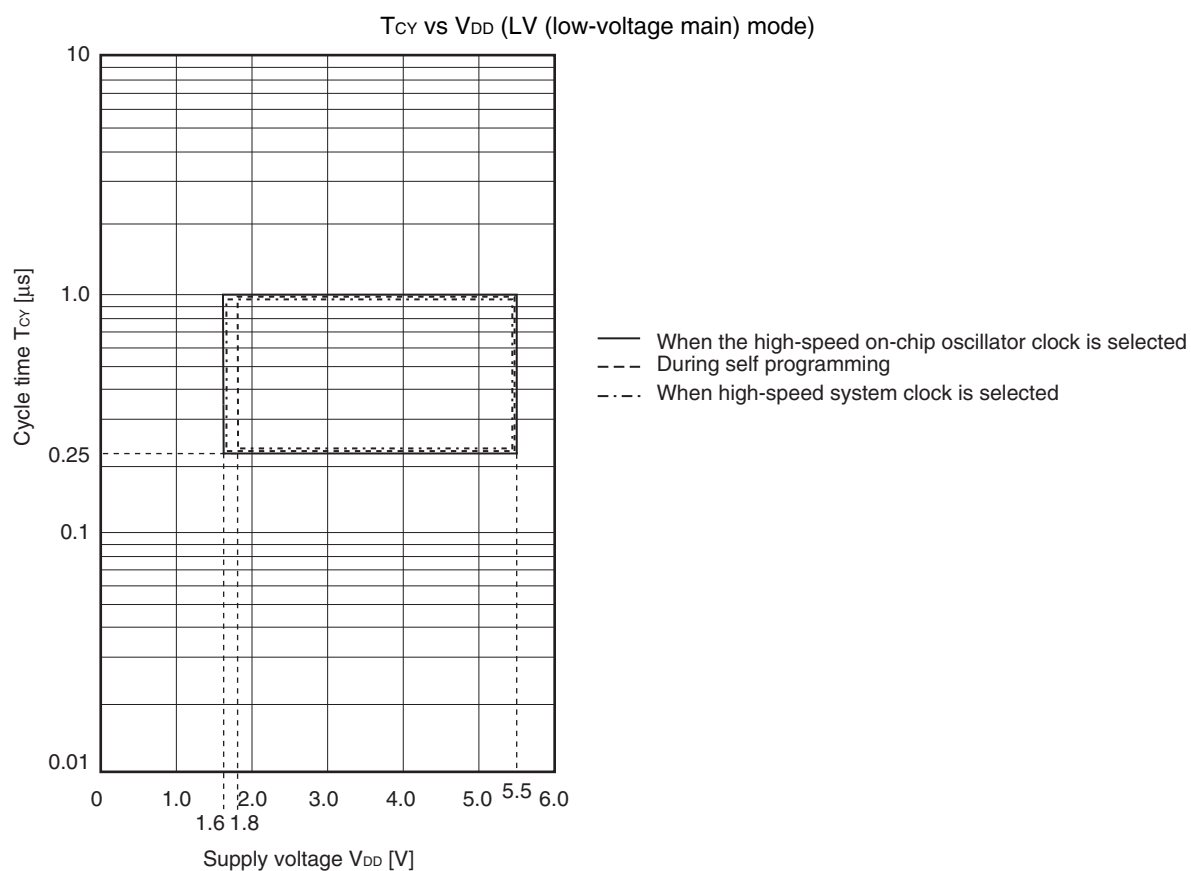
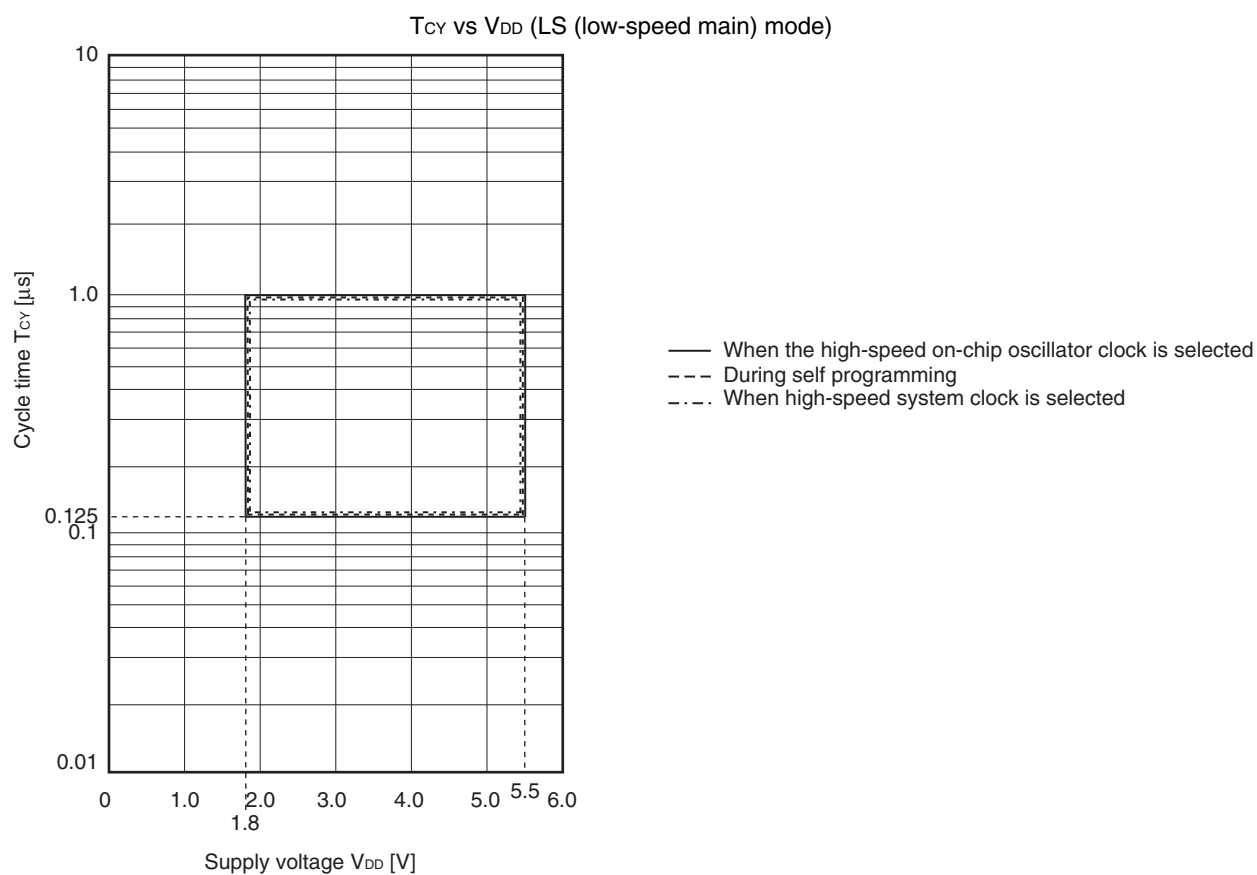
(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.62	1.89	mA	
					V _{DD} = 3.0 V		0.62	1.89	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.50	1.48	mA	
					V _{DD} = 3.0 V		0.50	1.48	mA	
					f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.12	mA
						V _{DD} = 3.0 V		0.44	1.12	mA
				LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		290	620	μA
						V _{DD} = 2.0 V		290	620	μA
				LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		460	700	μA
						V _{DD} = 2.0 V		460	700	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
				LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		110	390	μA
						Resonator connection		160	450	μA
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V		Square wave input		110	390	μA	
					Resonator connection		160	450	μA	
			Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = −40°C	Square wave input		0.31	0.66	μA	
					Resonator connection		0.50	0.85	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input		0.38	0.66	μA	
					Resonator connection		0.57	0.85	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input		0.47	3.49	μA	
					Resonator connection		0.66	3.68	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.80	6.10	μA	
					Resonator connection		0.99	6.29	μA	
				f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input		1.52	10.46	μA	
					Resonator connection		1.71	10.65	μA	
	I _{DD3} ^{Note 6}	STOP mode ^{Note 8}	T _A = −40°C					0.19	0.54	μA
			T _A = +25°C					0.26	0.54	μA
			T _A = +50°C					0.35	3.37	μA
			T _A = +70°C					0.68	5.98	μA
			T _A = +85°C					1.40	10.34	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When $RTCLPC = 1$ and setting ultra-low current consumption ($AMPHS1 = 1$). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

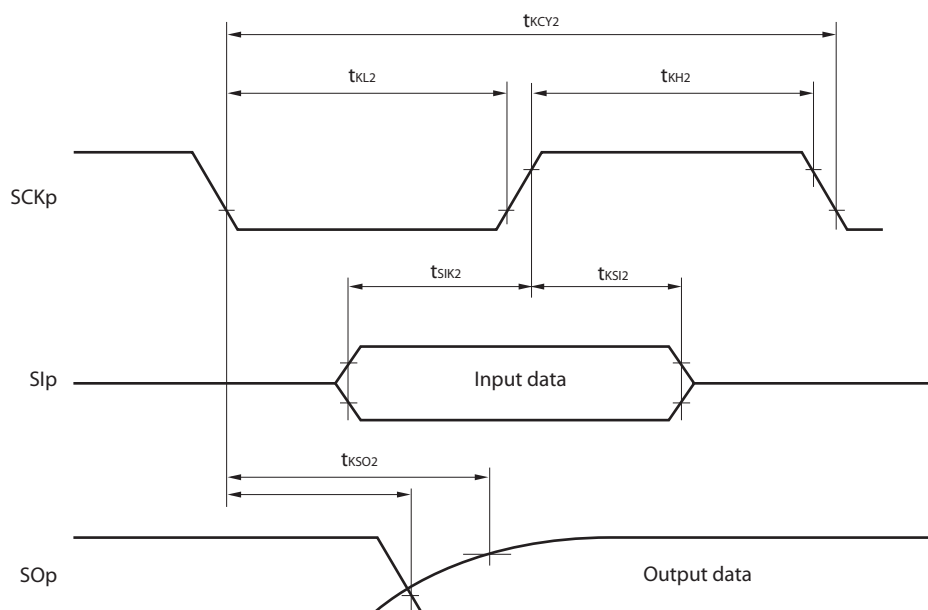
Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 2/f _{CLK}	4.0 V ≤ EV _{DD0} ≤ 5.5 V	62.5		250		500	ns
			2.7 V ≤ EV _{DD0} ≤ 5.5 V	83.3		250		500	ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V	t _{KCY1} /2 – 7		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V	t _{KCY1} /2 – 10		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
Slp setup time (to SCKp↑) Note 1	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V	23		110		110		ns
		2.7 V ≤ EV _{DD0} ≤ 5.5 V	33		110		110		ns
Slp hold time (from SCKp↑) Note 2	t _{KSI1}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t _{KSO1}	C = 20 pF Note 4		10		10		10	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

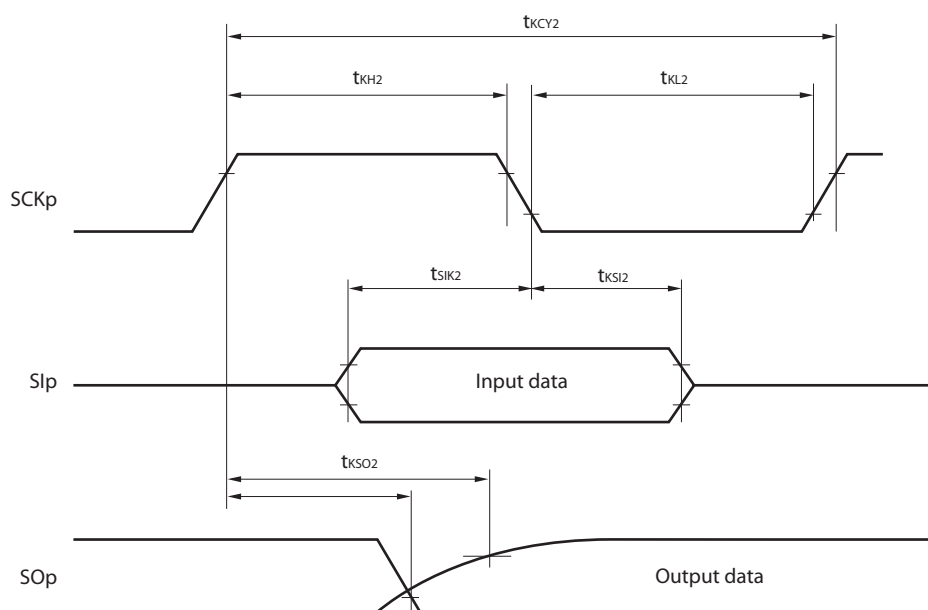
Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. This value is valid only when CSI00's peripheral I/O redirect function is not used.
 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)
 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00))

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution EV _{DD0} = AV _{REFP} = V _{DD} ^{Notes 3, 4}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±5.0	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 5}	1.2	±8.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI26	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57	95	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution EV _{DD0} = AV _{REFP} = V _{DD} ^{Notes 3, 4}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.35	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 5}		±0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution EV _{DD0} = AV _{REFP} = V _{DD} ^{Notes 3, 4}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.35	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 5}		±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution EV _{DD0} = AV _{REFP} = V _{DD} ^{Notes 3, 4}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±3.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 5}		±6.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution EV _{DD0} = AV _{REFP} = V _{DD} ^{Notes 3, 4}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±2.0	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 5}		±2.5	LSB
Analog input voltage	V _{AIN}	ANI16 to ANI26	0		AV _{REFP} and EV _{DD0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	600		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	1000		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	2300		ns
SCKp high-level width	t_{KH1}		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 150$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 340$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 916$		ns
SCKp low-level width	t_{KL1}		$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 24$		ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 36$		ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $\text{C}_b = 30\text{ pF}$, $\text{R}_b = 5.5\text{ k}\Omega$	$t_{\text{KCY1}}/2 - 100$		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

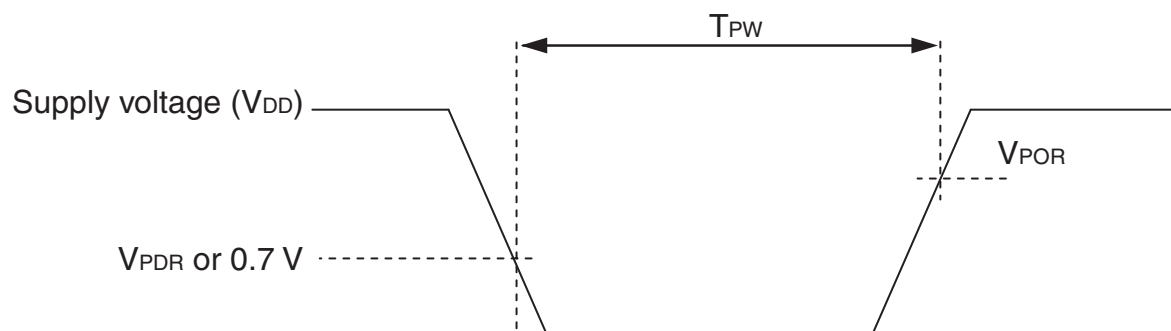
4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.3 POR circuit characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T_{PW}		300			μs

Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V _{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V _{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V _{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V _{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V _{LVD5}	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V _{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V _{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t _{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+105^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V _{LVDD0}	V _{POC2} , V _{POC1} , V _{POC0} = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V _{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V _{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V _{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V