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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

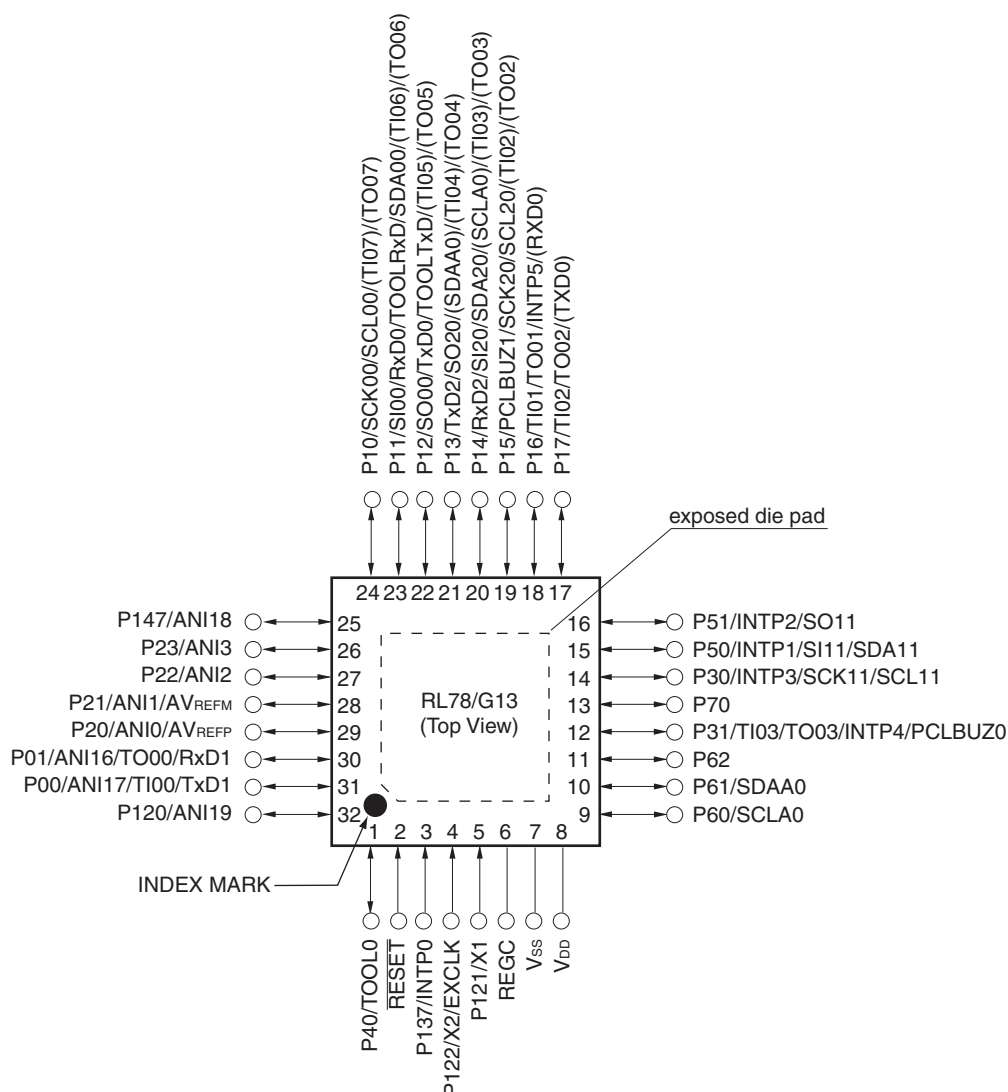| Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100ghgna-w0

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A	R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAFA#X0, R5F100JLAFA#X0
			D	R5F100JCDFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDFA#V0, R5F100JGDFA#V0, R5F100JHDFA#V0, R5F100JJDFA#V0, R5F100JKDFA#V0, R5F100JLDFA#V0 R5F100JCDFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDFA#X0, R5F100JGDFA#X0, R5F100JHDFA#X0, R5F100JJDFA#X0, R5F100JKDFA#X0, R5F100JLDFA#X0
			G	R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0,R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0,R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0
		Not mounted	A	R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAFA#X0, R5F101JLAFA#X0
			D	R5F101JCDFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDFA#V0, R5F101JGDFA#V0, R5F101JHDFA#V0, R5F101JJDFA#V0, R5F101JKDFA#V0, R5F101JLDFA#V0 R5F101JCDFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDFA#X0, R5F101JGDFA#X0, R5F101JHDFA#X0, R5F101JJDFA#X0, R5F101JKDFA#X0, R5F101JLDFA#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

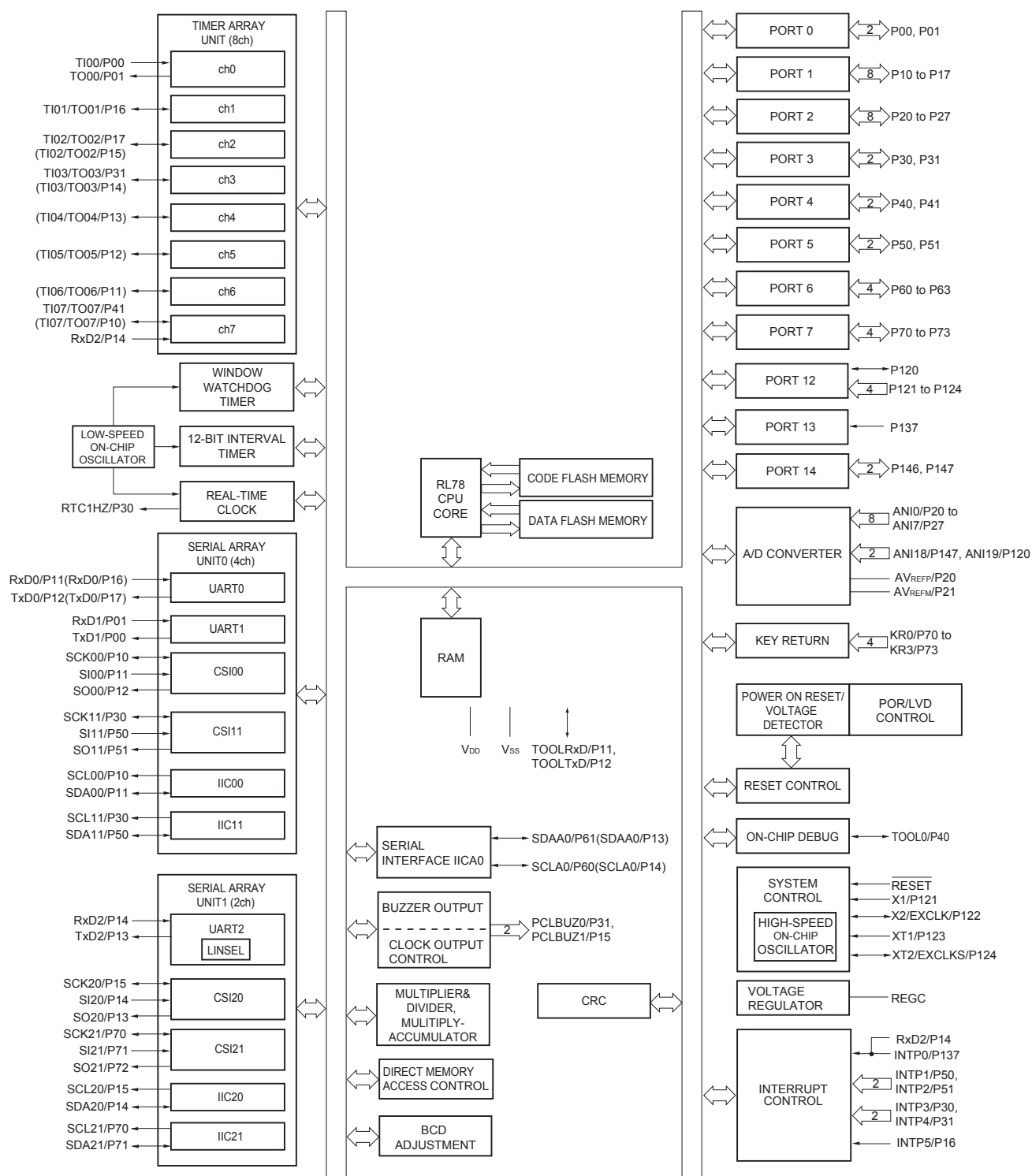**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

  2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

  3. It is recommended to connect an exposed die pad to Vss.

1.5.7 40-pin products
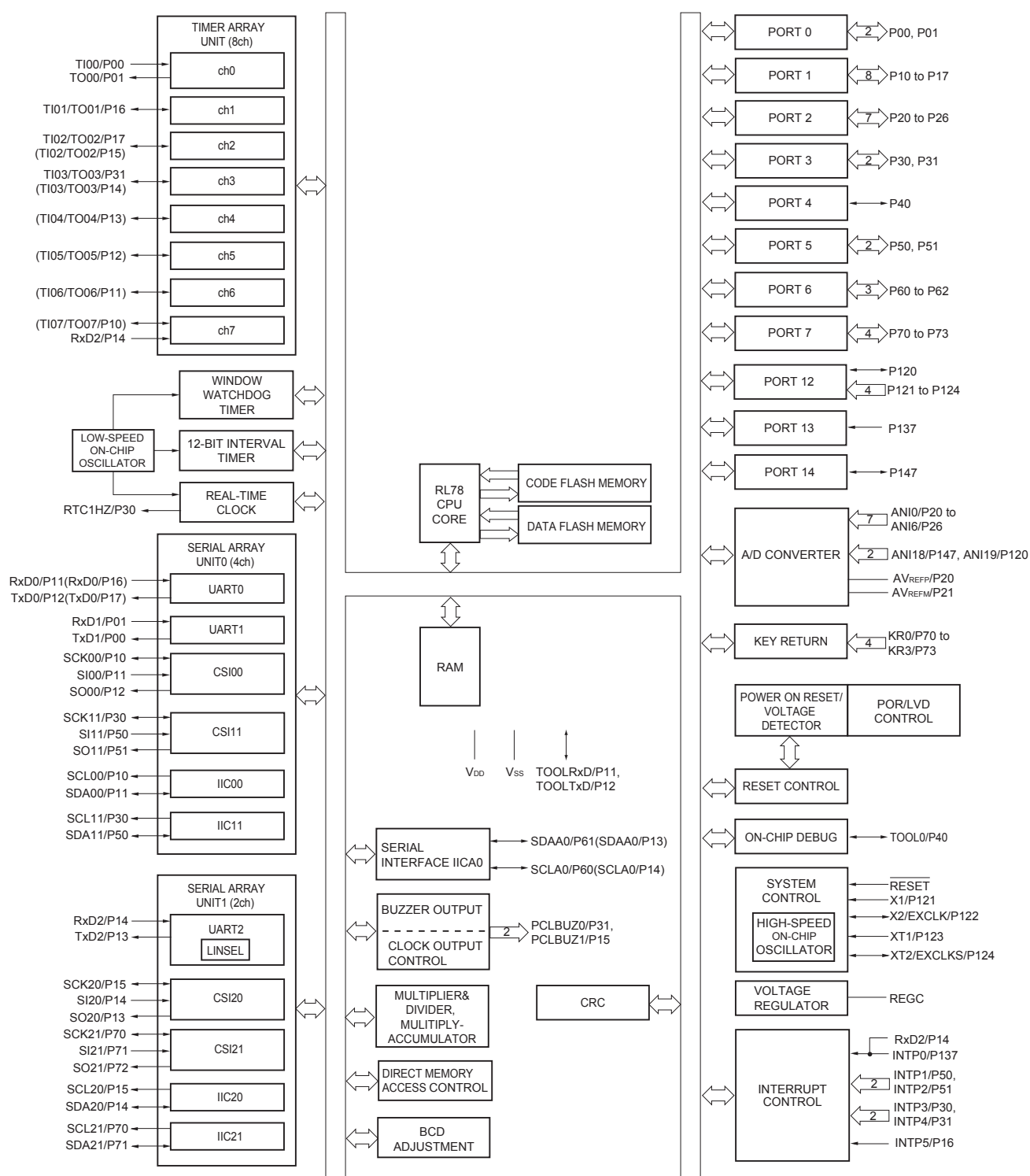
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.8 44-pin products

TIMER ARRAY UNIT (8ch)

TI00/P00 — ch0
TO00/P01

TI01/TO01/P16 — ch1

TI02/TO02/P17
(TI02/TO02/P15) — ch2

TI03/TO03/P31
(TI03/TO03/P14) — ch3

(TI04/TO04/P13) — ch4

(TI05/TO05/P12) — ch5

(TI06/TO06/P11) — ch6

TI07/TO07/P41
(TI07/TO07/P10) — ch7
RxD2/P14

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR — 12-BIT INTERVAL TIMER

RTC1HZ/P30 — REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16) — UART0
TxD0/P12(TxD0/P17)

RxD1/P01 — UART1
TxD1/P00

SCK00/P10
SI00/P11 — CSI00
SO00/P12

SCK11/P30
SI11/P50 — CSI11
SO11/P51

SCL00/P10 — IIC00
SDA00/P11

SCL11/P30 — IIC11
SDA11/P50

SERIAL ARRAY UNIT1 (2ch)

RxD2/P14 — UART2
TxD2/P13   LINSEL

SCK20/P15
SI20/P14 — CSI20
SO20/P13
SCK21/P70
SI21/P71 — CSI21
SO21/P72

SCL20/P15 — IIC20
SDA20/P14

SCL21/P70 — IIC21
SDA21/P71

RL78 CPU CORE

CODE FLASH MEMORY
DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11,
TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13)
SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT
CLOCK OUTPUT CONTROL — 2 — PCLBUZ0/P31,
PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 2 — P00, P01
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 2 — P40, P41
PORT 5 — 2 — P50, P51
PORT 6 — 4 — P60 to P63
PORT 7 — 4 — P70 to P73
PORT 12 — P120
          4 — P121 to P124
PORT 13 — P137
PORT 14 — 2 — P146, P147

A/D CONVERTER — 8 — ANI0/P20 to ANI7/P27
                2 — ANI18/P147, ANI19/P120
                AV$_{REFP}$/P20
                AV$_{REFM}$/P21

KEY RETURN — 4 — KR0/P70 to KR3/P73

POWER ON RESET/ VOLTAGE DETECTOR   POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL
HIGH-SPEED ON-CHIP OSCILLATOR — RESET
X1/P121
X2/EXCLK/P122
XT1/P123
XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL — RxD2/P14
INTP0/P137
2 — INTP1/P50, INTP2/P51
2 — INTP3/P30, INTP4/P31
INTP5/P16

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

4. When setting to PIOR = 1

(2/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output		–		1		1		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)												
8/10-bit resolution A/D converter		6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface		[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel												
	I²C bus	–		1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)												
DMA controller		2 channels											
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt		–											
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access												
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)												
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)												
On-chip debug function		Provided											
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)												
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)												

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

AC Timing Test Points
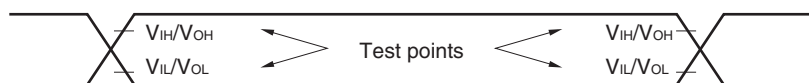
External System Clock Timing
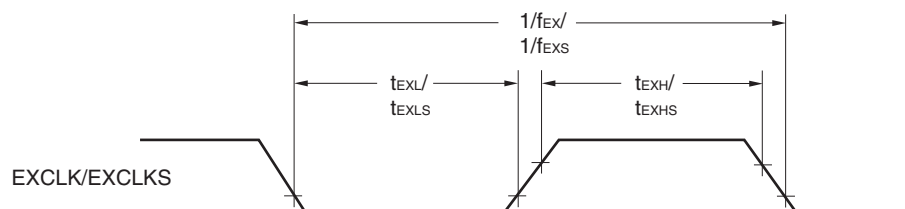
TI/TO Timing
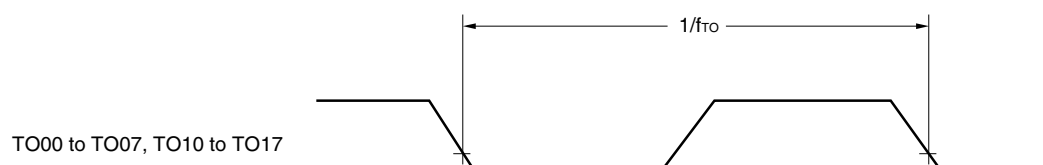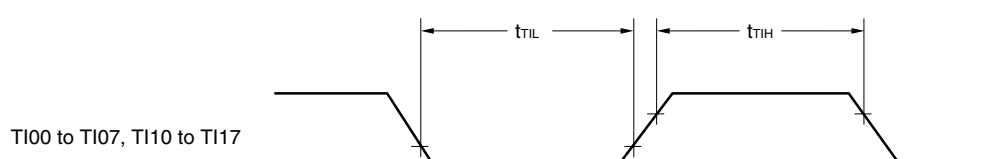
Interrupt Request Input Timing
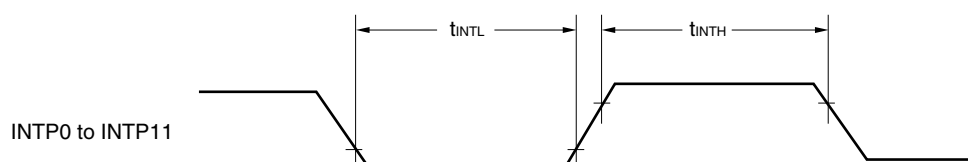
Key Interrupt Input Timing
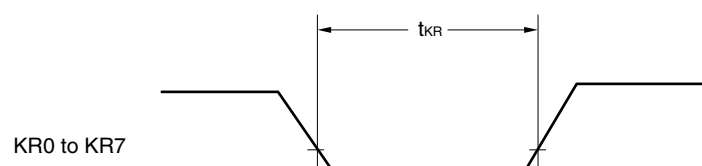
$\overline{\text{RESET}}$ **Input Timing**
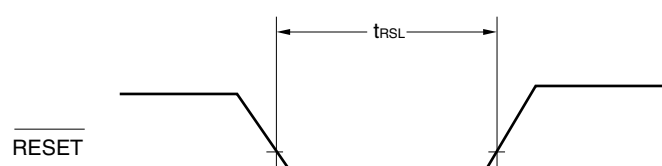
(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(TA = –40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		1.3		0.6	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**		$f_{MCK}/6$ **Note 1**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		1.3		0.6	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		$f_{MCK}/6$ **Notes 1 to 3**		$f_{MCK}/6$ **Notes 1, 2**		$f_{MCK}/6$ **Notes 1, 2**	bps
			Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ **Note 4**		5.3		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

    2. Use it with EVDD0≥Vb.

    3. The following conditions are required for low voltage interface when EVDD0 < VDD.

      2.4 V ≤ EVDD0 < 2.7 V : MAX. 2.6 Mbps

      1.8 V ≤ EVDD0 < 2.4 V : MAX. 1.3 Mbps

    4. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

      HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

                                  16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

      LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

      LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (When 20- to 52-pin products)/EVDD tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.**

Remarks 1. Vb[V]: Communication line voltage

    2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

    3. fMCK: Serial array unit operation clock frequency

      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

    4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]		1.2	±10.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±6.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI14		0		V$_{DD}$	V
		ANI16 to ANI26		0		EV$_{DD0}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{TMPS25}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

      2. This value is indicated as a ratio (%FSR) to the full-scale value.

      3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

      4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.8 Flash Memory Programming Characteristics

(T$_A$ = –40 to +85°C, 1.8 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f$_{CLK}$	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C	100,000			
		Retained for 20 years T$_A$ = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f$_X$)^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency $^{Notes 1, 2}$	f$_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−1.0		+1.0	%
		−40 to −20 °C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−1.5		+1.5	%
		+85 to +105 °C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	−2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				8.5[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			15.0	mA
			2.4 V ≤ EV$_{DD0}$ < 2.7 V			9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			40.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			35.0	mA
			2,4 V ≤ EV$_{DD0}$ < 2.7 V			20.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				80.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P156				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	2,4 V ≤ V$_{DD}$ ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$, EV$_{SS1}$ and V$_{SS}$ pin.

    2. Do not exceed the total current value.

    3. Specification under conditions where the duty factor ≤ 70%.

    The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

    <Example> Where n = 80% and I$_{OL}$ = 10.0 mA

        Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

    However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

    A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter is in operation.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

Remarks 1. f$_{IL}$:   Low-speed on-chip oscillator clock frequency

2. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f$_{CLK}$: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T$_A$ = 25°C

5. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.4 V $\leq$ EV$_{DD0}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)
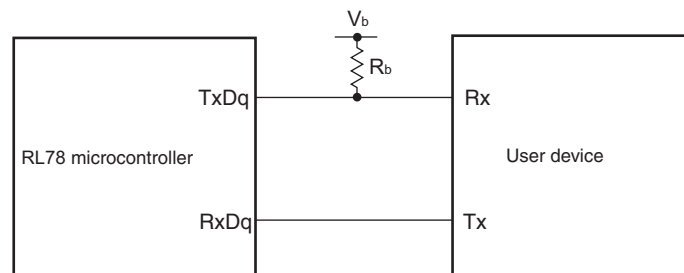
CSI mode connection diagram (during communication at different potential)
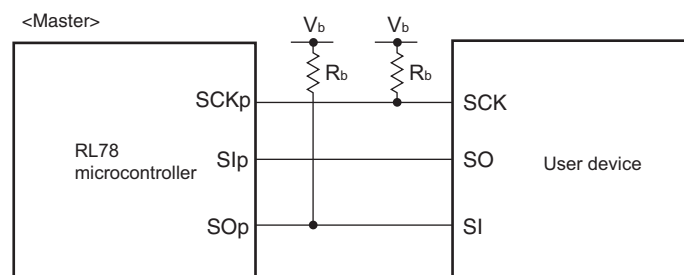
Remarks **1.** R$_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
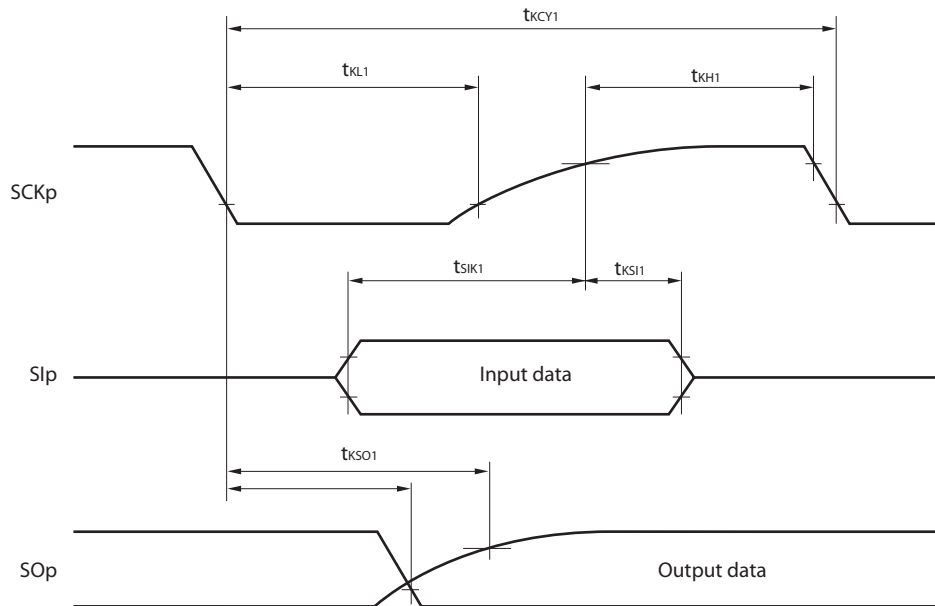
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
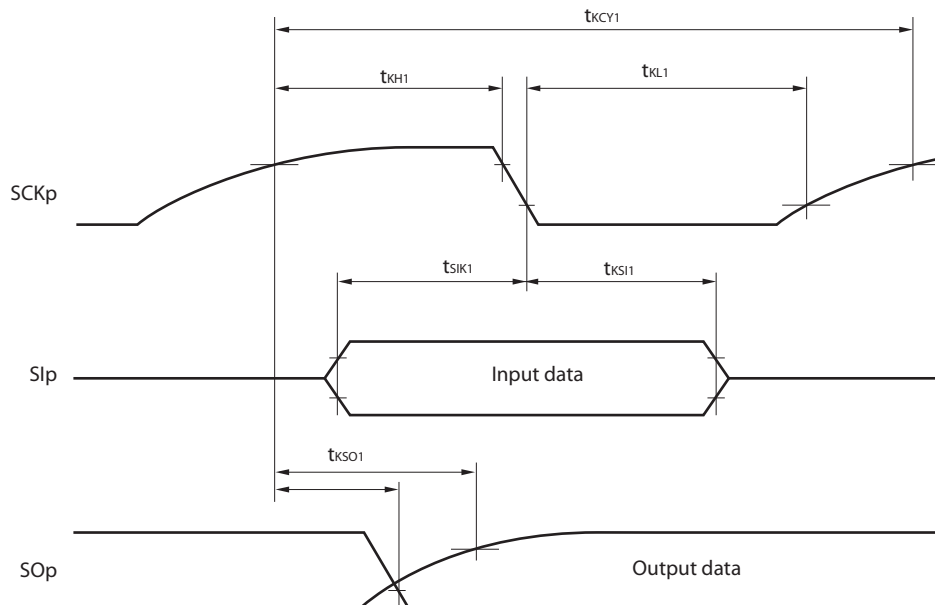
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	12/f$_{MCK}$		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ $\leq$ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	12/f$_{MCK}$		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ $\leq$ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ $\leq$ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ $\leq$ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ $\leq$ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ $\leq$ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		t$_{KCY2}$/2 – 24		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		t$_{KCY2}$/2 – 36		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V [Note 2]		t$_{KCY2}$/2 – 100		ns
SIp setup time (to SCKp↑) [Note2]	t$_{SIK2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ Note 3, Reference voltage (−) = AV$_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

INDEX MARK

DETAIL C

φ b
(LAND PAD)

φ 0.34±0.05
(APERTURE OF
SOLDER RESIST)

DETAIL D

0.70±0.05   R0.17±0.05
0.55±0.05   R0.12±0.05
0.75
0.55

0.55
0.75
0.55±0.05
0.70±0.05

DETAIL E

R0.17±0.05   0.70±0.05
R0.12±0.05   0.55±0.05
0.75
0.55

0.55
0.75
0.55±0.05   R0.275±0.05
0.70±0.05   R0.35±0.05
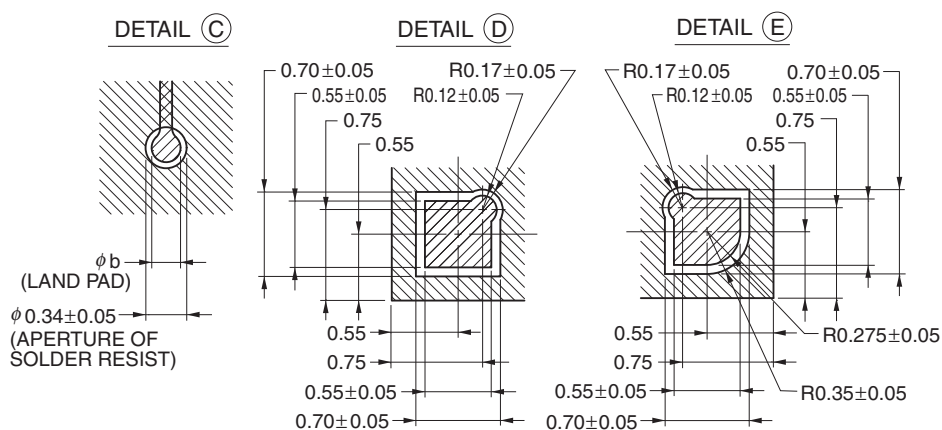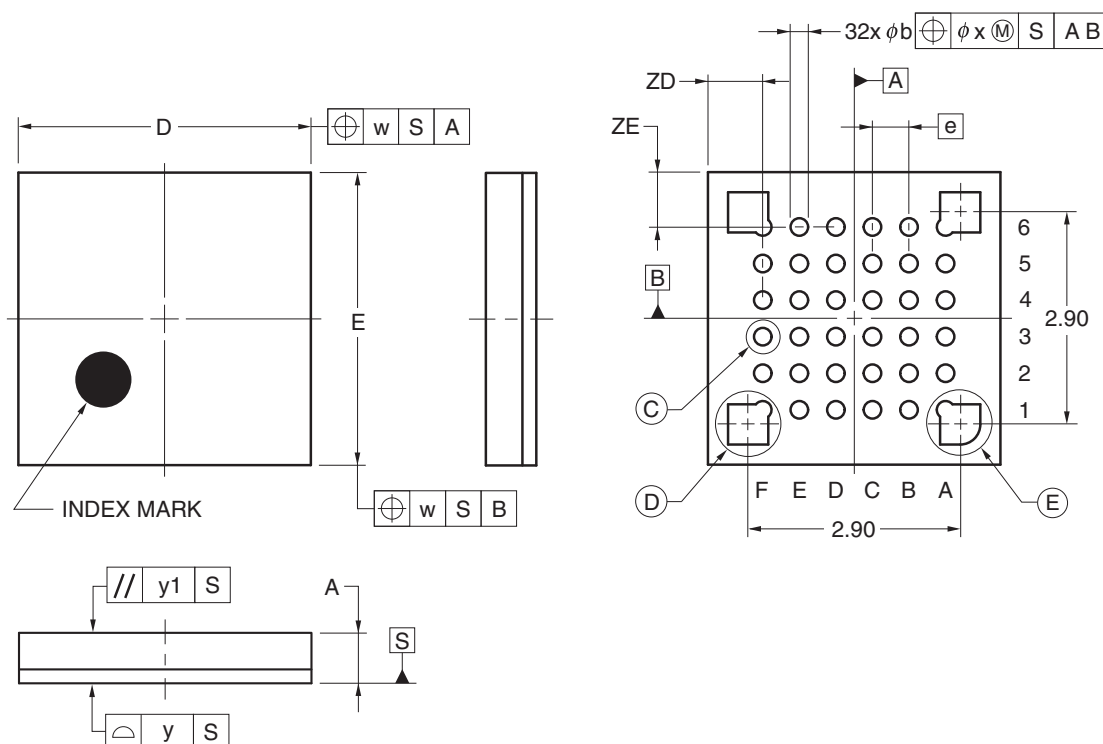
ITEM	DIMENSIONS (UNIT:mm)
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

32x φb   φ x Ⓜ S A B
ZD
ZE
2.90
2.90