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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100jedfa-x0

Table 1-1. List of Ordering Part Numbers

(10/12)

Pin count	Package	Data flash	Fields of Application <small>Note</small>	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGAFA#V0, R5F100MHAFA#V0, R5F100MJAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGAFA#X0, R5F100MHAFA#X0, R5F100MJAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0 R5F100MF DFA#V0, R5F100MG DFA#V0, R5F100MH DFA#V0, R5F100MJD FA#V0, R5F100MK DFA#V0, R5F100MLD FA#V0 R5F100MF DFA#X0, R5F100MG DFA#X0, R5F100MH DFA#X0, R5F100MJD FA#X0, R5F100MK DFA#X0, R5F100MLD FA#X0 R5F100MFG FA#V0, R5F100MGG FA#V0, R5F100MHG FA#V0, R5F100MJG FA#V0 R5F100MFG FA#X0, R5F100MGG FA#X0, R5F100MHG FA#X0, R5F100MJG FA#X0
			D	R5F100MF DFA#V0, R5F100MG DFA#V0, R5F100MH DFA#V0, R5F100MJD FA#V0, R5F100MK DFA#V0, R5F100MLD FA#V0 R5F100MF DFA#X0, R5F100MG DFA#X0, R5F100MH DFA#X0, R5F100MJD FA#X0, R5F100MK DFA#X0, R5F100MLD FA#X0 R5F100MFG FA#V0, R5F100MGG FA#V0, R5F100MHG FA#V0, R5F100MJG FA#V0 R5F100MFG FA#X0, R5F100MGG FA#X0, R5F100MHG FA#X0, R5F100MJG FA#X0
			G	R5F101MFAFA#V0, R5F101MGAFA#V0, R5F101MHAFA#V0, R5F101MJAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGAFA#X0, R5F101MHAFA#X0, R5F101MJAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0 R5F101MF DFA#V0, R5F101MG DFA#V0, R5F101MH DFA#V0, R5F101MJD FA#V0, R5F101MK DFA#V0, R5F101MLD FA#V0 R5F101MF DFA#X0, R5F101MG DFA#X0, R5F101MH DFA#X0, R5F101MJD FA#X0, R5F101MK DFA#X0, R5F101MLD FA#X0 R5F101MFG FA#V0, R5F101MGG FA#V0, R5F101MHG FA#V0, R5F101MJG FA#V0 R5F101MFG FA#X0, R5F101MGG FA#X0, R5F101MHG FA#X0, R5F101MJG FA#X0
		Not mounted	A	R5F101MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0 R5F100MF DFB#V0, R5F100MG DFB#V0, R5F100MH DFB#V0, R5F100MJD FB#V0, R5F100MK DFB#V0, R5F100MLD FB#V0 R5F100MF DFB#X0, R5F100MG DFB#X0, R5F100MH DFB#X0, R5F100MJD FB#X0, R5F100MK DFB#X0, R5F100MLD FB#X0 R5F100MFG FB#V0, R5F100MGG FB#V0, R5F100MHG FB#V0, R5F100MJG FB#V0 R5F100MFG FB#X0, R5F100MGG FB#X0, R5F100MHG FB#X0, R5F100MJG FB#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0 R5F100MF DFB#V0, R5F100MG DFB#V0, R5F100MH DFB#V0, R5F100MJD FB#V0, R5F100MK DFB#V0, R5F100MLD FB#V0 R5F100MF DFB#X0, R5F100MG DFB#X0, R5F100MH DFB#X0, R5F100MJD FB#X0, R5F100MK DFB#X0, R5F100MLD FB#X0 R5F100MFG FB#V0, R5F100MGG FB#V0, R5F100MHG FB#V0, R5F100MJG FB#V0 R5F100MFG FB#X0, R5F100MGG FB#X0, R5F100MHG FB#X0, R5F100MJG FB#X0
			D	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0 R5F100MF DFB#V0, R5F100MG DFB#V0, R5F100MH DFB#V0, R5F100MJD FB#V0, R5F100MK DFB#V0, R5F100MLD FB#V0 R5F100MF DFB#X0, R5F100MG DFB#X0, R5F100MH DFB#X0, R5F100MJD FB#X0, R5F100MK DFB#X0, R5F100MLD FB#X0 R5F100MFG FB#V0, R5F100MGG FB#V0, R5F100MHG FB#V0, R5F100MJG FB#V0 R5F100MFG FB#X0, R5F100MGG FB#X0, R5F100MHG FB#X0, R5F100MJG FB#X0
			G	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0 R5F101MF DFB#V0, R5F101MG DFB#V0, R5F101MH DFB#V0, R5F101MJD FB#V0, R5F101MK DFB#V0, R5F101MLD FB#V0 R5F101MF DFB#X0, R5F101MG DFB#X0, R5F101MH DFB#X0, R5F101MJD FB#X0, R5F101MK DFB#X0, R5F101MLD FB#X0 R5F101MFG FB#V0, R5F101MGG FB#V0, R5F101MHG FB#V0, R5F101MJG FB#V0 R5F101MFG FB#X0, R5F101MGG FB#X0, R5F101MHG FB#X0, R5F101MJG FB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0 R5F101MF DFB#V0, R5F101MG DFB#V0, R5F101MH DFB#V0, R5F101MJD FB#V0, R5F101MK DFB#V0, R5F101MLD FB#V0 R5F101MF DFB#X0, R5F101MG DFB#X0, R5F101MH DFB#X0, R5F101MJD FB#X0, R5F101MK DFB#X0, R5F101MLD FB#X0 R5F101MFG FB#V0, R5F101MGG FB#V0, R5F101MHG FB#V0, R5F101MJG FB#V0 R5F101MFG FB#X0, R5F101MGG FB#X0, R5F101MHG FB#X0, R5F101MJG FB#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(11/12)

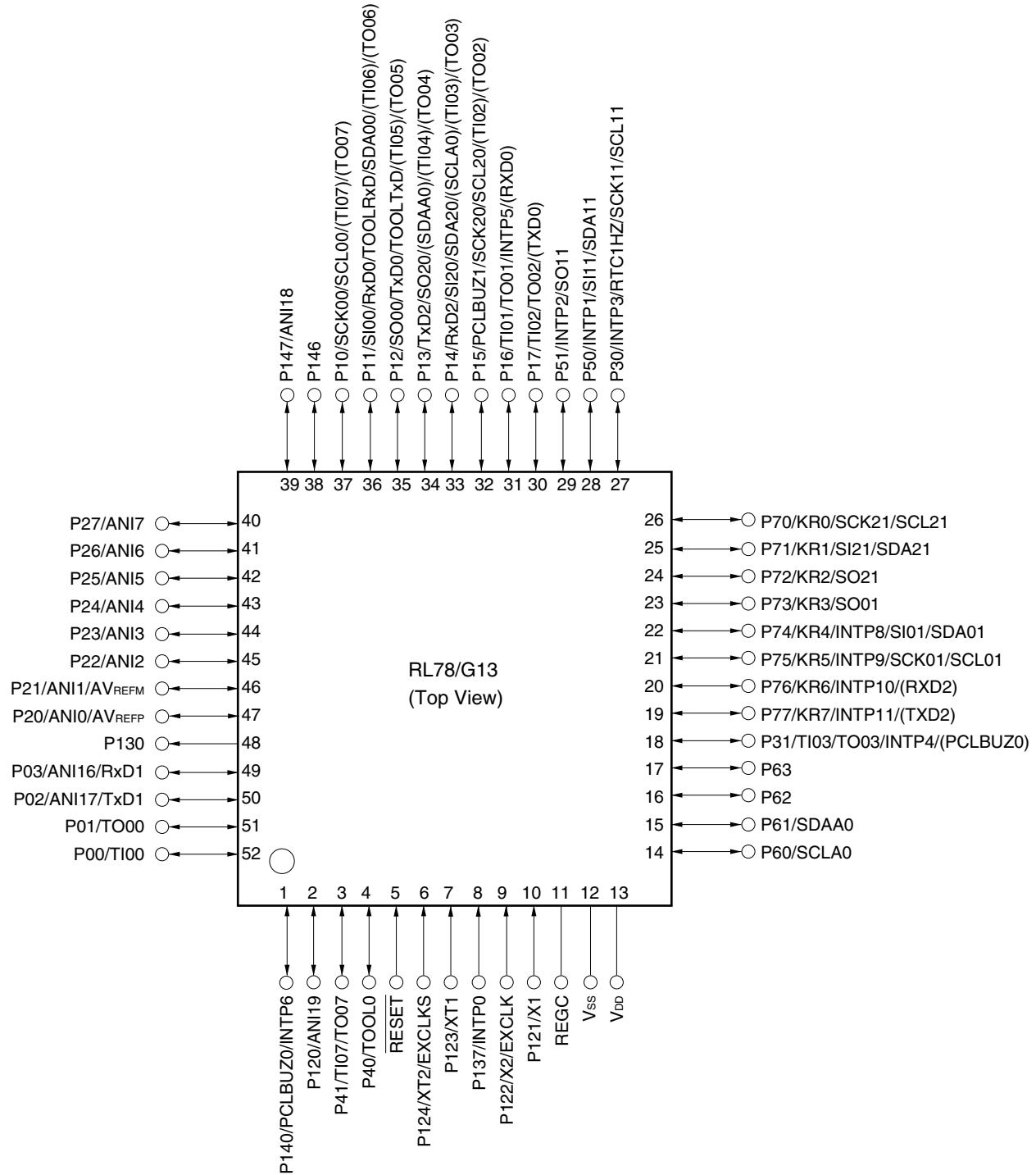
Pin count	Package	Data flash	Fields of Application <small>Note</small>	Ordering Part Number
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	Mounted	A	R5F100PFAFB#V0, R5F100PGAFB#V0, R5F100PHAFB#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFB#X0, R5F100PHAFB#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 R5F100PFDFB#V0, R5F100PGDFB#V0, R5F100PHDFB#V0, R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0 R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0, R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0 R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0, R5F100PJGFB#V0 R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0, R5F100PJGFB#X0
			D	R5F100PFAFB#V0, R5F100PGAFB#V0, R5F100PHAFB#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFB#X0, R5F100PHAFB#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 R5F100PFDFB#V0, R5F100PGDFB#V0, R5F100PHDFB#V0, R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0 R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0, R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0
			G	R5F101PFAFB#V0, R5F101PGAFB#V0, R5F101PHAFB#V0, R5F101PJAFB#V0, R5F101PKAFB#V0, R5F101PLAFB#V0 R5F101PFAFB#X0, R5F101PGAFB#X0, R5F101PHAFB#X0, R5F101PJAFB#X0, R5F101PKAFB#X0, R5F101PLAFB#X0 R5F101PFDFB#V0, R5F101PGDFB#V0, R5F101PHDFB#V0, R5F101PJDFB#V0, R5F101PKDFB#V0, R5F101PLDFB#V0 R5F101PFDFB#X0, R5F101PGDFB#X0, R5F101PHDFB#X0, R5F101PJDFB#X0, R5F101PKDFB#X0, R5F101PLDFB#X0
		Not mounted	A	R5F101PFAFB#V0, R5F101PGAFB#V0, R5F101PHAFB#V0, R5F101PJAFB#V0, R5F101PKAFB#V0, R5F101PLAFB#V0 R5F101PFAFB#X0, R5F101PGAFB#X0, R5F101PHAFB#X0, R5F101PJAFB#X0, R5F101PKAFB#X0, R5F101PLAFB#X0 R5F101PFDFB#V0, R5F101PGDFB#V0, R5F101PHDFB#V0, R5F101PJDFB#V0, R5F101PKDFB#V0, R5F101PLDFB#V0 R5F101PFDFB#X0, R5F101PGDFB#X0, R5F101PHDFB#X0, R5F101PJDFB#X0, R5F101PKDFB#X0, R5F101PLDFB#X0
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	Mounted	A	R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFKA#V0, R5F100PKAFKA#V0, R5F100PLAFA#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFKA#X0, R5F100PKAFKA#X0, R5F100PLAFA#X0 R5F100PF DFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJ DFA#V0, R5F100PK DFA#V0, R5F100PL DFA#V0 R5F100PF DFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJ DFA#X0, R5F100PK DFA#X0, R5F100PL DFA#X0 R5F100PFGFA#V0, R5F100PGGFA#V0, R5F100PHGFA#V0, R5F100PJGFA#V0 R5F100PFGFA#X0, R5F100PGGFA#X0, R5F100PHGFA#X0, R5F100PJGFA#X0
			D	R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFKA#V0, R5F100PKAFKA#V0, R5F100PLAFA#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFKA#X0, R5F100PKAFKA#X0, R5F100PLAFA#X0 R5F100PF DFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJ DFA#V0, R5F100PK DFA#V0, R5F100PL DFA#V0 R5F100PF DFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJ DFA#X0, R5F100PK DFA#X0, R5F100PL DFA#X0
			G	R5F100PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFA#V0, R5F100PJAFKA#V0, R5F100PKAFKA#V0, R5F100PLAFA#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFA#X0, R5F100PJAFKA#X0, R5F100PKAFKA#X0, R5F100PLAFA#X0 R5F100PF DFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJ DFA#V0, R5F100PK DFA#V0, R5F100PL DFA#V0 R5F100PF DFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJ DFA#X0, R5F100PK DFA#X0, R5F100PL DFA#X0
		Not mounted	A	R5F101PFAFA#V0, R5F101PGAFA#V0, R5F101PHAFA#V0, R5F101PJAFKA#V0, R5F101PKAFKA#V0, R5F101PLAFA#V0 R5F101PFAFA#X0, R5F101PGAFA#X0, R5F101PHAFA#X0, R5F101PJAFKA#X0, R5F101PKAFKA#X0, R5F101PLAFA#X0 R5F101PF DFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJ DFA#V0, R5F101PK DFA#V0, R5F101PL DFA#V0 R5F101PF DFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJ DFA#X0, R5F101PK DFA#X0, R5F101PL DFA#X0

Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)

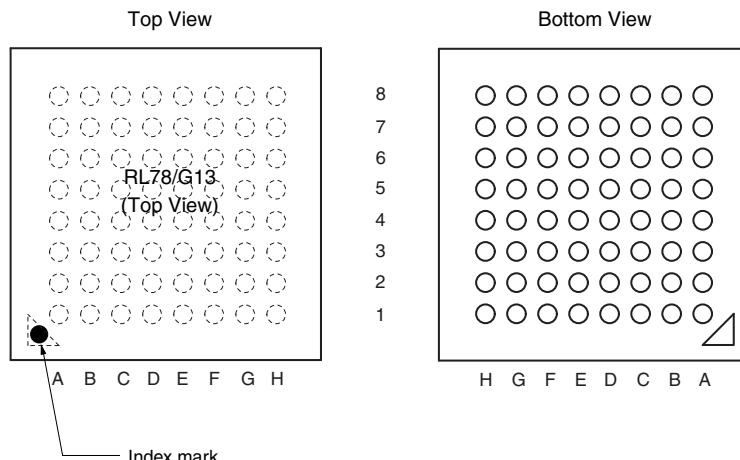


Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05	C1	P51/INTP2/SO11	E1	P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)	G1	P146
A2	P30/INTP3/RTC1HZ/SCK11/SCL11	C2	P71/KR1/SI21/SDA21	E2	P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)	G2	P25/ANI5
A3	P70/KR0/SCK21/SCL21	C3	P74/KR4/INTP8/SI01/SDA01	E3	P15/SCK20/SCL20/(TI02)/(TO02)	G3	P24/ANI4
A4	P75/KR5/INTP9/SCK01/SCL01	C4	P52/(INTP10)	E4	P16/TI01/TO01/INTP5/(SI00)/(RxD0)	G4	P22/ANI2
A5	P77/KR7/INTP11/(TxD2)	C5	P53/(INTP11)	E5	P03/ANI16/SI10/RxD1/SDA10	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/TI07/TO07	G6	P02/ANI17/SO10/TxD1
A7	P60/SCLA0	C7	V _{ss}	E7	RESET	G7	P00/TI00
A8	EV _{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/INTP1/SI11/SDA11	D1	P55/(PCLBUZ1)/(SCK00)	F1	P10/SCK00/SCL00/(TI07)/(TO07)	H1	P147/ANI18
B2	P72/KR2/SO21	D2	P06/TI06/TO06	F2	P11/SI00/RxD0/TOOLRxDSDA00/(TI06)/(TO06)	H2	P27/ANI7
B3	P73/KR3/SO01	D3	P17/TI02/TO02/(SO00)/(TxD0)	F3	P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)	H3	P26/ANI6
B4	P76/KR6/INTP10/(RxD2)	D4	P54	F4	P21/ANI1/AV _{REFM}	H4	P23/ANI3
B5	P31/TI03/TO03/INTP4/(PCLBUZ0)	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10	H5	P20/ANI0/AV _{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V _{DD}	D7	REGC	F7	P01/TO00	H7	P140/PCLBUZ0/INTP6
B8	EV _{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

Cautions 1. Make EV_{SS0} pin the same potential as V_{ss} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
3. Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

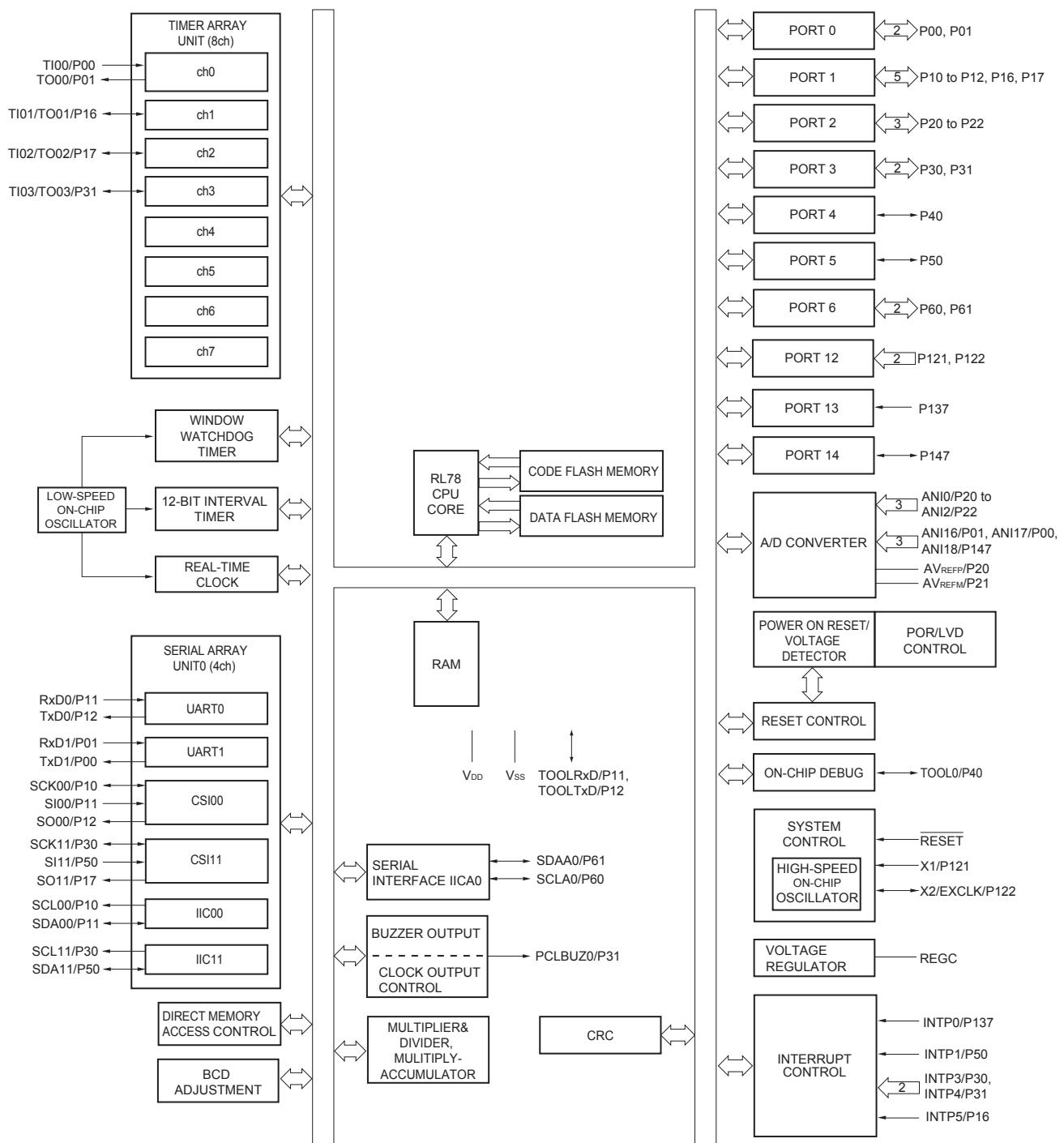
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{ss} and EV_{SS0} pins to separate ground lines.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

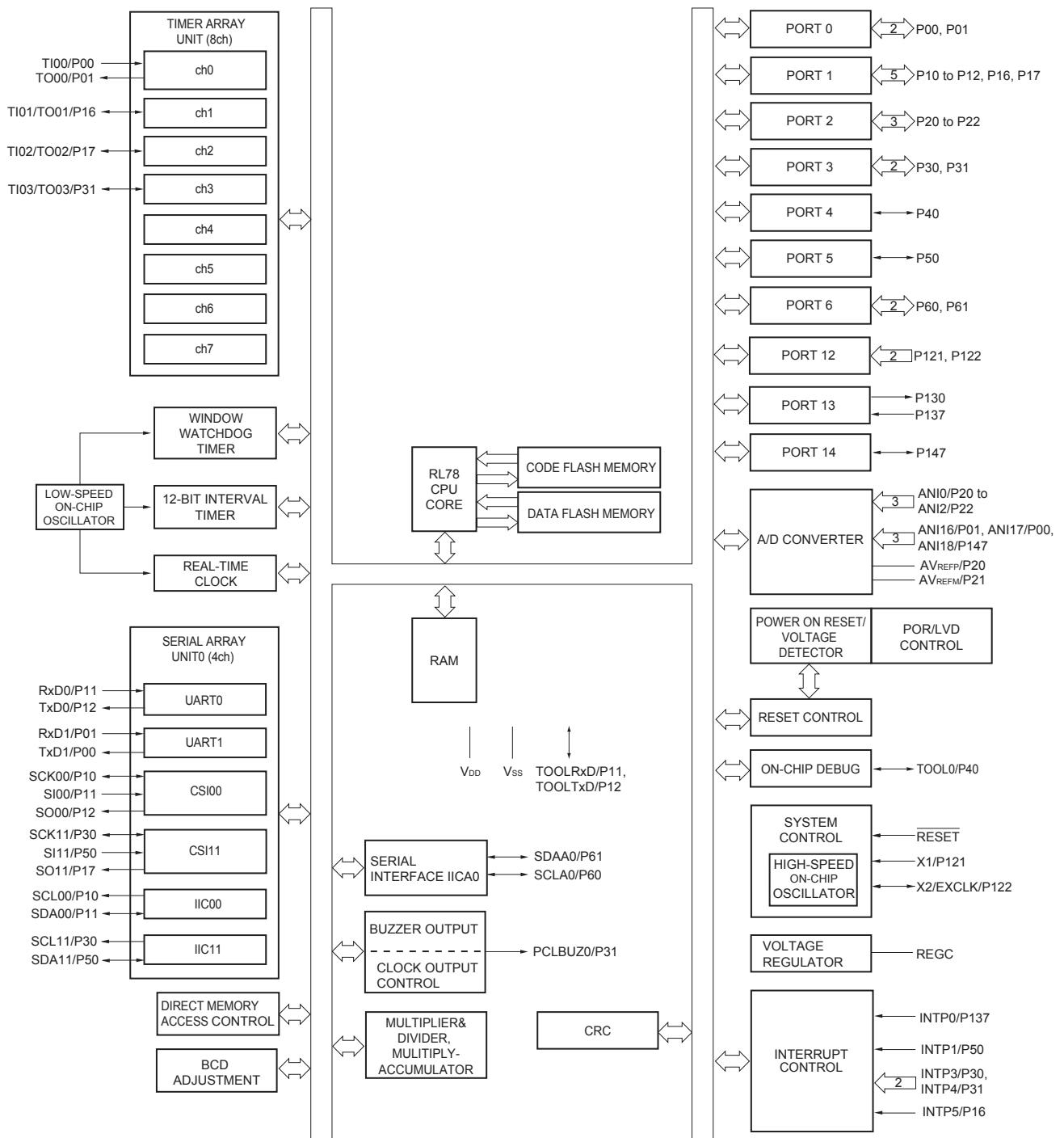
1.4 Pin Identification

AN10 to AN14,		REGC:	Regulator capacitance
AN16 to ANI26:	Analog input	RESET:	Reset
AV _{REFM} :	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AV _{REFP} :	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EV _{VDD0} , EV _{VDD1} :	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EV _{SS0} , EV _{SS1} :	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11,	
KR0 to KR7:	Key return	SDA20, SDA21, SDA30, SDA31:	Serial data input/output
P00 to P07:	Port 0	SI00, SI01, SI10, SI11,	
P10 to P17:	Port 1	SI20, SI21, SI30, SI31:	Serial data input
P20 to P27:	Port 2	SO00, SO01, SO10,	
P30 to P37:	Port 3	SO11, SO20, SO21,	
P40 to P47:	Port 4	SO30, SO31:	Serial data output
P50 to P57:	Port 5	TI00 to TI07,	
P60 to P67:	Port 6	TI10 to TI17:	Timer input
P70 to P77:	Port 7	TO00 to TO07,	
P80 to P87:	Port 8	TO10 to TO17:	Timer output
P90 to P97:	Port 9	TOOL0:	Data input/output for tool
P100 to P106:	Port 10	TOOLRxD, TOOLTxD:	Data input/output for external device
P110 to P117:	Port 11	TxD0 to TxD3:	Transmit data
P120 to P127:	Port 12	V _{DD} :	Power supply
P130, P137:	Port 13	V _{SS} :	Ground
P140 to P147:	Port 14	X1, X2:	Crystal oscillator (main system clock)
P150 to P156:	Port 15	XT1, XT2:	Crystal oscillator (subsystem clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

1.5.2 24-pin products



1.5.3 25-pin products



2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products A: Consumer applications $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxAxx, R5F101xxAxx

D: Industrial applications $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxDxx, R5F101xxDxx

G: Industrial applications when $T_A = -40$ to $+105^\circ\text{C}$ products is used in the range of $T_A = -40$ to $+85^\circ\text{C}$

R5F100xxGxx

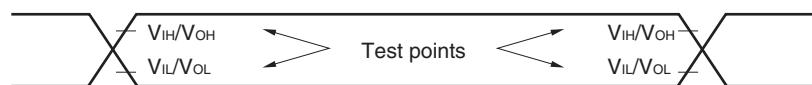
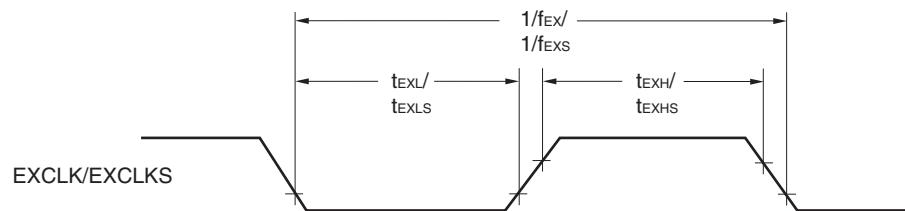
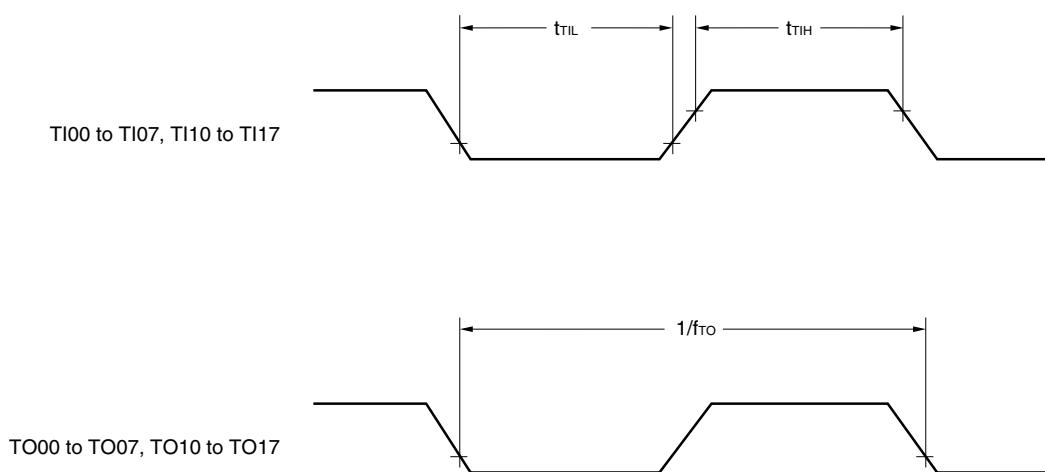
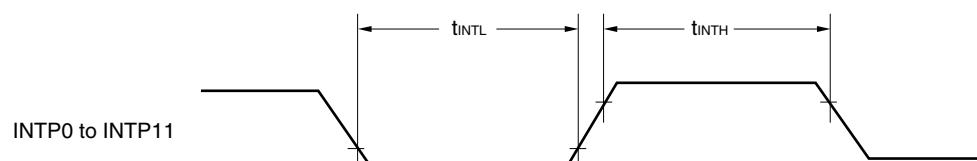
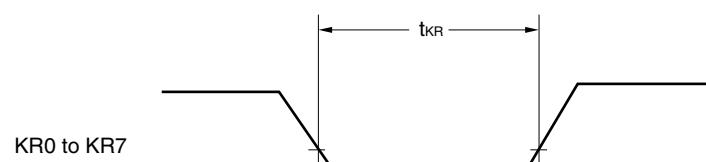
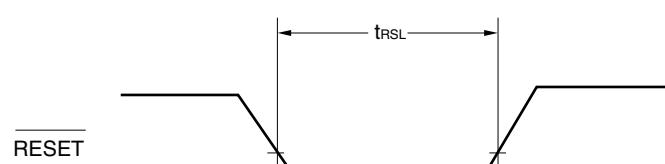
- Cautions**
1. **The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**
 2. **With products not provided with an $\text{EV}_{\text{DD}0}$, $\text{EV}_{\text{DD}1}$, $\text{EV}_{\text{SS}0}$, or $\text{EV}_{\text{SS}1}$ pin, replace $\text{EV}_{\text{DD}0}$ and $\text{EV}_{\text{DD}1}$ with V_{DD} , or replace $\text{EV}_{\text{SS}0}$ and $\text{EV}_{\text{SS}1}$ with V_{ss} .**
 3. **The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.**

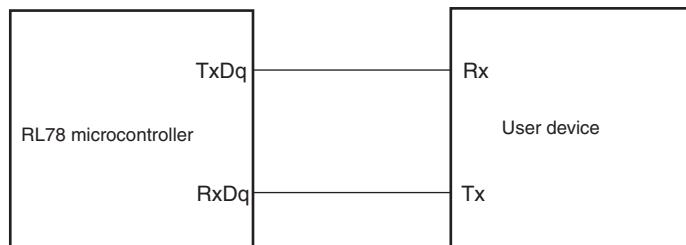
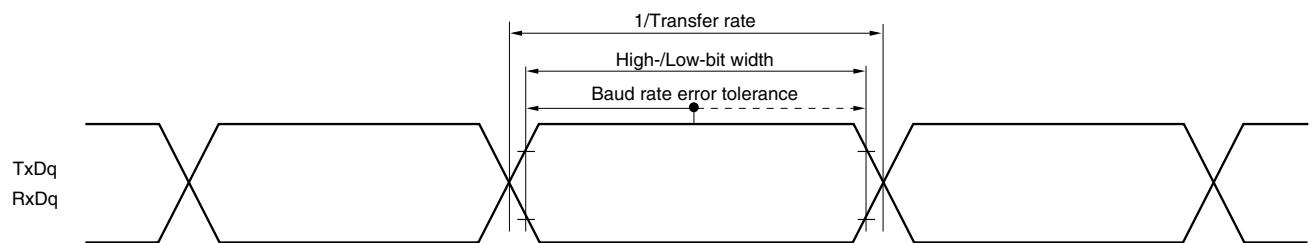
2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
		Subsystem clock (f _{SUB}) operation		1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V _{DD} < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25		1	μs
External system clock frequency	f _{EX}	2.7 V ≤ V _{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V _{DD} < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V _{DD} < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V _{DD} < 1.8 V			1.0		4.0	MHz
	f _{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V _{DD} < 2.7 V			30			ns
		1.8 V ≤ V _{DD} < 2.4 V			60			ns
		1.6 V ≤ V _{DD} < 1.8 V			120			ns
	t _{EXHS} , t _{EXLS}				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t _{TIH} , t _{TL}				1/f _{MCK} +10			ns ^{Note}
TO00 to TO07, TO10 to TO17 output frequency	f _{TO}	HS (high-speed main) mode	4.0 V ≤ EV _{DD0} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD0} < 4.0 V				8	MHz
			1.8 V ≤ EV _{DD0} < 2.7 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
		LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 5.5 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.6 V ≤ EV _{DD0} ≤ 5.5 V				2	MHz
		HS (high-speed main) mode	4.0 V ≤ EV _{DD0} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV _{DD0} < 4.0 V				8	MHz
			1.8 V ≤ EV _{DD0} < 2.7 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 5.5 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
		LV (low-voltage main) mode	1.8 V ≤ EV _{DD0} ≤ 5.5 V				4	MHz
			1.6 V ≤ EV _{DD0} < 1.8 V				2	MHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V				4	MHz
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 5.5 V	1				μs
		INTP1 to INTP11	1.6 V ≤ EV _{DD0} ≤ 5.5 V	1				μs
Key interrupt input low-level width	t _{KR}	KR0 to KR7	1.8 V ≤ EV _{DD0} ≤ 5.5 V	250				ns
			1.6 V ≤ EV _{DD0} < 1.8 V	1				μs
RESET low-level width	t _{RSR}				10			μs

(Note and Remark are listed on the next page.)

AC Timing Test Points**External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

UART mode connection diagram (during communication at same potential)**UART mode bit width (during communication at same potential) (reference)**

Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years TA = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library
3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(TA = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

($T_A = -40$ to $+105^\circ\text{C}$, $2.4 \text{ V} \leq EV_{DD0} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = 0 \text{ V}$) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit	
Supply current <small>Note 1</small>	I_{DD1}	Operating mode	HS (high-speed main) mode <small>Note 5</small>	$f_{IH} = 32 \text{ MHz}^{\text{Note 3}}$	Basic operation	$V_{DD} = 5.0 \text{ V}$		2.1		mA	
					Normal operation	$V_{DD} = 3.0 \text{ V}$		2.1		mA	
					$V_{DD} = 5.0 \text{ V}$		4.6	7.5		mA	
					$V_{DD} = 3.0 \text{ V}$		4.6	7.5		mA	
					$V_{DD} = 5.0 \text{ V}$		3.7	5.8		mA	
					$V_{DD} = 3.0 \text{ V}$		3.7	5.8		mA	
					$V_{DD} = 5.0 \text{ V}$		2.7	4.2		mA	
					$V_{DD} = 3.0 \text{ V}$		2.7	4.2		mA	
		HS (high-speed main) mode <small>Note 5</small>		$f_{MX} = 20 \text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0 \text{ V}$	Normal operation	Square wave input		3.0	4.9	mA	
						Resonator connection		3.2	5.0	mA	
				$f_{MX} = 20 \text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0 \text{ V}$	Normal operation	Square wave input		3.0	4.9	mA	
						Resonator connection		3.2	5.0	mA	
				$f_{MX} = 10 \text{ MHz}^{\text{Note 2}}$, $V_{DD} = 5.0 \text{ V}$	Normal operation	Square wave input		1.9	2.9	mA	
						Resonator connection		1.9	2.9	mA	
				$f_{MX} = 10 \text{ MHz}^{\text{Note 2}}$, $V_{DD} = 3.0 \text{ V}$	Normal operation	Square wave input		1.9	2.9	mA	
						Resonator connection		1.9	2.9	mA	
		Subsystem clock operation	$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 4</small> $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9		μA	
						Resonator connection		4.2	5.0	μA	
						Square wave input		4.1	4.9	μA	
						Resonator connection		4.2	5.0	μA	
						Square wave input		4.2	5.5	μA	
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 4</small> $T_A = +25^\circ\text{C}$	Normal operation		Resonator connection		4.3	5.6	μA	
						Square wave input		4.3	6.3	μA	
						Resonator connection		4.4	6.4	μA	
						Square wave input		4.6	7.7	μA	
						Resonator connection		4.7	7.8	μA	
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 4</small> $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7		μA	
						Resonator connection		7.0	19.8	μA	

(Notes and Remarks are listed on the next page.)

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4 \text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0 \text{ V}$) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32 \text{ MHz}$ ^{Note 3}	Basic operation	$V_{DD} = 5.0 \text{ V}$		2.3	mA
					Normal operation	$V_{DD} = 3.0 \text{ V}$		2.3	mA
				$f_{IH} = 24 \text{ MHz}$ ^{Note 3}	Normal operation	$V_{DD} = 5.0 \text{ V}$		5.2	mA
					Normal operation	$V_{DD} = 3.0 \text{ V}$		5.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20 \text{ MHz}$ ^{Note 2} , $V_{DD} = 5.0 \text{ V}$	Normal operation	Square wave input		3.4	mA
					Normal operation	Resonator connection		3.6	mA
				$f_{MX} = 20 \text{ MHz}$ ^{Note 2} , $V_{DD} = 3.0 \text{ V}$	Normal operation	Square wave input		3.4	mA
					Normal operation	Resonator connection		3.6	mA
		Subsystem clock operation	$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		2.1	3.5	mA
				Normal operation	Resonator connection		2.1	3.5	mA
				$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.9	5.9 μA
					Normal operation	Resonator connection		5.0	6.0 μA
			$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		5.0	7.6 μA	
				Normal operation	Resonator connection		5.1	7.7 μA	
				$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.2	9.3 μA
					Normal operation	Resonator connection		5.3	9.4 μA
			$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		5.7	13.3 μA	
				Normal operation	Resonator connection		5.8	13.4 μA	
			$f_{SUB} = 32.768 \text{ kHz}$ ^{Note 4} $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		10.0	46.0 μA	
				Normal operation	Resonator connection		10.0	46.0 μA	

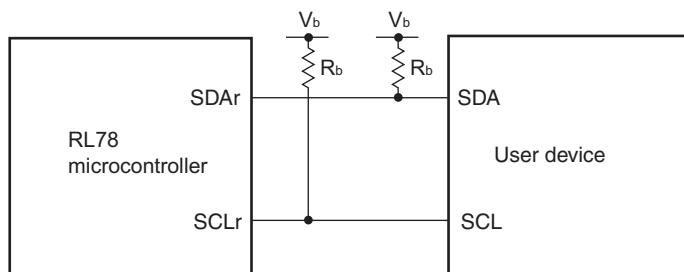
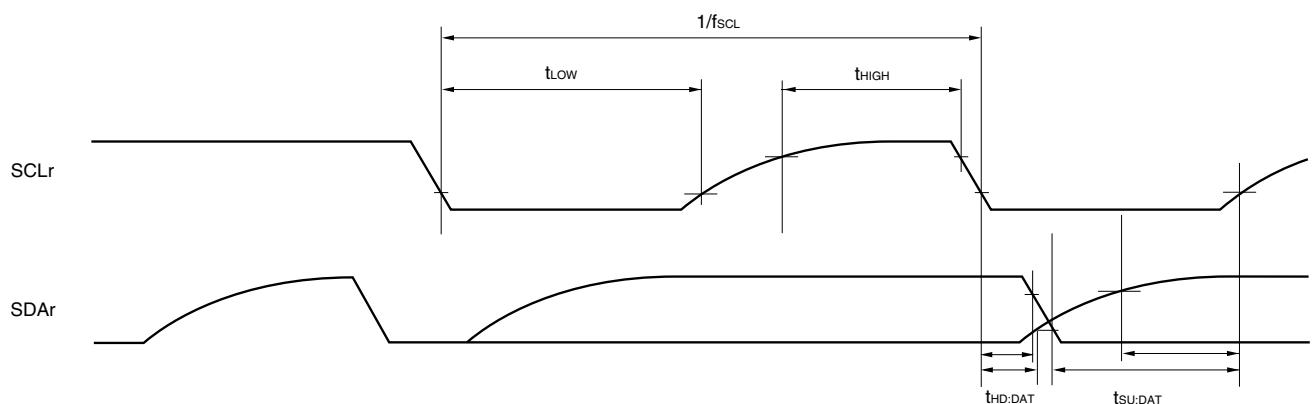
(Notes and Remarks are listed on the next page.)

(3) Peripheral Functions (Common to all products)(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} Note 1				0.20		μA
RTC operating current	I _{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I _{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I _{WDT} Notes 1, 2, 5	f _{IL} = 15 kHz			0.22		μA
A/D converter operating current	I _{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I _{TMPS} Note 1				75.0		μA
LVD operating current	I _{LVD} Notes 1, 7				0.08		μA
Self programming operating current	I _{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I _{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I _{SNOZ} Note 1	ADC operation	The mode is performed ^{Note 10}		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V_{DD}.

2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remarks

- 1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
- 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
- 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = Vss	Reference voltage (+) = VBGR Reference voltage (-) = AVREFM
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI26	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

- (1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, Vss = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

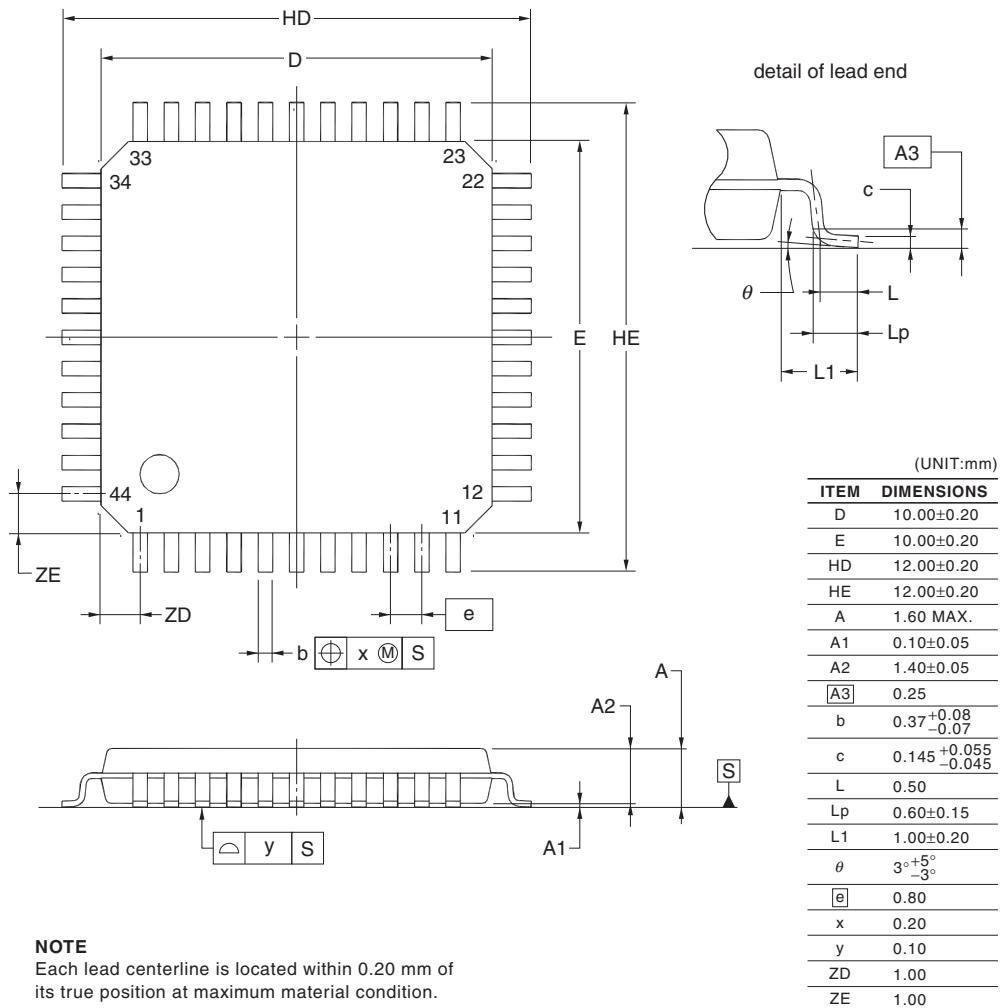
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AVREFP = VDD ^{Note 3}	2.4 V ≤ AVREFP ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	10-bit resolution AVREFP = VDD ^{Note 3}	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Full-scale error ^{Notes 1, 2}	Efs	10-bit resolution AVREFP = VDD ^{Note 3}	2.4 V ≤ AVREFP ≤ 5.5 V			±0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AVREFP = VDD ^{Note 3}	2.4 V ≤ AVREFP ≤ 5.5 V			±2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AVREFP = VDD ^{Note 3}	2.4 V ≤ AVREFP ≤ 5.5 V			±1.5	LSB
Analog input voltage	VAIN	ANI2 to ANI14		0		AVREFP	V
		Internal reference voltage output (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)			VBGR ^{Note 4}		V
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)			VTMPS25 ^{Note 4}		V

(Notes are listed on the next page.)

4.8 44-pin Products

R5F100FAAfp, R5F100FCAfp, R5F100FDAfp, R5F100FEAfp, R5F100FFAfp, R5F100FGAfp,
 R5F100FHAfp, R5F100FJAfp, R5F100FKAfp, R5F100FLAfp
 R5F101FAAfp, R5F101FCAfp, R5F101FDAfp, R5F101FEAfp, R5F101FFAfp, R5F101FGAfp,
 R5F101FHAfp, R5F101FJAfp, R5F101FKAfp, R5F101FLAfp
 R5F100FADfp, R5F100FCDFP, R5F100FDDfp, R5F100FEDfp, R5F100FFDFP, R5F100FGDFP,
 R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
 R5F101FADfp, R5F101FCDFP, R5F101FDDfp, R5F101FEDfp, R5F101FFDFP, R5F101FGDFP,
 R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP
 R5F100FAGfp, R5F100FCGfp, R5F100FDGfp, R5F100FEGfp, R5F100FFGfp, R5F100FGGfp,
 R5F100FHGfp, R5F100FJGfp

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,

R5F100LJABG

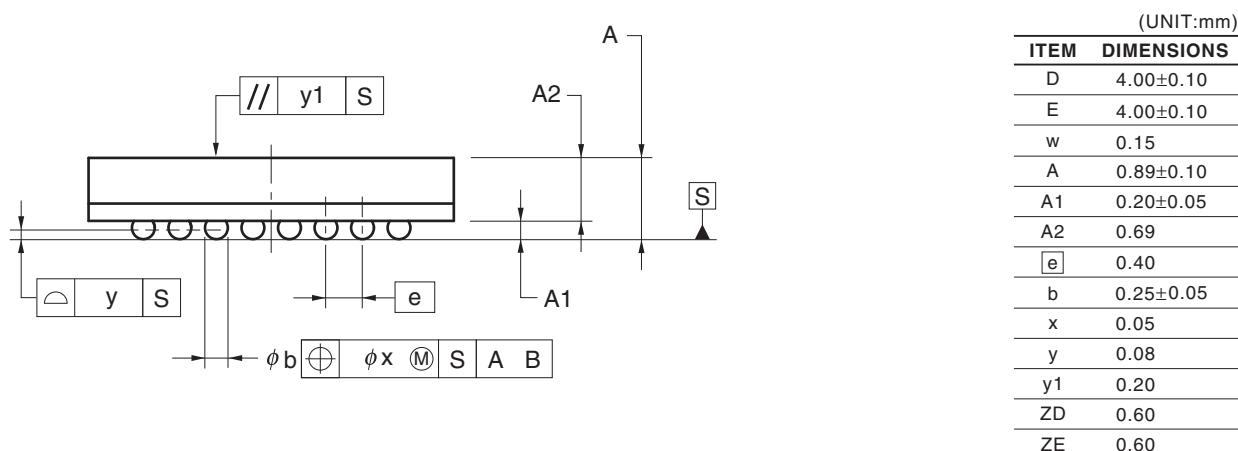
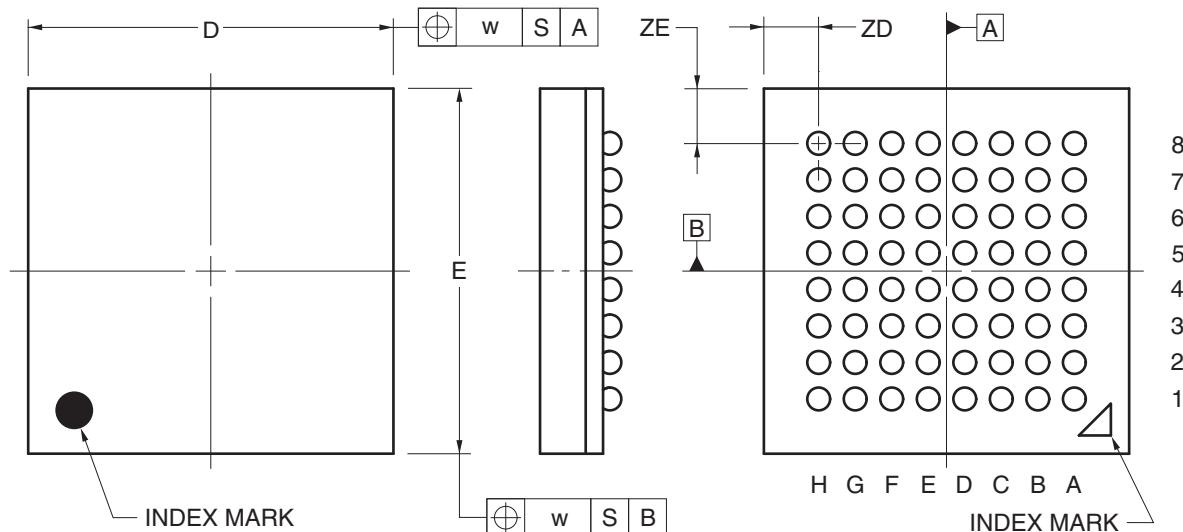
R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,

R5F101LJABG

R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,

R5F100LJGBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03

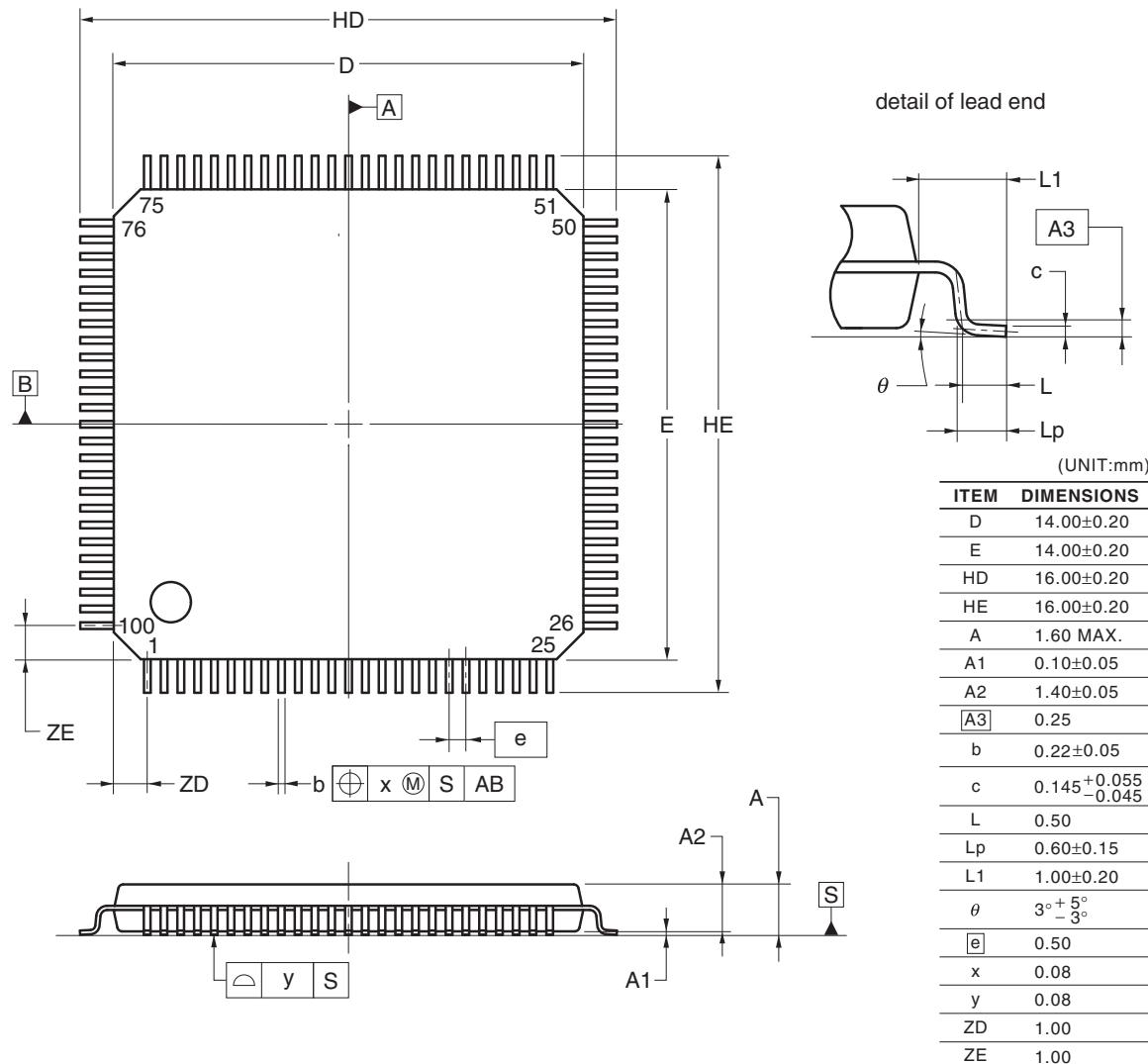


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4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
 R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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