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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100jdfa-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100jdfa-x0</a>

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0 R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0 R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0 R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	A	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0 R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(4/12)

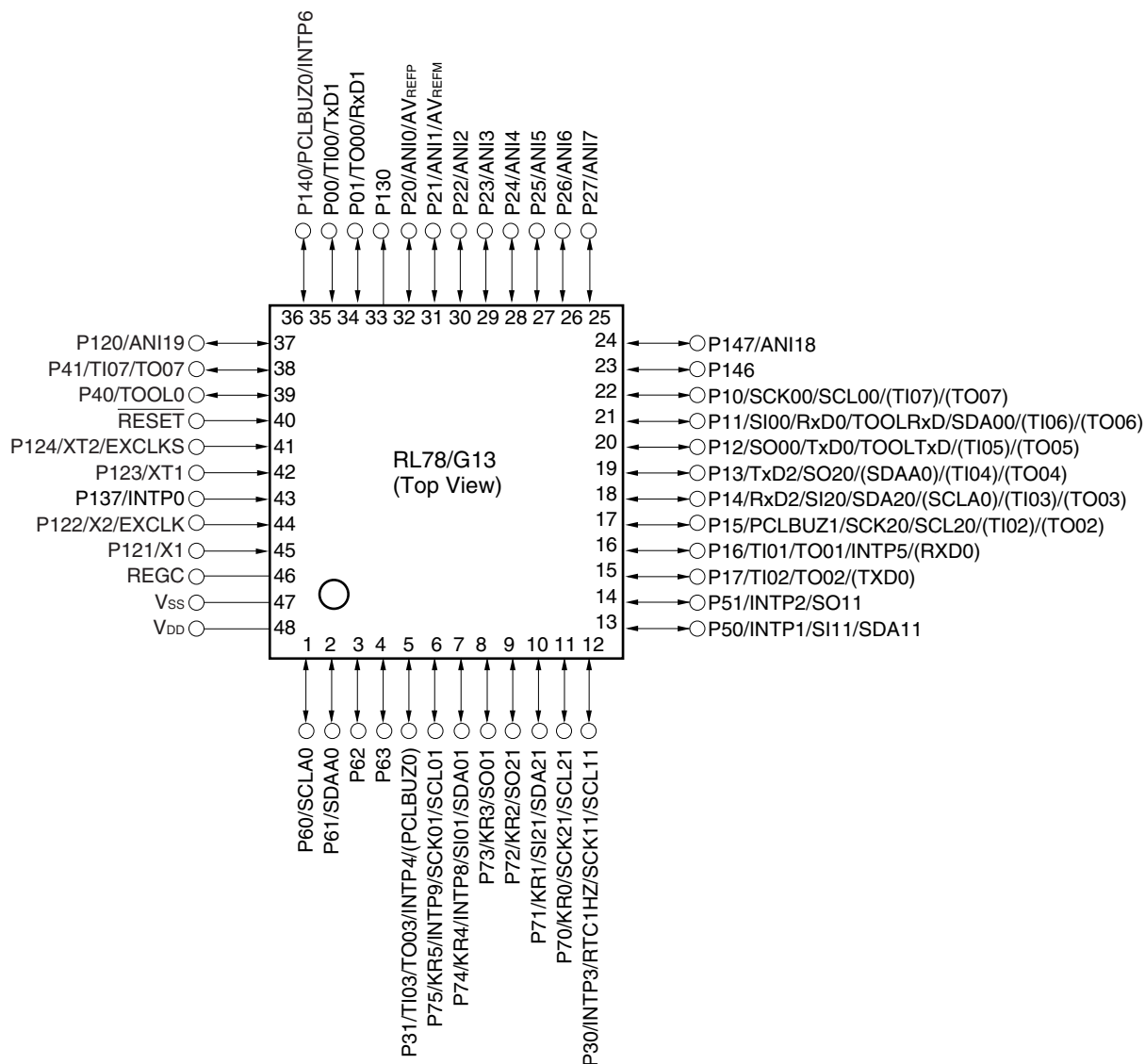
Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)	Mounted	A	R5F100FAAFP#V0, R5F100FCAFP#V0, R5F100FDAFP#V0, R5F100FEAFP#V0, R5F100FFAFP#V0, R5F100FGAFP#V0, R5F100FHAFP#V0, R5F100FJAFP#V0, R5F100FKAFP#V0, R5F100FLAFP#V0 R5F100FAAFP#X0, R5F100FCAFP#X0, R5F100FDAFP#X0, R5F100FEAFP#X0, R5F100FFAFP#X0, R5F100FGAFP#X0, R5F100FHAFP#X0, R5F100FJAFP#X0, R5F100FKAFP#X0, R5F100FLAFP#X0
			D	R5F100FADFP#V0, R5F100FCDFP#V0, R5F100FDDFP#V0, R5F100FEDFP#V0, R5F100FFDFP#V0, R5F100FGDFP#V0, R5F100FHDFP#V0, R5F100FJDFP#V0, R5F100FKDFP#V0, R5F100FLDFP#V0 R5F100FADFP#X0, R5F100FCDFP#X0, R5F100FDDFP#X0, R5F100FEDFP#X0, R5F100FFDFP#X0, R5F100FGDFP#X0, R5F100FHDFP#X0, R5F100FJDFP#X0, R5F100FKDFP#X0, R5F100FLDFP#X0
			G	R5F100FAGFP#V0, R5F100FCGFP#V0, R5F100FDGFP#V0, R5F100FEGFP#V0, R5F100FFGFP#V0, R5F100FGGFP#V0, R5F100FHGFP#V0, R5F100FJGFP#V0 R5F100FAGFP#X0, R5F100FCGFP#X0, R5F100FDGFP#X0, R5F100FEGFP#X0, R5F100FFGFP#X0, R5F100FGGFP#X0, R5F100FHGFP#X0, R5F100FJGFP#X0
		Not mounted	A	R5F101FAAFP#V0, R5F101FCAFP#V0, R5F101FDAFP#V0, R5F101FEAFP#V0, R5F101FFAFP#V0, R5F101FGAFP#V0, R5F101FHAFP#V0, R5F101FJAFP#V0, R5F101FKAFP#V0, R5F101FLAFP#V0 R5F101FAAFP#X0, R5F101FCAFP#X0, R5F101FDAFP#X0, R5F101FEAFP#X0, R5F101FFAFP#X0, R5F101FGAFP#X0, R5F101FHAFP#X0, R5F101FJAFP#X0, R5F101FKAFP#X0, R5F101FLAFP#X0
			D	R5F101FADFP#V0, R5F101FCDFP#V0, R5F101FDDFP#V0, R5F101FEDFP#V0, R5F101FFDFP#V0, R5F101FGDFP#V0, R5F101FHDFP#V0, R5F101FJDFP#V0, R5F101FKDFP#V0, R5F101FLDFP#V0 R5F101FADFP#X0, R5F101FCDFP#X0, R5F101FDDFP#X0, R5F101FEDFP#X0, R5F101FFDFP#X0, R5F101FGDFP#X0, R5F101FHDFP#X0, R5F101FJDFP#X0, R5F101FKDFP#X0, R5F101FLDFP#X0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.3.9 48-pin products

- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

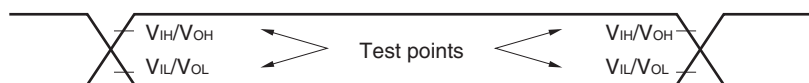
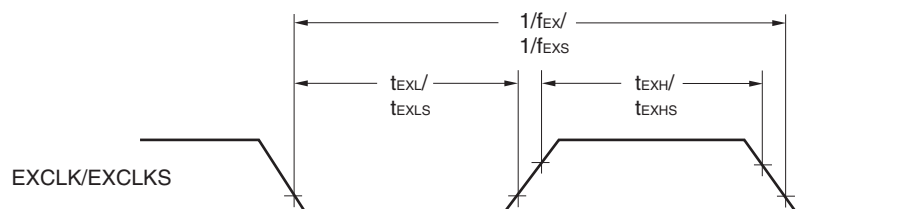
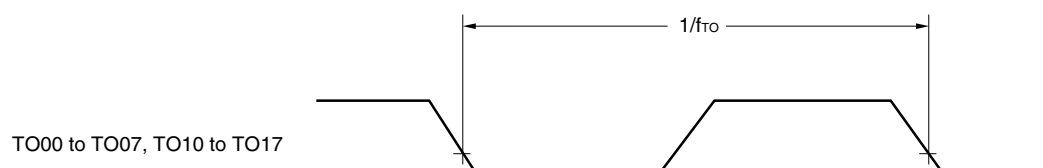
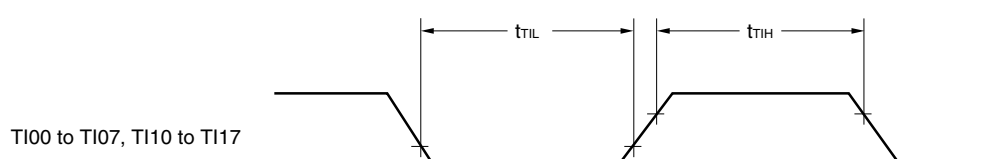
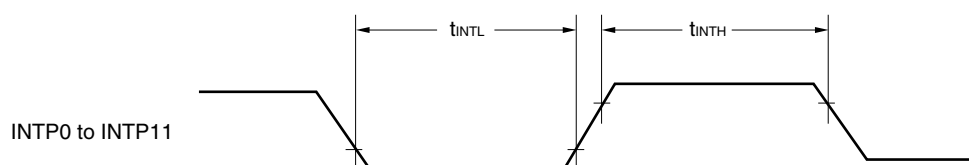
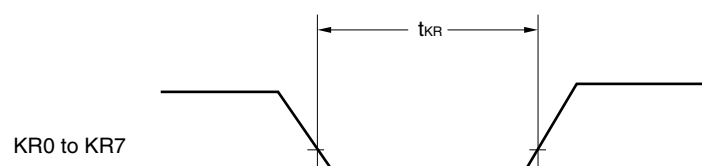
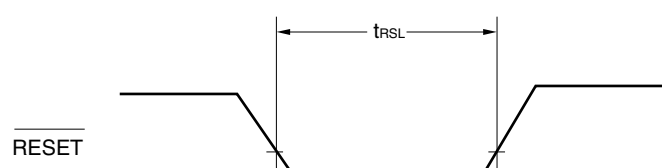
**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V) (5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I <sub>LIH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>DD0</sub>		1	μA		
	I <sub>LIH2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>DD</sub>		1	μA		
	I <sub>LIH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub>		−1	μA		
	I <sub>LIL2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>SS</sub>		−1	μA		
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub> , In input port		10	20	100	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**AC Timing Test Points****External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

- Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
- 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)**  
**(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <small>Note 5</small>	t <sub>KCY2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	20 MHz < f <sub>MCK</sub>	8/f <sub>MCK</sub>		—		—		ns
			f <sub>MCK</sub> ≤ 20 MHz	6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	16 MHz < f <sub>MCK</sub>	8/f <sub>MCK</sub>		—		—		ns
			f <sub>MCK</sub> ≤ 16 MHz	6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		6/f <sub>MCK</sub>		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 500		6/f <sub>MCK</sub> and 500		6/f <sub>MCK</sub> and 500		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 750		6/f <sub>MCK</sub> and 750		6/f <sub>MCK</sub> and 750		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		6/f <sub>MCK</sub> and 1500		6/f <sub>MCK</sub> and 1500		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 7		t <sub>KCY2</sub> /2 – 7		t <sub>KCY2</sub> /2 – 7		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 8		t <sub>KCY2</sub> /2 – 8		t <sub>KCY2</sub> /2 – 8		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 18		t <sub>KCY2</sub> /2 – 18		t <sub>KCY2</sub> /2 – 18		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		t <sub>KCY2</sub> /2 – 66		t <sub>KCY2</sub> /2 – 66		ns

(Notes, Caution, and Remarks are listed on the next page.)

## (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK2</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +20		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI2</sub>	1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO2</sub>	C = 30 pF <sup>Note 4</sup>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +44		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +75		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220	ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))



3. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> < 4.0 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.
6. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

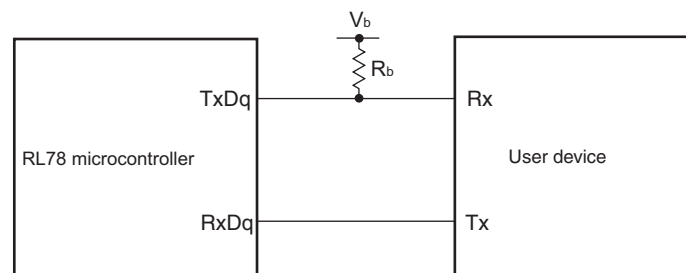
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

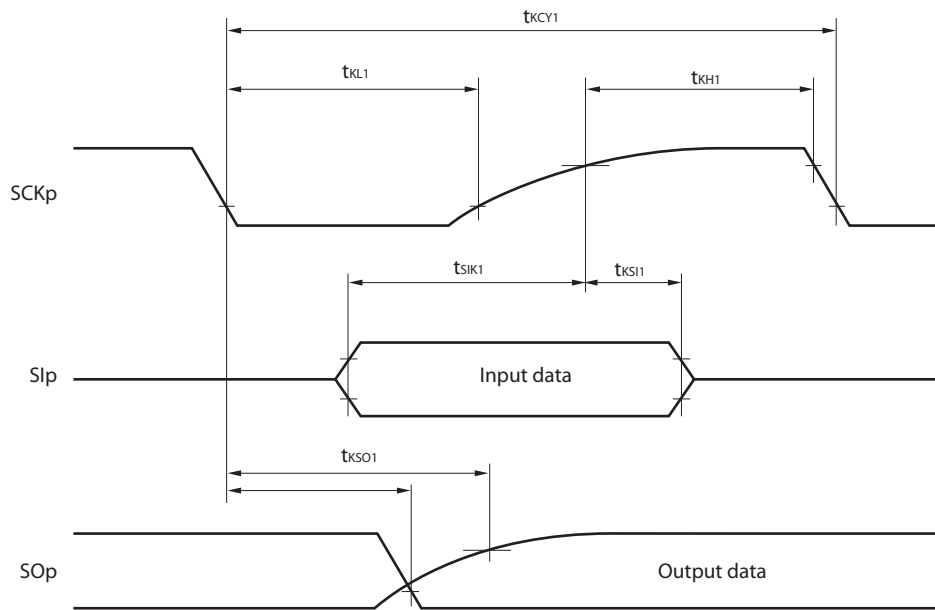
7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the Rx<sub>Dq</sub> pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the Tx<sub>Dq</sub> pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

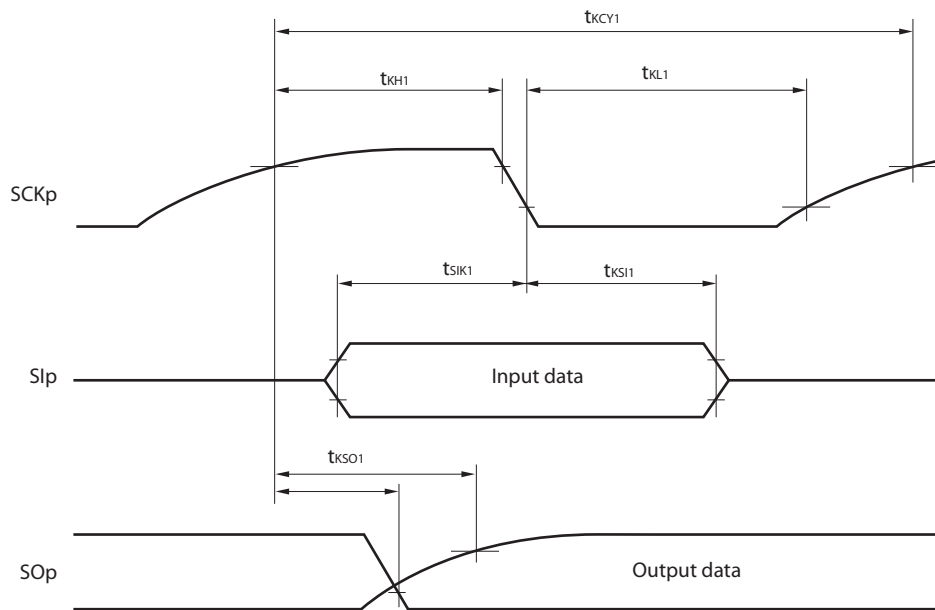
UART mode connection diagram (during communication at different potential)



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = V_{SS0} = 0\text{ V}$ ) (2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 7	f <sub>IH</sub> = 32 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.54	2.90	mA	
					V <sub>DD</sub> = 3.0 V		0.54	2.90	mA	
				f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.44	2.30	mA	
					V <sub>DD</sub> = 3.0 V		0.44	2.30	mA	
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.40	1.70	mA	
					V <sub>DD</sub> = 3.0 V		0.40	1.70	mA	
			HS (high-speed main) mode Note 7	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +25°C	Square wave input		0.30	0.57	μA	
					Resonator connection		0.49	0.76	μA	
		f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +50°C		Square wave input		0.37	1.17	μA		
				Resonator connection		0.56	1.36	μA		
		f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +70°C		Square wave input		0.53	1.97	μA		
				Resonator connection		0.72	2.16	μA		
		f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +85°C		Square wave input		0.82	3.37	μA		
				Resonator connection		1.01	3.56	μA		
		f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +105°C	Square wave input		3.01	15.37	μA			
			Resonator connection		3.20	15.56	μA			
	I <sub>DD3</sub> <sup>Note 6</sup>	STOP mode <sup>Note 8</sup>	T <sub>A</sub> = −40°C					0.18	0.50	μA
			T <sub>A</sub> = +25°C					0.23	0.50	μA
			T <sub>A</sub> = +50°C					0.30	1.10	μA
			T <sub>A</sub> = +70°C					0.46	1.90	μA
			T <sub>A</sub> = +85°C					0.75	3.30	μA
			T <sub>A</sub> = +105°C					2.94	15.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.  
 HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
  8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

## (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V})$ 

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	$t_{\text{KCY}1}$	$t_{\text{KCY}1} \geq 4/f_{\text{CLK}}$	250		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	500		ns
SCKp high-/low-level width	$t_{\text{KH}1}$ , $t_{\text{KL}1}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$t_{\text{KCY}1}/2 - 24$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$t_{\text{KCY}1}/2 - 36$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	$t_{\text{KCY}1}/2 - 76$		ns
Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>	$t_{\text{SIK}1}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note 2</sup>	$t_{\text{KSI}1}$		38		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 3</sup>	$t_{\text{KSO}1}$	$C = 30\text{ pF}$ <sup>Note 4</sup>		50	ns

- Notes**
1. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp setup time becomes “to SCKp $\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  2. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The Slp hold time becomes “from SCKp $\downarrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  3. When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ . The delay time to SOp output becomes “from SCKp $\uparrow$ ” when  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 1$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 0$ .
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
  2.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

5. The smaller maximum transfer rate derived by using  $f_{MCK}/12$  or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when  $2.4\text{ V} \leq V_{DD0} < 3.3\text{ V}$  and  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

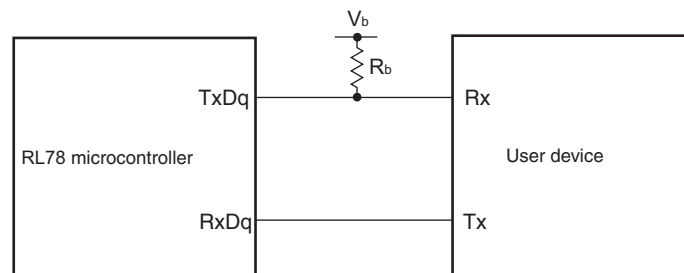
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $V_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(3) When reference voltage (+) =  $V_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) =  $V_{SS}$  (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ , Reference voltage (–) =  $V_{SS}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	$\pm 7.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	$E_{ZS}$	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	$E_{FS}$	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 4.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI0 to ANI14		0		$V_{DD}$	V
		ANI16 to ANI26		0		$EV_{DD0}$	V
		Internal reference voltage output ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{BGR}$ <sup>Note 3</sup>			V
		Temperature sensor output voltage ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{TMPS25}$ <sup>Note 3</sup>			V

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

## 3.8 Flash Memory Programming Characteristics

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	fCLK	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites <small>Notes 1,2,3</small>	C <sub>enwr</sub>	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	1,000			Times
Number of data flash rewrites <small>Notes 1,2,3</small>		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
  2. When using flash memory programmer and Renesas Electronics self programming library.
  3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
  4. This temperature is the average value at which data are retained.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} = V_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = V_{SS0} = V_{SS1} = 0\text{ V}$ )**

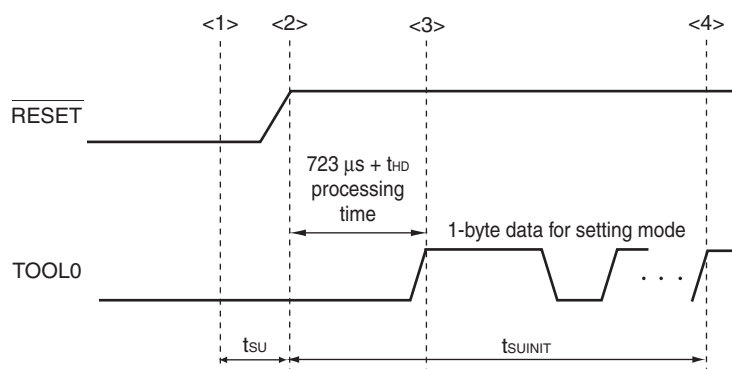
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps



## 3.10 Timing of Entry to Flash Memory Programming Modes

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset must be released before the external reset is released.	1			ms



&lt;1&gt; The low level is input to the TOOL0 pin.

&lt;2&gt; The external reset is released (POR and LVD reset must be released before the external reset is released.).

&lt;3&gt; The TOOL0 pin is set to the high level.

&lt;4&gt; Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

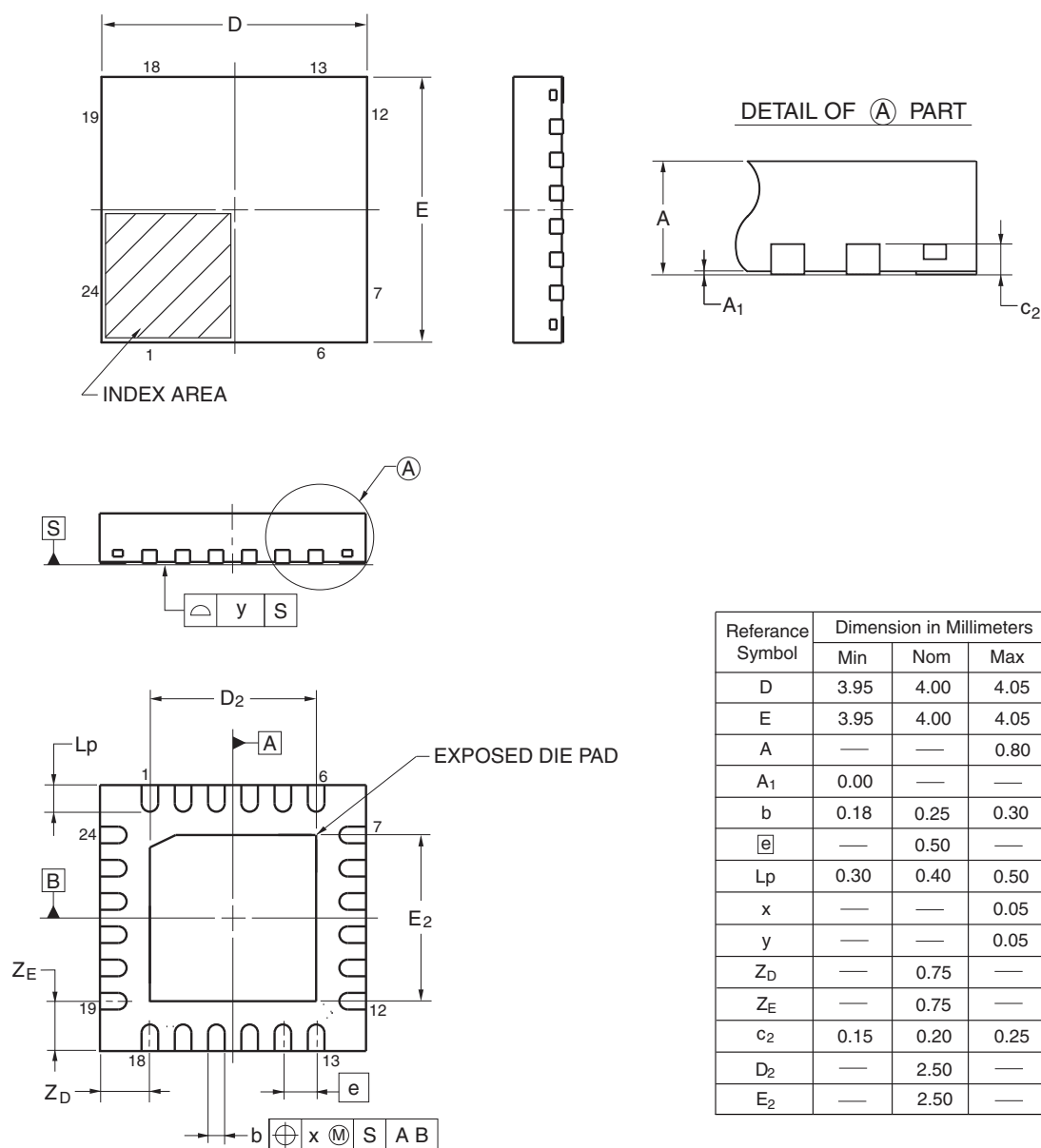
$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

## 4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA  
 R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA  
 R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA  
 R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA  
 R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

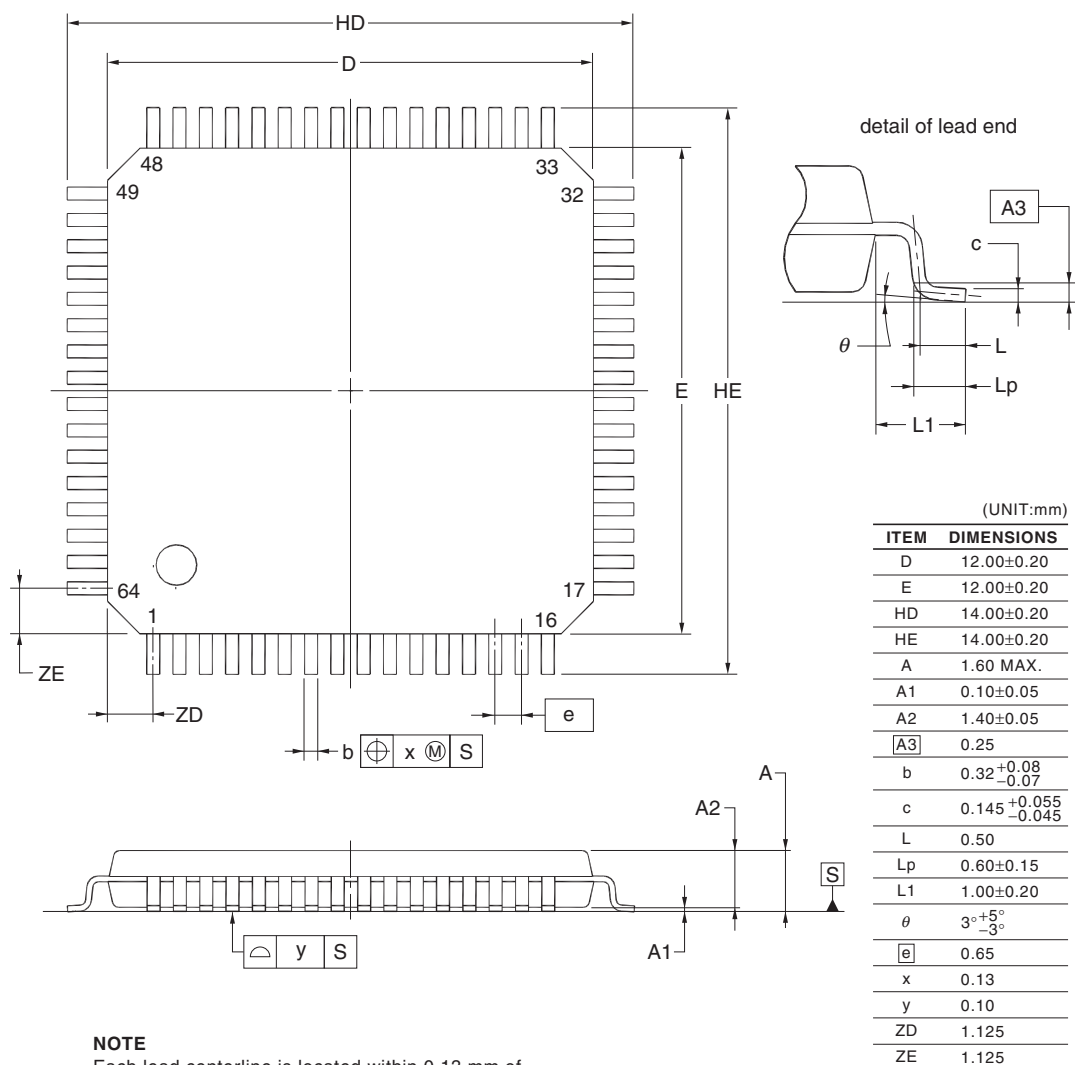
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04



## 4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAF, A,  
 R5F100LKAFA, R5F100LLAFA  
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAF, A,  
 R5F101LKAFA, R5F101LLAFA  
 R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LHDFA, R5F100LJDFA,  
 R5F100LK DFA, R5F100LLDFA  
 R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LHDFA, R5F101LJDFA,  
 R5F101LK DFA, R5F101LLDFA  
 R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,  
 R5F100LJGFA

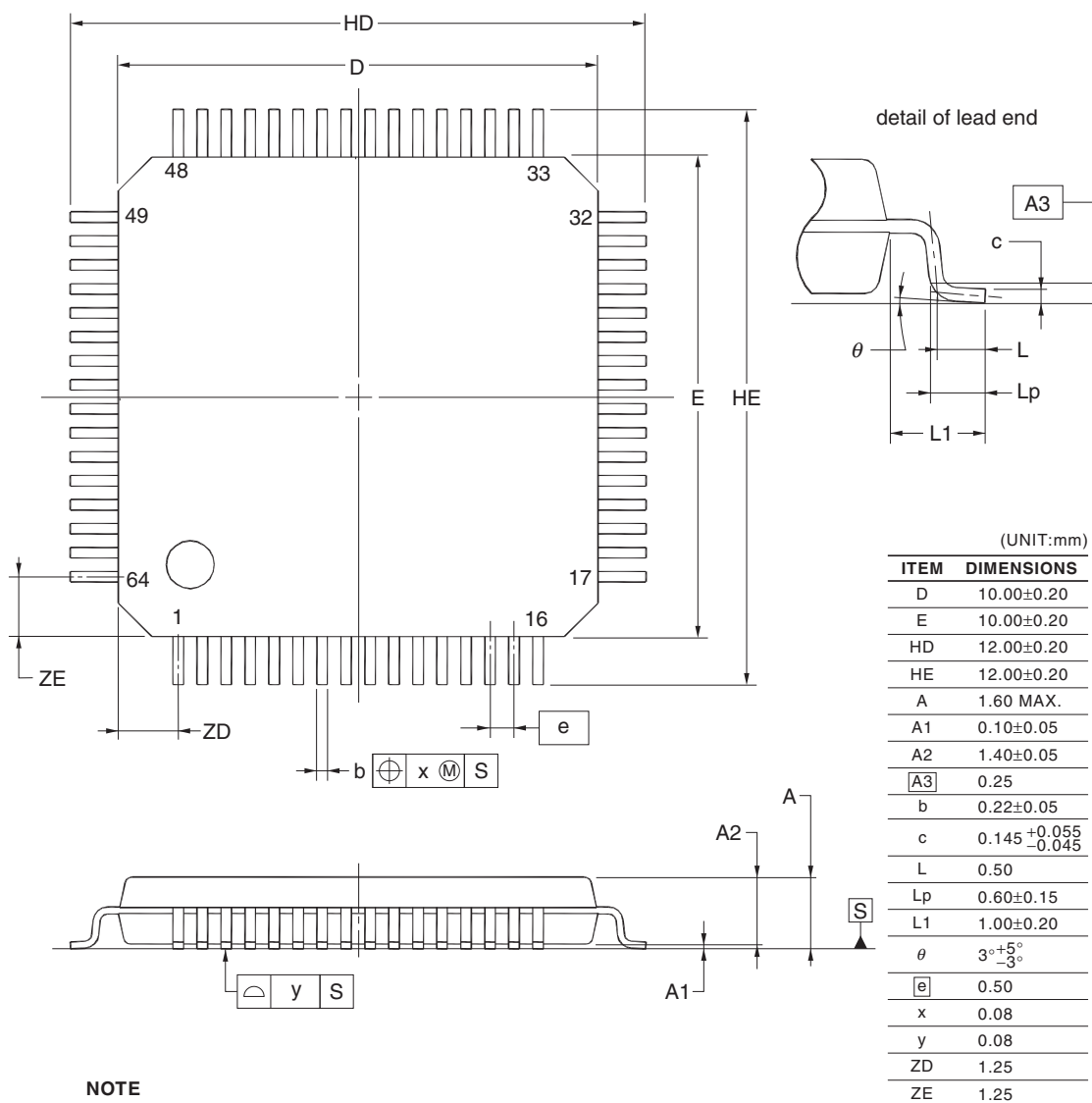
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

**NOTE**

Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,  
 R5F100LKAFB, R5F100LLAFB  
 R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB,  
 R5F101LJAFB, R5F101LKAFB, R5F101LLAFB  
 R5F100LCDFB, R5F100LDDFB, R5F100LEDDB, R5F100LDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,  
 R5F100LKDFB, R5F100LLDFB  
 R5F101LCDFB, R5F101LDDFB, R5F101LEDDB, R5F101LDFB, R5F101LGDFB, R5F101LHDFB,  
 R5F101LJDFB, R5F101LKDFB, R5F101LLDFB  
 R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB,  
 R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



#### NOTE

Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (2/2)
		109	Addition of (1) I <sup>2</sup> C standard mode
		111	Addition of (2) I <sup>2</sup> C fast mode
		112	Addition of (3) I <sup>2</sup> C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)