# Renesas Electronics America Inc - R5F100LCAFB#30 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LFQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lcafb-30 |

**Table 1-1. List of Ordering Part Numbers**

(5/12)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 48 pins | 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch) | Mounted | A | R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0<br>R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0 |
| | | | D | R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0<br>R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0 |
| | | | G | R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0<br>R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0 |
| | | Not mounted | A | R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0<br>R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0 |
| | | | D | R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0<br>R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0 |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

**Table 1-1. List of Ordering Part Numbers**

(9/12)

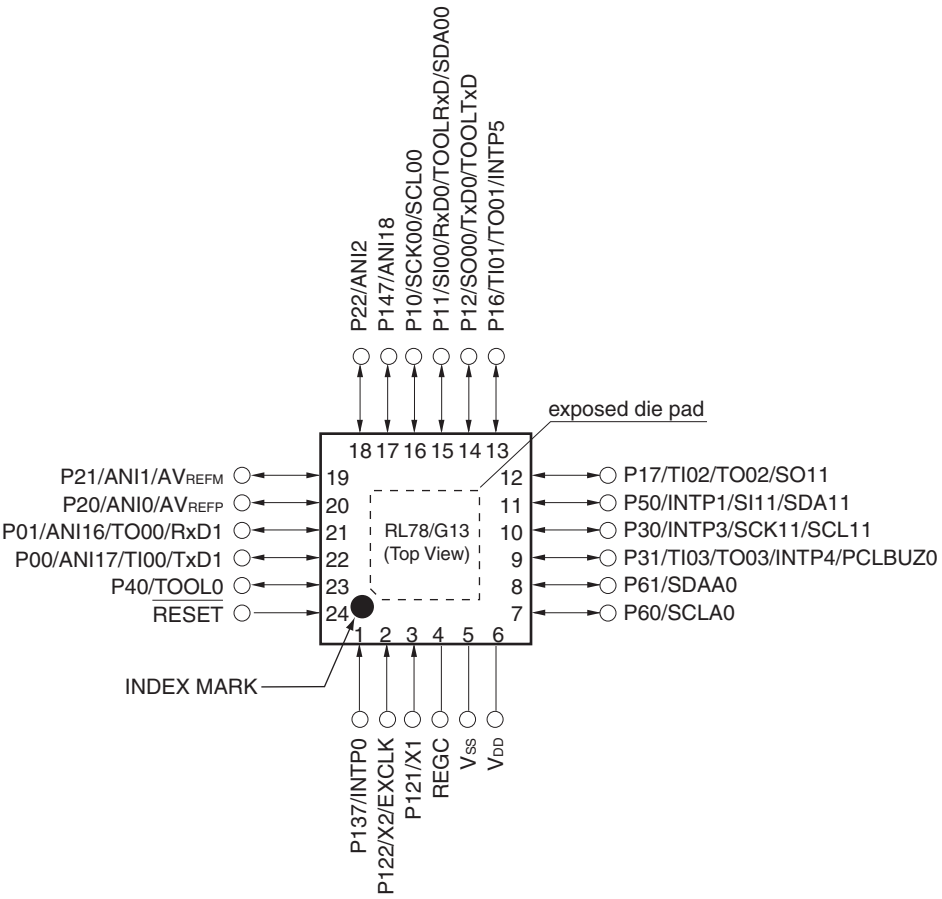
| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 64 pins | 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch) | Mounted | A | R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0<br>R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0 |
| | | | D | R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDFB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0<br>R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDFB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0 |
| | | | G | R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0<br>R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0<br>R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0<br>R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0 |
| | | Not mounted | A | R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0<br>R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0 |
| | | | D | R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDFB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0<br>R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDFB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0 |
| | 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch) | Mounted | A | R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0<br>R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0 |
| | | | G | R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGBG#U0, R5F100LGGBG#U0, R5F100LHGBG#U0, R5F100LJGBG#U0<br>R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGBG#W0, R5F100LGGBG#W0, R5F100LHGBG#W0, R5F100LJGBG#W0 |
| | | Not mounted | A | R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0<br>R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0 |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

### 1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)



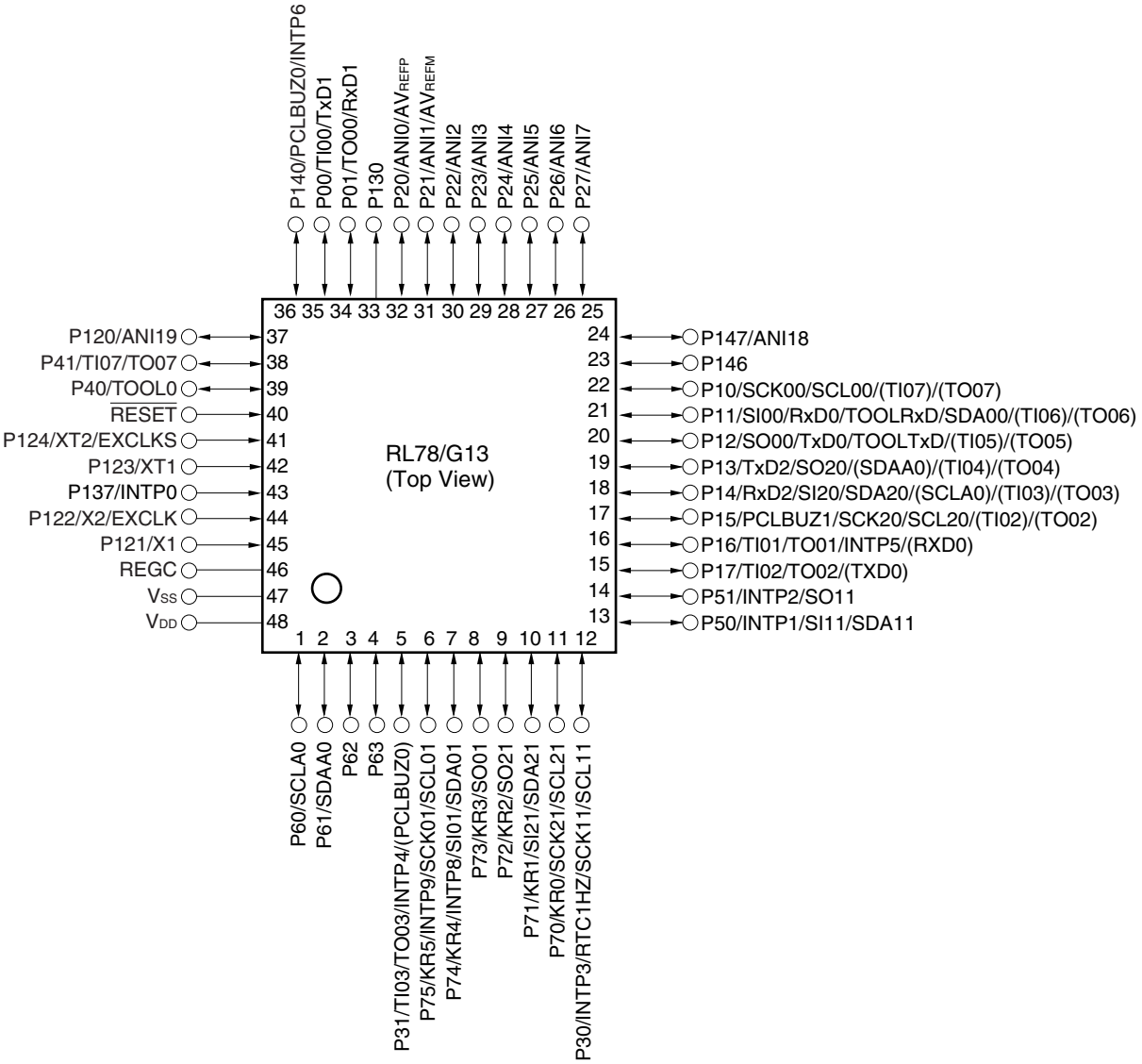

**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** It is recommended to connect an exposed die pad to $V_{SS}$.

### 1.3.9 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)




**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 20-pin | | 24-pin | | 25-pin | | 30-pin | | 32-pin | | 36-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F1006x | R5F1016x | R5F1007x | R5F1017x | R5F1008x | R5F1018x | R5F100Ax | R5F101Ax | R5F100Bx | R5F101Bx | R5F100Cx | R5F101Cx |
| Code flash memory (KB) | | 16 to 64 | | 16 to 64 | | 16 to 64 | | 16 to 128 | | 16 to 128 | | 16 to 128 | |
| Data flash memory (KB) | | 4 | – | 4 | – | 4 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 4 Note1 | | 2 to 4 Note1 | | 2 to 4 Note1 | | 2 to 12 Note1 | | 2 to 12 Note1 | | 2 to 12 Note1 | |
| Address space | | 1 MB | | | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | | | |
| Subsystem clock | | – | | | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | | | | | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | | | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | | | |
| I/O port | Total | 16 | | 20 | | 21 | | 26 | | 28 | | 32 | |
| | CMOS I/O | 13<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 5) | | 15<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 6) | | 15<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 6) | | 21<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 9) | | 22<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 9) | | 26<br>(N-ch O.D. I/O [$V_{DD}$ withstand voltage]: 10) | |
| | CMOS input | 3 | | 3 | | 3 | | 3 | | 3 | | 3 | |
| | CMOS output | – | | – | | 1 | | – | | – | | – | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | – | | 2 | | 2 | | 2 | | 3 | | 3 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel Note 2 | | | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | | | |
| | Timer output | 3 channels<br>(PWM outputs: 2 Note 3) | | 4 channels<br>(PWM outputs: 3 Note 3) | | | | 4 channels (PWM outputs: 3 Note 3),<br>8 channels (PWM outputs: 7 Note 3) Note 4 | | | | | |
| | RTC output | – | | | | | | | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**2.** Only the constant-period interrupt function when the low-speed on-chip oscillator clock ($f_{IL}$) is selected

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | $I_{LIH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{DD0}$ | | | | 1 | μA |
| | $I_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I = V_{DD}$ | | | | 1 | μA |
| | $I_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I = V_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | $I_{LIL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{SS0}$ | | | | –1 | μA |
| | $I_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | $V_I = V_{SS}$ | | | | –1 | μA |
| | $I_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | $V_I = V_{SS}$ | In input port or external clock input | | | –1 | μA |
| | | | | In resonator connection | | | –10 | μA |
| On-chip pll-up resistance | $R_U$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | $V_I = EV_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

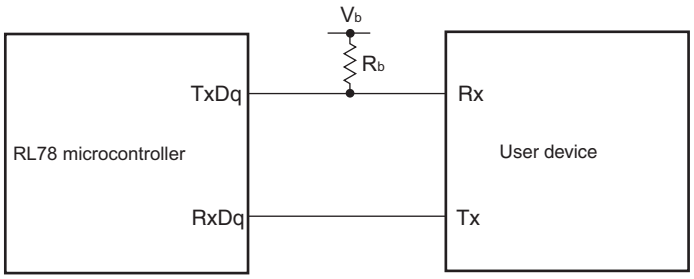
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**7.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**



## 2.5.2 Serial interface IICA

### (1) $I^2C$ standard mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Standard mode: $f_{CLK}$ ≥ 1 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 100 | 0 | 100 | 0 | 100 | kHz |
| | | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | — | | 0 | 100 | 0 | 100 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Hold time when SCLA0 = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |
| Hold time when SCLA0 = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 250 | | 250 | | 250 | | ns |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 250 | | 250 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 3.45 | 0 | 3.45 | 0 | 3.45 | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 0 | 3.45 | 0 | 3.45 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.0 | | 4.0 | | 4.0 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.0 | | 4.0 | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 4.7 | | 4.7 | | 4.7 | | μs |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | 4.7 | | 4.7 | | μs |

(**Notes**, **Caution** and **Remark** are listed on the next page.)

### (3) $I^2C$ fast mode plus

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode plus: $f_{CLK}$ ≥ 10 MHz | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | 1000 | — | | — | | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 50 | | — | | — | | μs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0 | 0.45 | — | | — | | μs |
| Setup time of stop condition | $t_{SU:STO}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.26 | | — | | — | | μs |
| Bus-free time | $t_{BUF}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 0.5 | | — | | — | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

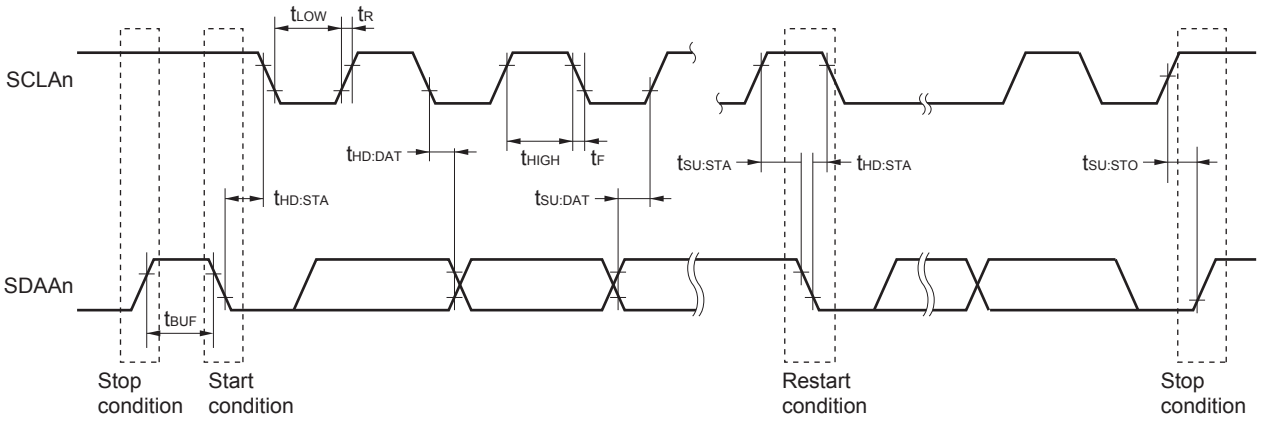
<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: $C_b$ = 120 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**




**Remark** n = 0, 1

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error Note 1 | AINL | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | 1.2 | ±10.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | μs |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Full-scale error Notes 1, 2 | $E_{FS}$ | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±0.85 | %FSR |
| Integral linearity error Note 1 | ILE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±6.5 | LSB |
| Differential linearity error Note 1 | DLE | 10-bit resolution | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V Note 3 | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI26 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$ Note 4 | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$ Note 4 | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

**4.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 32 MHz

$2.4\ V \leq V_{DD} \leq 5.5\ V$@1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

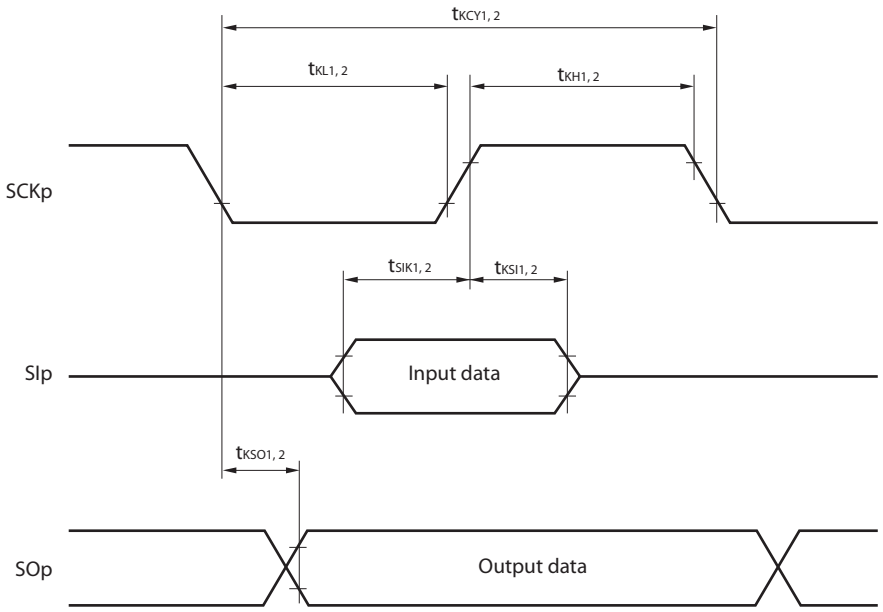
**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

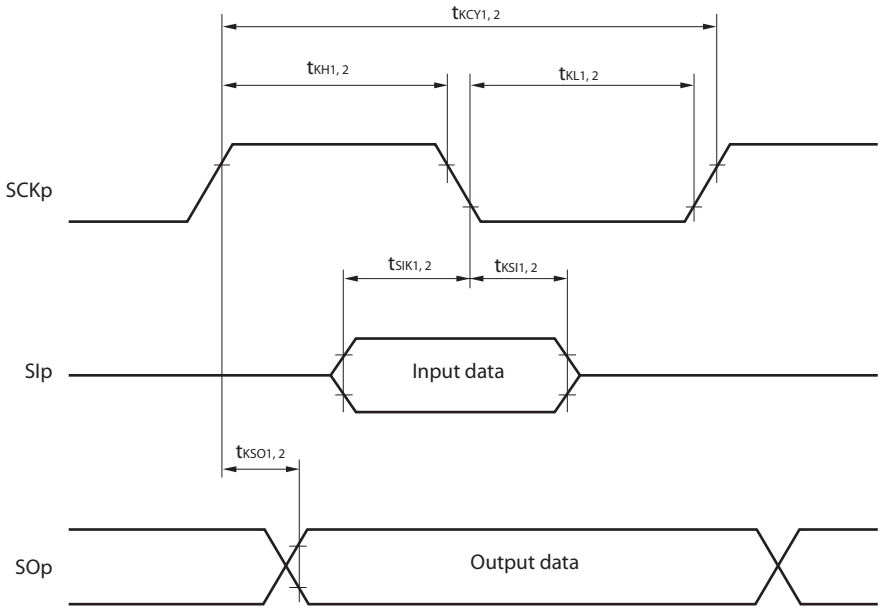
**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A$ = 25°C

**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (during communication at same potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

**2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**(4) During communication at same potential (simplified $I^2C$ mode)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note2 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

**(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Transmission | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | **Note 1** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 1.4 kΩ, $V_b$ = 2.7 V | | 2.6 Note 2 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | **Note 3** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 2.7 kΩ, $V_b$ = 2.3 V | | 1.2 Note 4 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | **Note 5** | bps |
| | | | | Theoretical value of the maximum transfer rate $C_b$ = 50 pF, $R_b$ = 5.5 kΩ, $V_b$ = 1.6 V | | 0.43 Note 6 | Mbps |

**Notes 1.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V and 2.7 V ≤ $V_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**2.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

**3.** The smaller maximum transfer rate derived by using $f_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.4 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time Note 1 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V Note 2 | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) Note2 | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) Note 3 | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output Note 4 | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**(3) When reference voltage (+) = $V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = $V_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{DD}$, Reference voltage (–) = $V_{SS}$)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution<br>Target pin: ANI0 to ANI14, ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| | | 10-bit resolution<br>Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode) | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.375 | | 39 | μs |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.5625 | | 39 | μs |
| | | | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±4.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI0 to ANI14 | | 0 | | $V_{DD}$ | V |
| | | ANI16 to ANI26 | | 0 | | $EV_{DD0}$ | V |
| | | Internal reference voltage output (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{BGR}$[Note 3] | | | V |
| | | Temperature sensor output voltage (2.4 V ≤ $V_{DD}$ ≤ 5.5 V, HS (high-speed main) mode) | | $V_{TMPS25}$[Note 3] | | | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

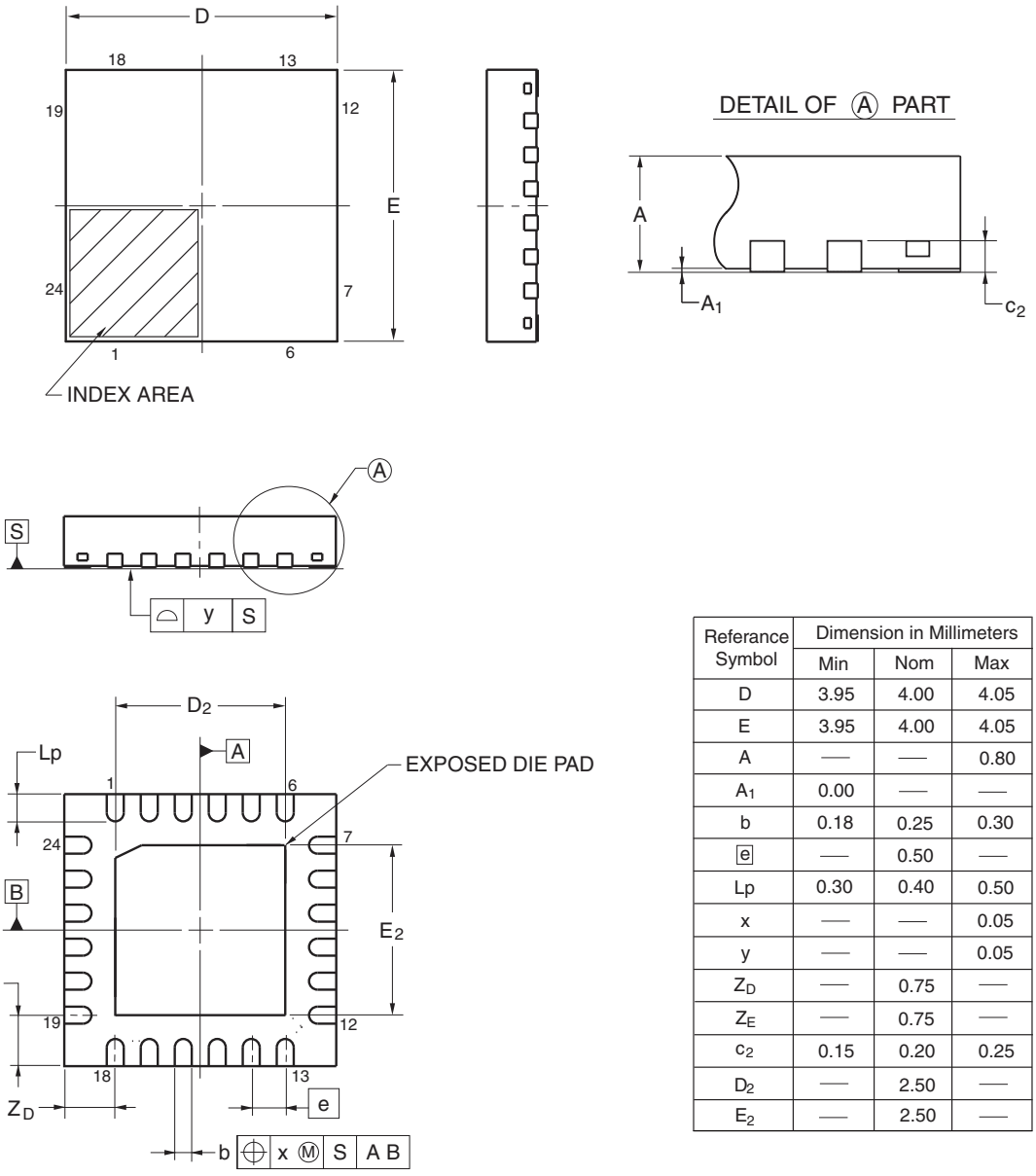
**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

## 4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |

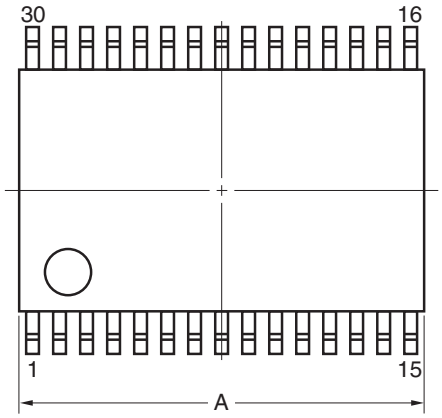



| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 3.95 | 4.00 | 4.05 |
| E | 3.95 | 4.00 | 4.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 2.50 | — |
| $E_2$ | — | 2.50 | — |

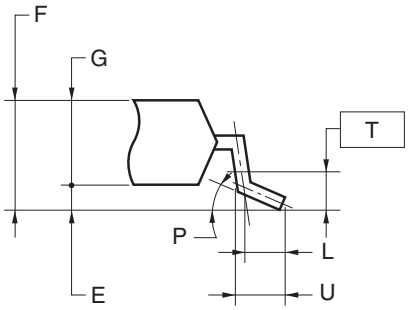
## 4.4 30-pin Products

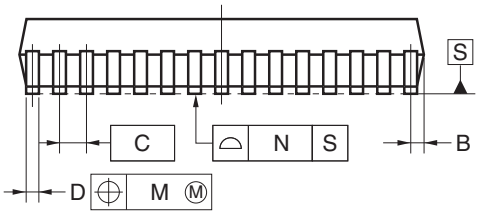
R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
R5F100AAGSP, R5F100ACGSP, R5F100ADGSP,R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

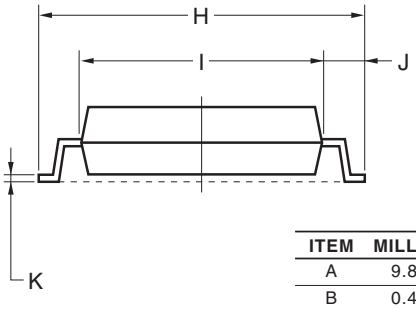
| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18 |




detail of lead end



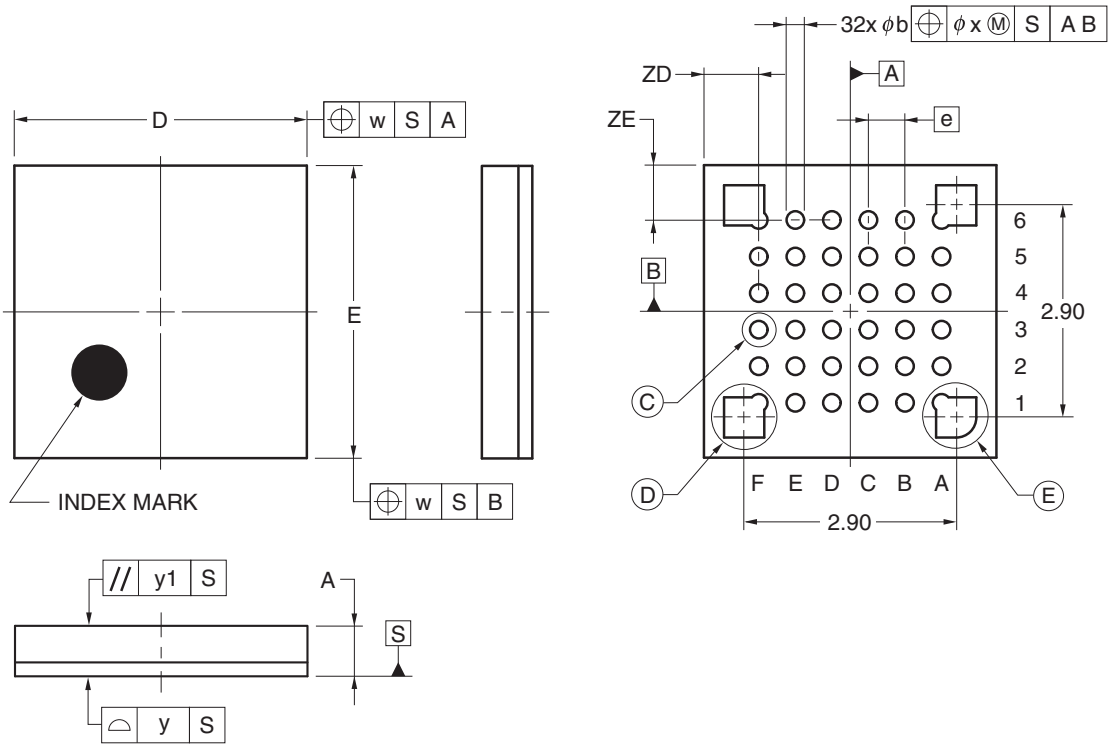

**NOTE**
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

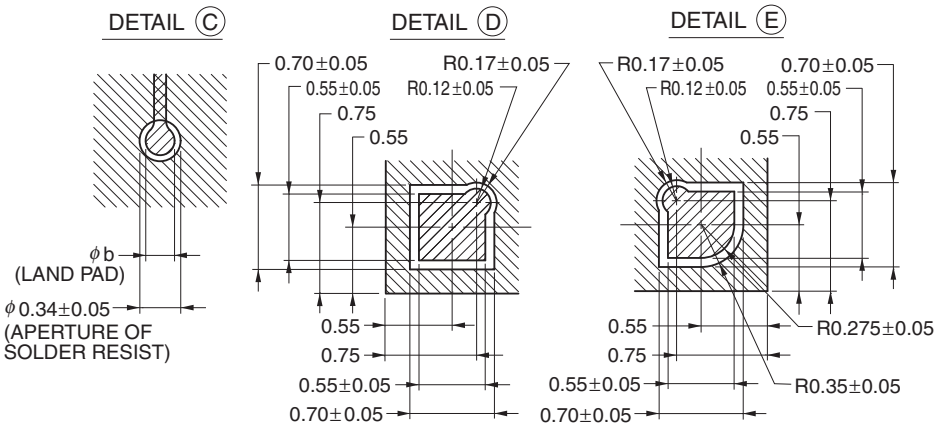
| ITEM | MILLIMETERS |
|---|---|
| A | 9.85±0.15 |
| B | 0.45 MAX. |
| C | 0.65 (T.P.) |
| D | $0.24^{+0.08}_{-0.07}$ |
| E | 0.1±0.05 |
| F | 1.3±0.1 |
| G | 1.2 |
| H | 8.1±0.2 |
| I | 6.1±0.2 |
| J | 1.0±0.2 |
| K | 0.17±0.03 |
| L | 0.5 |
| M | 0.13 |
| N | 0.10 |
| P | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| T | 0.25 |
| U | 0.6±0.15 |

## 4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA36-4x4-0.50 | PWLG0036KA-A | P36FC-50-AA4-2 | 0.023 |



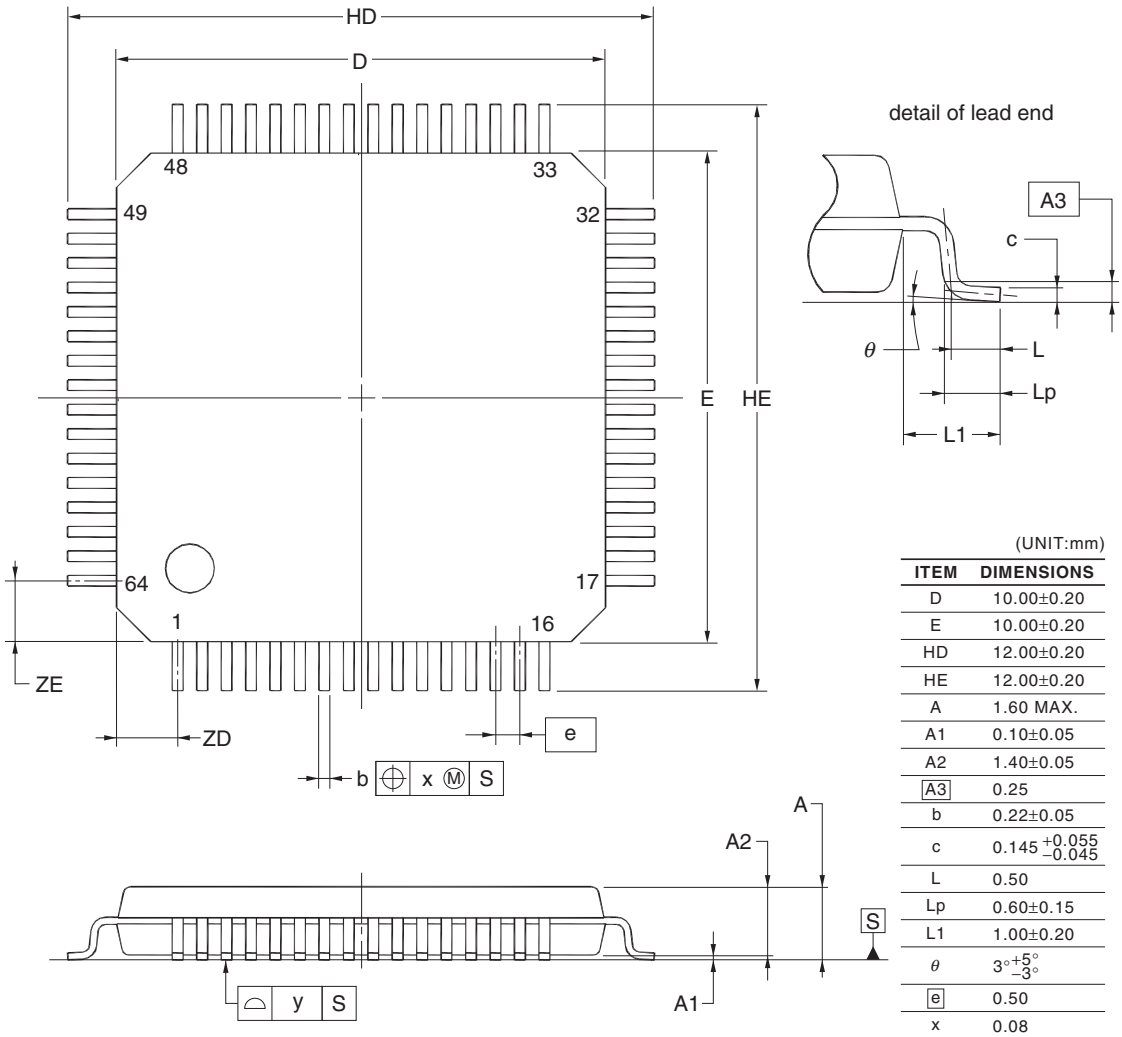




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 4.00±0.10 |
| E | 4.00±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69±0.07 |
| b | 0.24±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.75 |
| ZE | 0.75 |

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB, R5F100LKDFB, R5F100LLDFB
R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB, R5F101LKDFB, R5F101LLDFB
R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB, R5F100LJGFB

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-LFQFP64-10x10-0.50 | PLQP0064KF-A | P64GB-50-UEU-2 | 0.35 |




(UNIT:mm)

| ITEM | DIMENSIONS |
|---|---|
| D | 10.00±0.20 |
| E | 10.00±0.20 |
| HD | 12.00±0.20 |
| HE | 12.00±0.20 |
| A | 1.60 MAX. |
| A1 | 0.10±0.05 |
| A2 | 1.40±0.05 |
| A3 | 0.25 |
| b | 0.22±0.05 |
| c | $0.145^{+0.055}_{-0.045}$ |
| L | 0.50 |
| Lp | 0.60±0.15 |
| L1 | 1.00±0.20 |
| θ | $3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$ |
| e | 0.50 |
| x | 0.08 |
| y | 0.08 |
| ZD | 1.25 |
| ZE | 1.25 |

**NOTE**
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.