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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

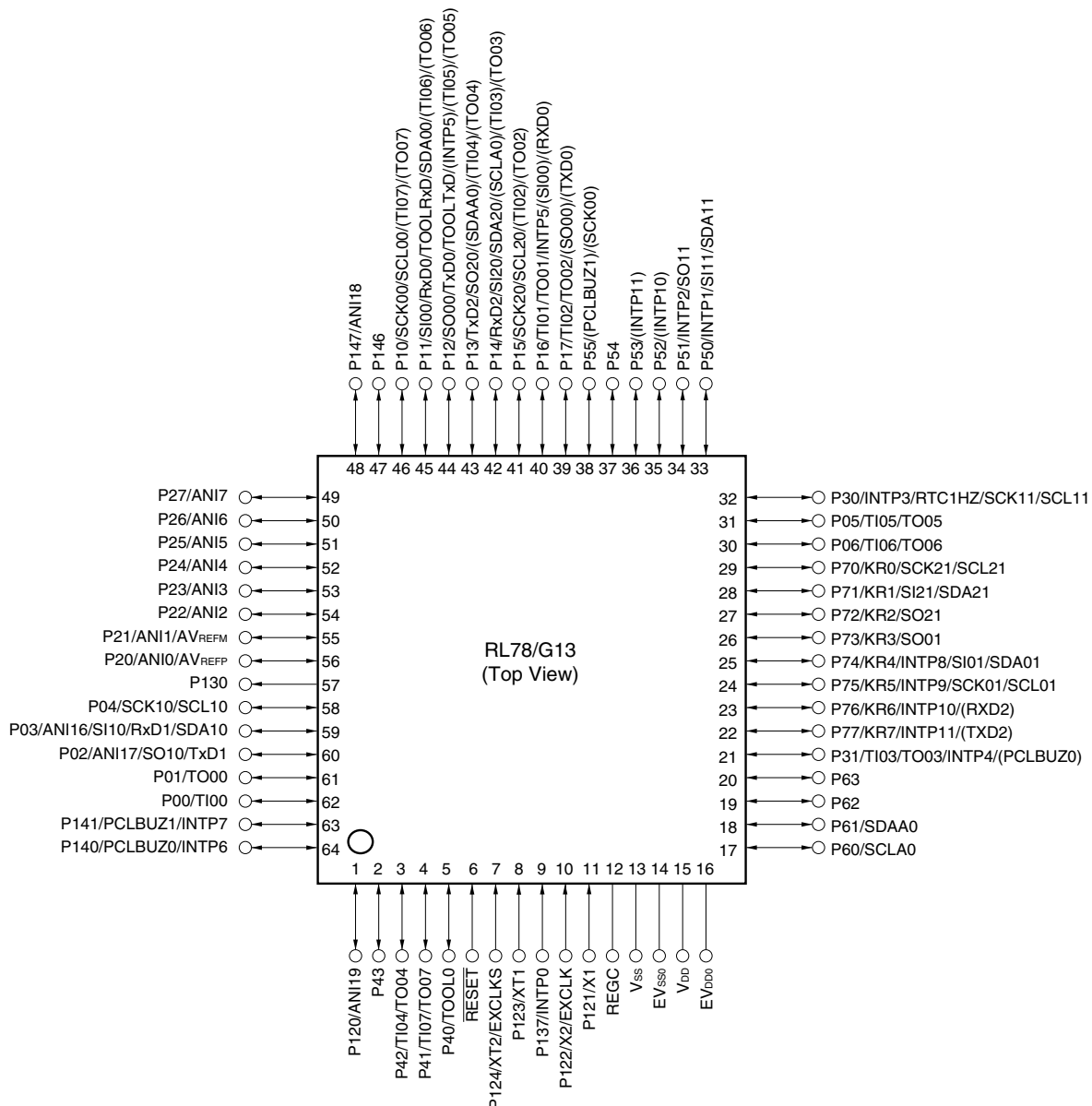| Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lcgfa-v0

Table 1-1. List of Ordering Part Numbers

(5/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0 R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0
			D	R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0 R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0
			G	R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0 R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0
		Not mounted	A	R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0 R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0
			D	R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0 R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.11　64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

Top side pins (48–33):

- P147/ANI18 (48)
- P146 (47)
- P10/SCK00/SCL00/(TI07)/(TO07) (46)
- P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06) (45)
- P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05) (44)
- P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04) (43)
- P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03) (42)
- P15/SCK20/SCL20/(TI02)/(TO02) (41)
- P16/TI01/TO01/INTP5/(SI00)/(RXD0) (40)
- P17/TI02/TO02/(SO00)/(TXD0) (39)
- P55/(PCLBUZ1)/(SCK00) (38)
- P54 (37)
- P53/(INTP11) (36)
- P52/(INTP10) (35)
- P51/INTP2/SO11 (34)
- P50/INTP1/SI11/SDA11 (33)

Left side pins:

- P27/ANI7 (49)
- P26/ANI6 (50)
- P25/ANI5 (51)
- P24/ANI4 (52)
- P23/ANI3 (53)
- P22/ANI2 (54)
- P21/ANI1/AV$_{REFM}$ (55)
- P20/ANI0/AV$_{REFP}$ (56)
- P130 (57)
- P04/SCK10/SCL10 (58)
- P03/ANI16/SI10/RxD1/SDA10 (59)
- P02/ANI17/SO10/TxD1 (60)
- P01/TO00 (61)
- P00/TI00 (62)
- P141/PCLBUZ1/INTP7 (63)
- P140/PCLBUZ0/INTP6 (64)

RL78/G13
(Top View)

Right side pins:

- P30/INTP3/RTC1HZ/SCK11/SCL11 (32)
- P05/TI05/TO05 (31)
- P06/TI06/TO06 (30)
- P70/KR0/SCK21/SCL21 (29)
- P71/KR1/SI21/SDA21 (28)
- P72/KR2/SO21 (27)
- P73/KR3/SO01 (26)
- P74/KR4/INTP8/SI01/SDA01 (25)
- P75/KR5/INTP9/SCK01/SCL01 (24)
- P76/KR6/INTP10/(RXD2) (23)
- P77/KR7/INTP11/(TXD2) (22)
- P31/TI03/TO03/INTP4/(PCLBUZ0) (21)
- P63 (20)
- P62 (19)
- P61/SDAA0 (18)
- P60/SCLA0 (17)

Bottom side pins (1–16):

- P120/ANI19 (1)
- P43 (2)
- P42/TI04/TO04 (3)
- P41/TI07/TO07 (4)
- P40/TOOL0 (5)
- RESET (6)
- P124/XT2/EXCLKS (7)
- P123/XT1 (8)
- P137/INTP0 (9)
- P122/X2/EXCLK (10)
- P121/X1 (11)
- REGC (12)
- V$_{SS}$ (13)
- EV$_{SS0}$ (14)
- V$_{DD}$ (15)
- EV$_{DD0}$ (16)

Cautions 1. Make EV$_{SS0}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4　Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins and connect the V$_{SS}$ and EV$_{SS0}$ pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8　Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.13 100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)
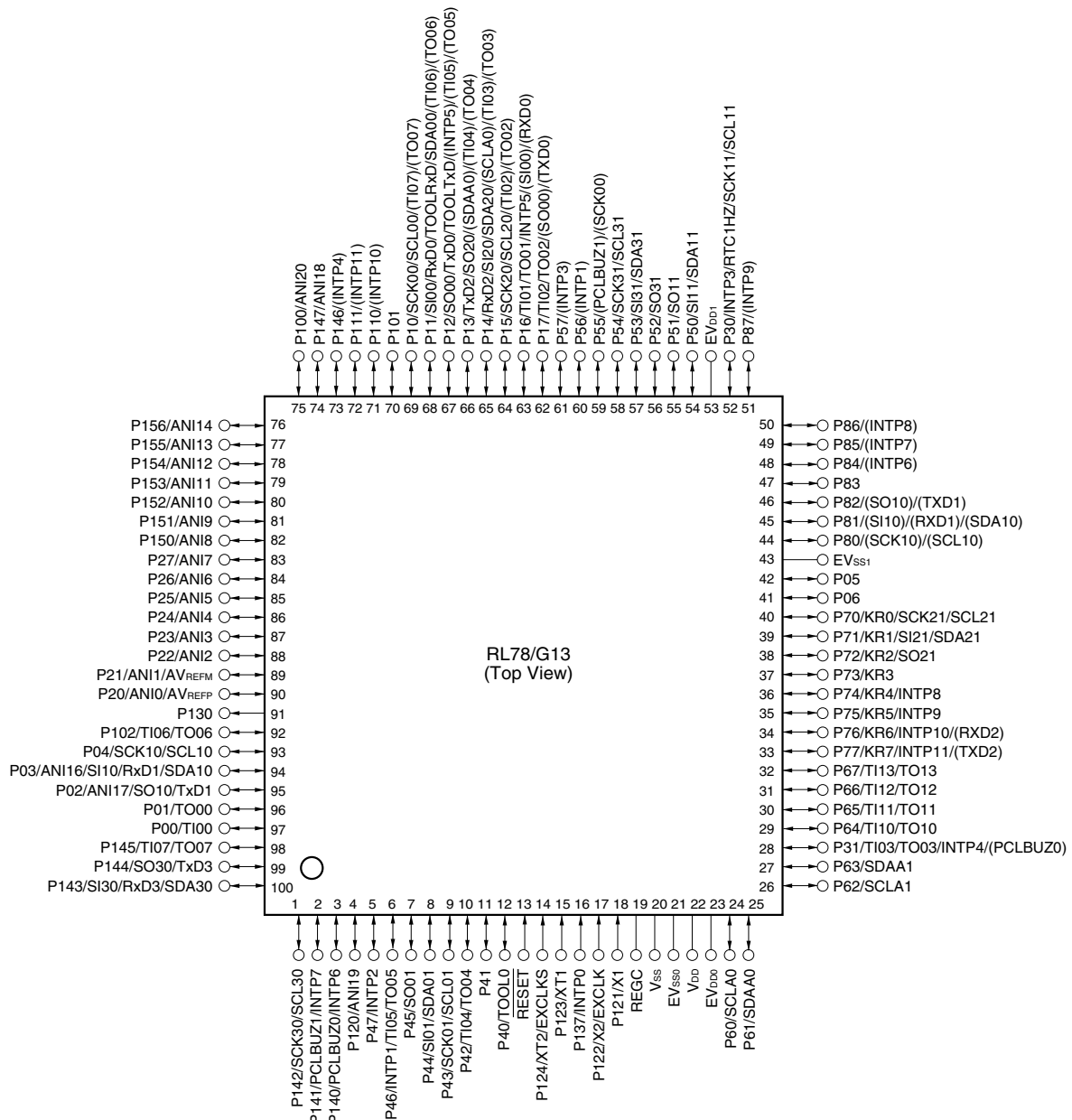
Cautions 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.

    2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

    3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

    2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

    3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.4 Pin Identification

ANI0 to ANI14, ANI16 to ANI26:	Analog input	$\overline{REGC}$: $\overline{RESET}$:	Regulator capacitance Reset
AV$_{REFM}$:	A/D converter reference potential ($-$ side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AV$_{REFP}$:	A/D converter reference potential (+ side) input	RxD0 to RxD3: SCK00, SCK01, SCK10,	Receive data
EV$_{DD0}$, EV$_{DD1}$:	Power supply for port	SCK11, SCK20, SCK21,	
EV$_{SS0}$, EV$_{SS1}$:	Ground for port	SCLA0, SCLA1:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20,SCL21, SCL30, SCL31:	Serial clock output
INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01,SDA10, SDA11,	
KR0 to KR7:	Key return	SDA20,SDA21, SDA30,	
P00 to P07:	Port 0	SDA31:	Serial data input/output
P10 to P17:	Port 1	SI00, SI01, SI10, SI11,	
P20 to P27:	Port 2	SI20, SI21, SI30, SI31:	Serial data input
P30 to P37:	Port 3	SO00, SO01, SO10,	
P40 to P47:	Port 4	SO11, SO20, SO21,	
P50 to P57:	Port 5	SO30, SO31:	Serial data output
P60 to P67:	Port 6	TI00 to TI07,	
P70 to P77:	Port 7	TI10 to TI17:	Timer input
P80 to P87:	Port 8	TO00 to TO07,	
P90 to P97:	Port 9	TO10 to TO17:	Timer output
P100 to P106:	Port 10	TOOL0:	Data input/output for tool
P110 to P117:	Port 11	TOOLRxD, TOOLTxD:	Data input/output for external device
P120 to P127:	Port 12	TxD0 to TxD3:	Transmit data
P130, P137:	Port 13	V$_{DD}$:	Power supply
P140 to P147:	Port 14	V$_{SS}$:	Ground
P150 to P156:	Port 15	X1, X2:	Crystal oscillator (main system clock)
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	XT1, XT2:	Crystal oscillator (subsystem clock)

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V$_{DD}$ < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f$_X$)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	f$_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ V$_{DD}$ < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ V$_{DD}$ < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I$_{OH1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			−10.0 [Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			−55.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			−10.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			−5.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			−2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			−80.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			−19.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			−10.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			−5.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			−135.0 [Note 4]	mA
	I$_{OH2}$	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV$_{DD0}$, EV$_{DD1}$, V$_{DD}$ pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OH}$ × 0.7)/(n × 0.01)

    <Example> Where n = 80% and I$_{OH}$ = −10.0 mA

        Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is −100 mA.

Caution **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

   2. When high-speed on-chip oscillator and subsystem clock are stopped.

   3. When high-speed system clock and subsystem clock are stopped.

   4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

   5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 32 MHz

   2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 16 MHz

   LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 8 MHz

   LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

   2. f$_{IH}$: High-speed on-chip oscillator clock frequency

   3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

   4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T$_A$ = –40 to +85°C, 2.7 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	62.5		250		500		ns
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	83.3		250		500		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		23		110		110		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		33		110		110		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	C = 20 pF Note 4			10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution   Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00))

3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with EV$_{DD0}$ $\geq$ V$_b$.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ EV$_{DD0}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)
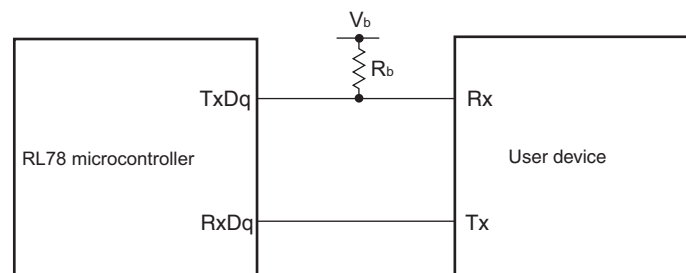
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	14/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	20/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	24 MHz < f$_{MCK}$	48/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD1}$	Operating mode	HS (high-speed main) mode Note 5	f$_{IH}$ = 32 MHz Note 3	Basic operation	V$_{DD}$ = 5.0 V		2.1		mA
						V$_{DD}$ = 3.0 V		2.1		mA
					Normal operation	V$_{DD}$ = 5.0 V		4.6	7.5	mA
						V$_{DD}$ = 3.0 V		4.6	7.5	mA
				f$_{IH}$ = 24 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		3.7	5.8	mA
						V$_{DD}$ = 3.0 V		3.7	5.8	mA
				f$_{IH}$ = 16 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		2.7	4.2	mA
						V$_{DD}$ = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode Note 5	f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = −40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +105°C	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.6 **Note 2**	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 **Note 4**	Mbps
			2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 **Note 6**	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV$_{DD0}$ < 4.0 V and 2.4 V ≤ V$_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution   Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)
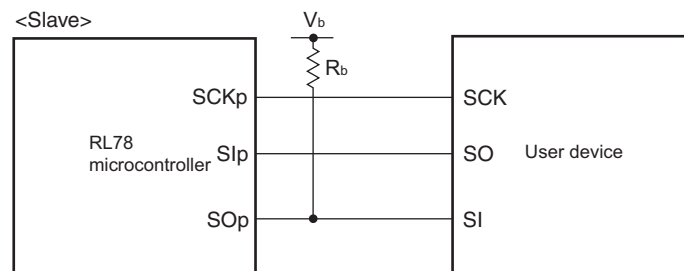
Remarks 1. R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02,

10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I^{2}C mode connection diagram (during communication at different potential)
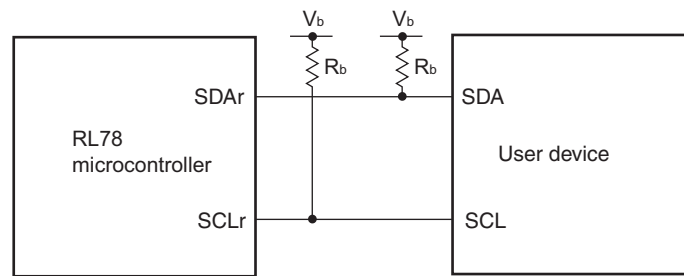
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
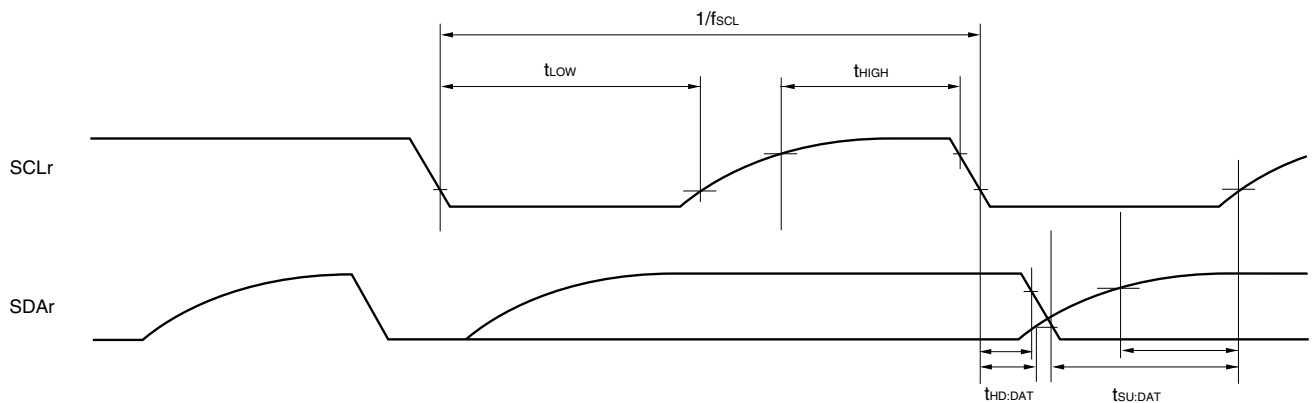
Caution   Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1. R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01, 02, 10, 12, 13)

3.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +105°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V_{LVD1}	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V_{LVD2}	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V_{LVD3}	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V_{LVD4}	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V_{LVD5}	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V_{LVD6}	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V_{LVD7}	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +105°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage			2.64	2.75	2.86	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		2.81	2.92	3.03	V
			Falling interrupt voltage		2.75	2.86	2.97	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.90	3.02	3.14	V
			Falling interrupt voltage		2.85	2.96	3.07	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.90	4.06	4.22	V
			Falling interrupt voltage		3.83	3.98	4.13	V

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms
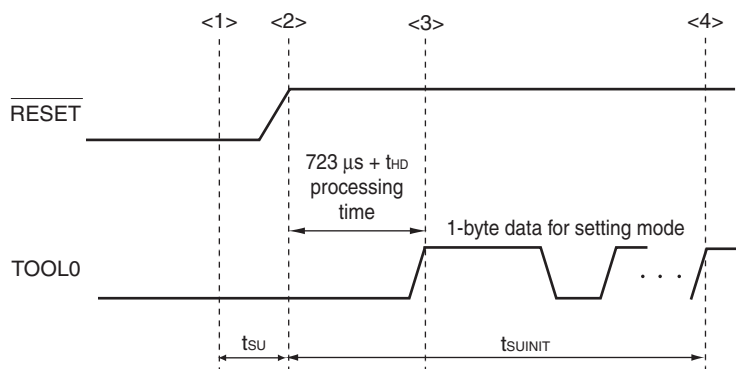
<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t$_{SU}$:   Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:   Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

		Description	
Rev.	**Date**	**Page**	**Summary**
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I^2C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I^2C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)
		109	Addition of (1) I^2C standard mode
		111	Addition of (2) I^2C fast mode
		112	Addition of (3) I^2C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)