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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100leafb-30

Table 1-1. List of Ordering Part Numbers

(4/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)	Mounted	A	R5F100FAAFP#V0, R5F100FCAFP#V0, R5F100FDAFP#V0, R5F100FEAFP#V0, R5F100FFAFP#V0, R5F100FGAFP#V0, R5F100FHAFP#V0, R5F100FJAFP#V0, R5F100FKAFP#V0, R5F100FLAFP#V0 R5F100FAAFP#X0, R5F100FCAFP#X0, R5F100FDAFP#X0, R5F100FEAFP#X0, R5F100FFAFP#X0, R5F100FGAFP#X0, R5F100FHAFP#X0, R5F100FJAFP#X0, R5F100FKAFP#X0, R5F100FLAFP#X0
			D	R5F100FADFP#V0, R5F100FCDFP#V0, R5F100FDDFP#V0, R5F100FEDFP#V0, R5F100FFDFP#V0, R5F100FGDFP#V0, R5F100FHDFP#V0, R5F100FJDFP#V0, R5F100FKDFP#V0, R5F100FLDFP#V0 R5F100FADFP#X0, R5F100FCDFP#X0, R5F100FDDFP#X0, R5F100FEDFP#X0, R5F100FFDFP#X0, R5F100FGDFP#X0, R5F100FHDFP#X0, R5F100FJDFP#X0, R5F100FKDFP#X0, R5F100FLDFP#X0
			G	R5F100FAGFP#V0, R5F100FCGFP#V0, R5F100FDGFP#V0, R5F100FEGFP#V0, R5F100FFGFP#V0, R5F100FGGFP#V0, R5F100FHGFP#V0, R5F100FJGFP#V0 R5F100FAGFP#X0, R5F100FCGFP#X0, R5F100FDGFP#X0, R5F100FEGFP#X0, R5F100FFGFP#X0, R5F100FGGFP#X0, R5F100FHGFP#X0, R5F100FJGFP#X0
		Not mounted	A	R5F101FAAFP#V0, R5F101FCAFP#V0, R5F101FDAFP#V0, R5F101FEAFP#V0, R5F101FFAFP#V0, R5F101FGAFP#V0, R5F101FHAFP#V0, R5F101FJAFP#V0, R5F101FKAFP#V0, R5F101FLAFP#V0 R5F101FAAFP#X0, R5F101FCAFP#X0, R5F101FDAFP#X0, R5F101FEAFP#X0, R5F101FFAFP#X0, R5F101FGAFP#X0, R5F101FHAFP#X0, R5F101FJAFP#X0, R5F101FKAFP#X0, R5F101FLAFP#X0
			D	R5F101FADFP#V0, R5F101FCDFP#V0, R5F101FDDFP#V0, R5F101FEDFP#V0, R5F101FFDFP#V0, R5F101FGDFP#V0, R5F101FHDFP#V0, R5F101FJDFP#V0, R5F101FKDFP#V0, R5F101FLDFP#V0 R5F101FADFP#X0, R5F101FCDFP#X0, R5F101FDDFP#X0, R5F101FEDFP#X0, R5F101FFDFP#X0, R5F101FGDFP#X0, R5F101FHDFP#X0, R5F101FJDFP#X0, R5F101FKDFP#X0, R5F101FLDFP#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(7/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A	R5F100JCAFA#V0, R5F100JDFA#V0, R5F100JEAF#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDFA#X0, R5F100JEAF#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKFA#X0, R5F100JLAFA#X0 D R5F100JCDA#V0, R5F100JDDA#V0, R5F100JEDA#V0, R5F100JFDA#V0, R5F100JGDA#V0, R5F100JHDA#V0, R5F100JJDA#V0, R5F100JKDA#V0, R5F100JLDA#V0 R5F100JCDA#X0, R5F100JDDA#X0, R5F100JEDA#X0, R5F100JFDA#X0, R5F100JGDA#X0, R5F100JHDA#X0, R5F100JJDA#X0, R5F100JKDA#X0, R5F100JLDA#X0 G R5F100JCGA#V0, R5F100JDGA#V0, R5F100JEGA#V0, R5F100JFGA#V0, R5F100JGGA#V0, R5F100JHGA#V0, R5F100JJGA#V0 R5F100JCGA#X0, R5F100JDGA#X0, R5F100JEGA#X0, R5F100JFGA#X0, R5F100JGGA#X0, R5F100JHGA#X0, R5F100JJGA#X0
		Not mounted	A	R5F101JCAFA#V0, R5F101JDFA#V0, R5F101JEAF#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDFA#X0, R5F101JEAF#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKFA#X0, R5F101JLAFA#X0 D R5F101JCDA#V0, R5F101JDDA#V0, R5F101JEDA#V0, R5F101JFDA#V0, R5F101JGDA#V0, R5F101JHDA#V0, R5F101JJDA#V0, R5F101JKDA#V0, R5F101JLDA#V0 R5F101JCDA#X0, R5F101JDDA#X0, R5F101JEDA#X0, R5F101JFDA#X0, R5F101JGDA#X0, R5F101JHDA#X0, R5F101JJDA#X0, R5F101JKDA#X0, R5F101JLDA#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

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Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	Mounted	A	R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0 R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0
			D	R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDDB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0 R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDDB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0
			G	R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0 R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0
				R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0, R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Not mounted	A	R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0 R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0
			D	R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDDB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0 R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDDB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Mounted	A	R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0
			G	R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGBG#U0, R5F100LGGBG#U0, R5F100LHGBG#U0, R5F100LJGBG#U0 R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGBG#W0, R5F100LGGBG#W0, R5F100LHGBG#W0, R5F100LJGBG#W0
	64-pin plastic VFPGA (4 × 4 mm, 0.4 mm pitch)	Not mounted	A	R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0 R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0

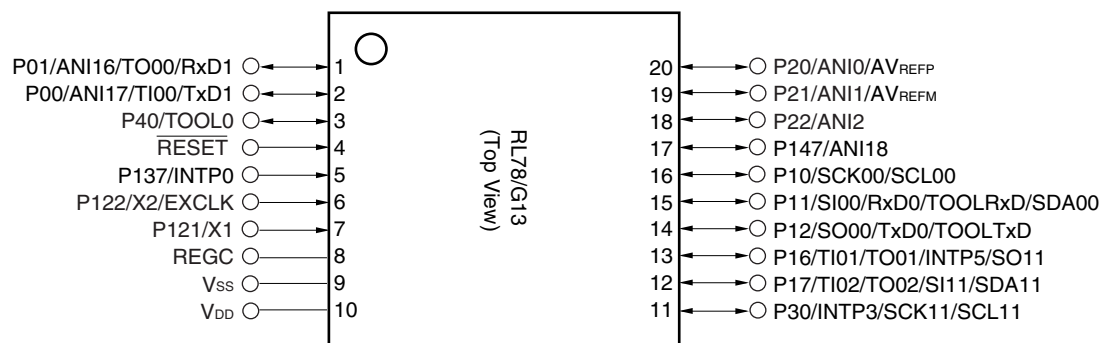
Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

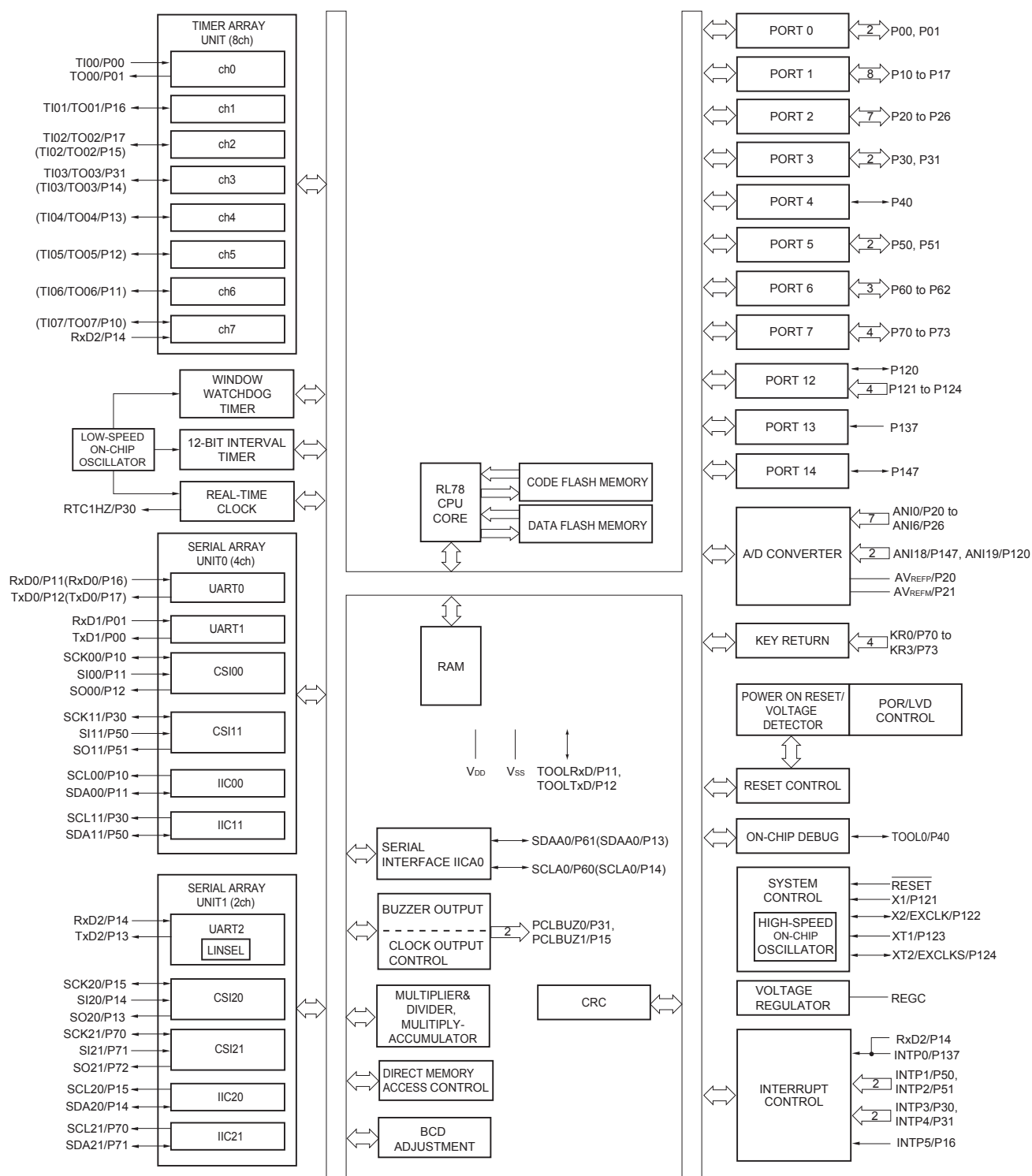
- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

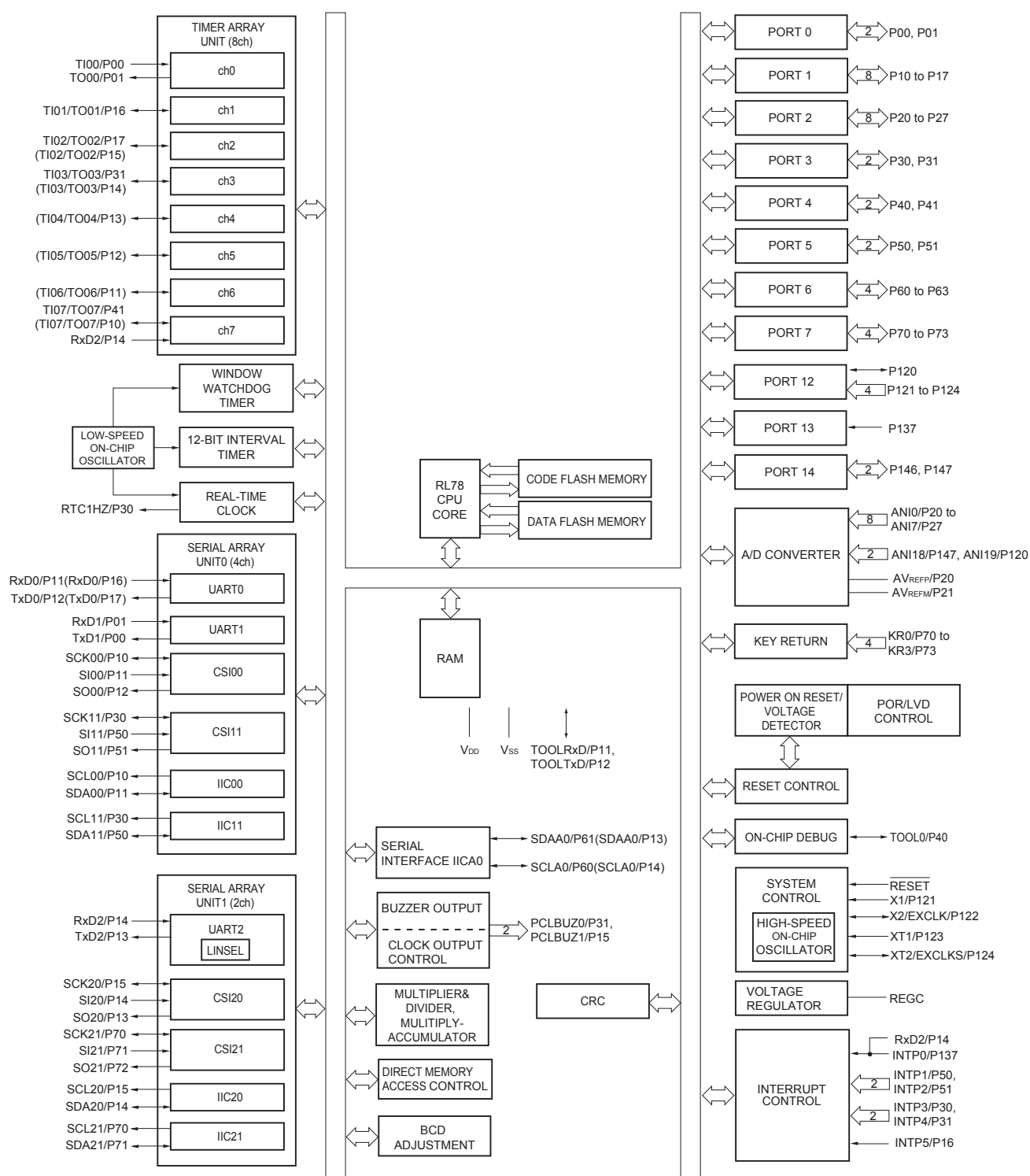
Remark For pin identification, see 1.4 Pin Identification.

1.5.7 40-pin products



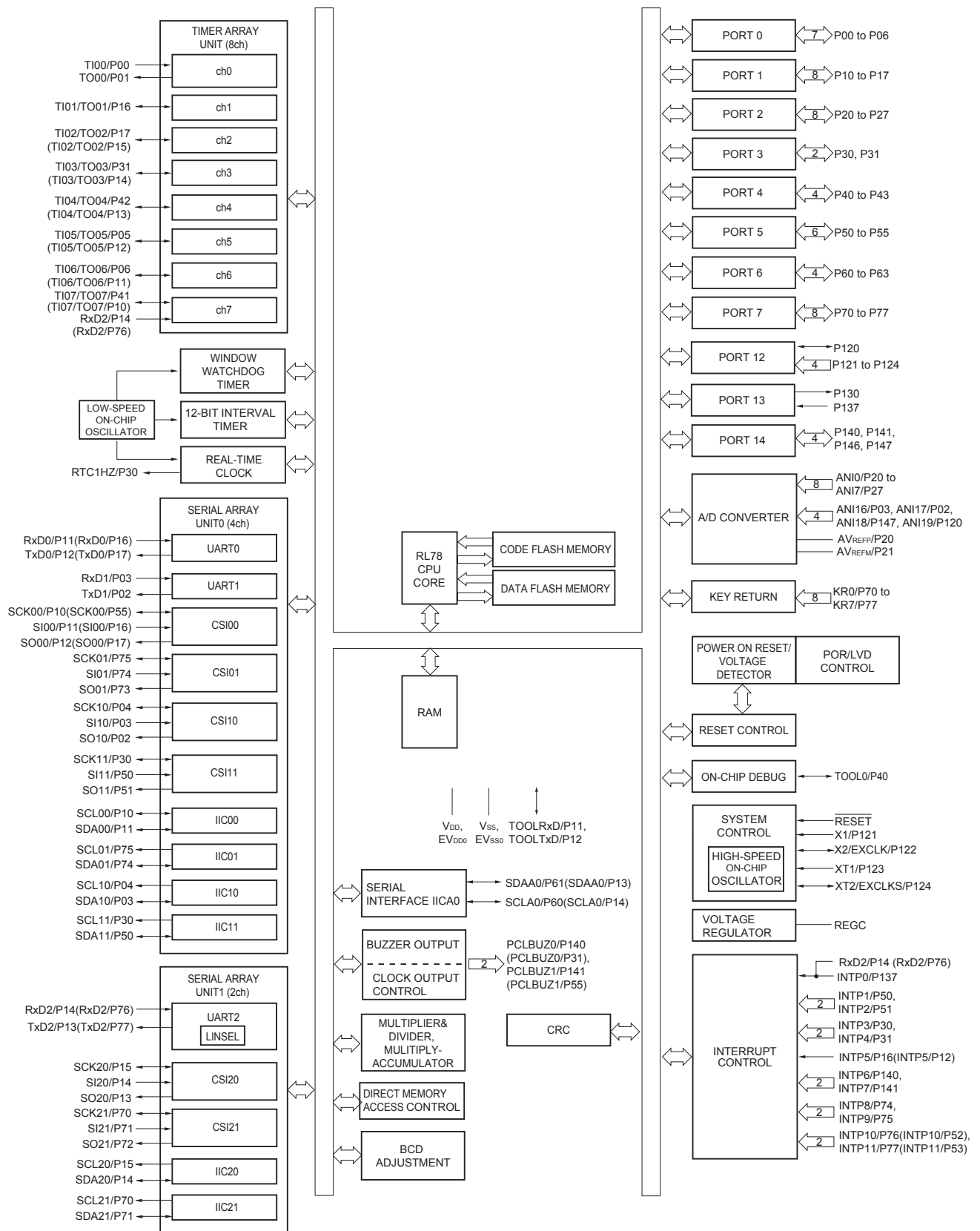
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.8 44-pin products



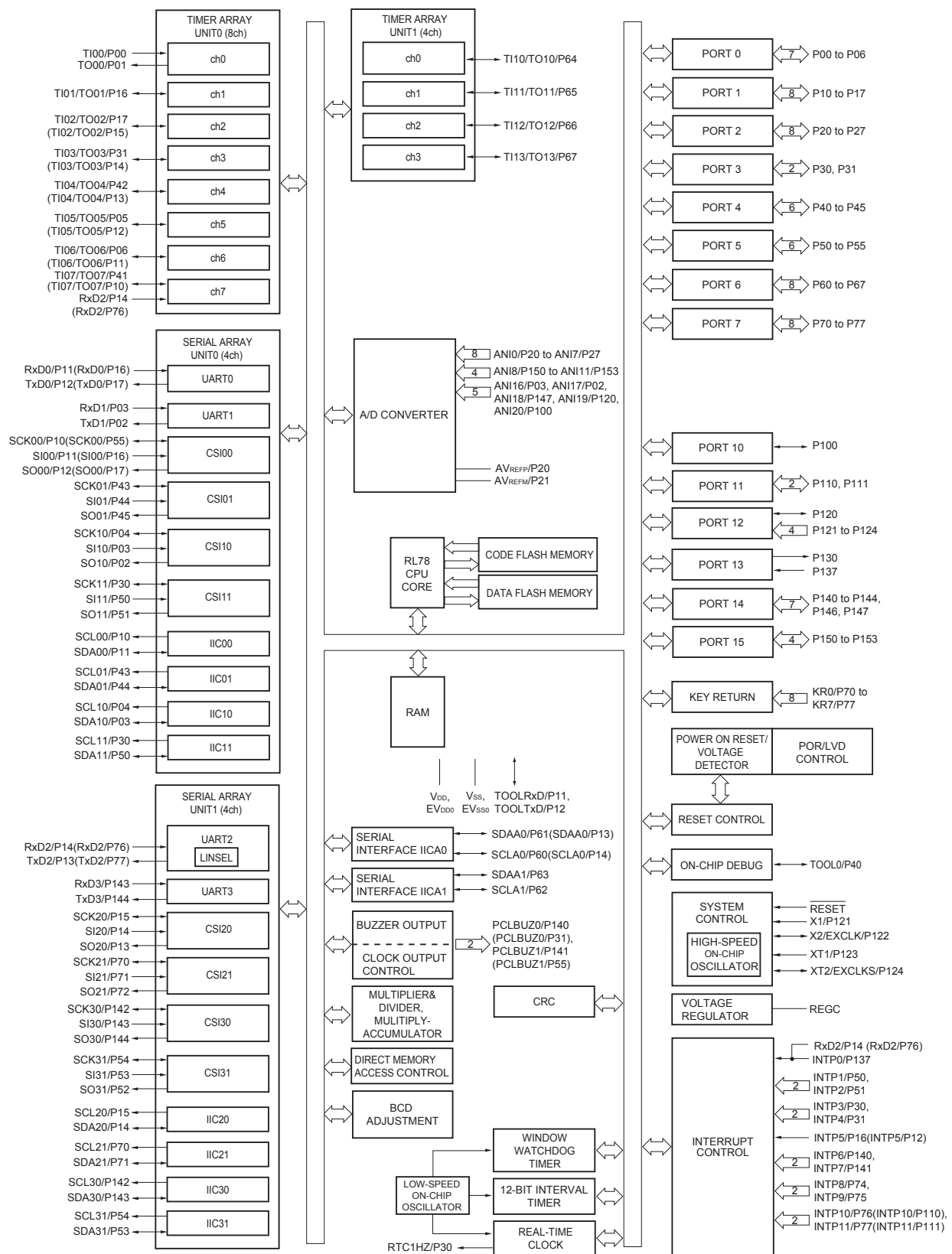
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.11 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.12 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output	—		1		1		2		2		2	
	• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)											
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface	[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I ² C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I ² C bus	—	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller	2 channels											
Vectored interrupt sources	Internal	23	24		24		27		27		27	
	External	3	5		5		6		6		6	
Key interrupt	—											
Reset	• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit	• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector	• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function	Provided											
Power supply voltage	V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)											
Operating ambient temperature	T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)											

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to }16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to }8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to }4\text{ MHz}$

- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

- Remarks 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(2/3)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSH1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		ns

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$
R5F100xxGxx

- Cautions 1.** The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
- 2.** With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
- 3.** The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.
- 4.** Please contact Renesas Electronics sales office for derating of operation under $T_A = +85^\circ\text{C}$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$)**.

There are following differences between the products "G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)" and the products "A: Consumer applications, and D: Industrial applications".

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C $1.6\text{ V} \leq V_{\text{DD}} < 1.8\text{ V}$ $\pm 5.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\% @ T_A = -40$ to -20°C	$2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 2.0\% @ T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to -20°C
Serial array unit	UART CSI: $f_{\text{CLK}}/2$ (supporting 16 Mbps), $f_{\text{CLK}}/4$ Simplified I ² C communication	UART CSI: $f_{\text{CLK}}/4$ Simplified I ² C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(Remark is listed on the next page.)

3.3.2 Supply current characteristics

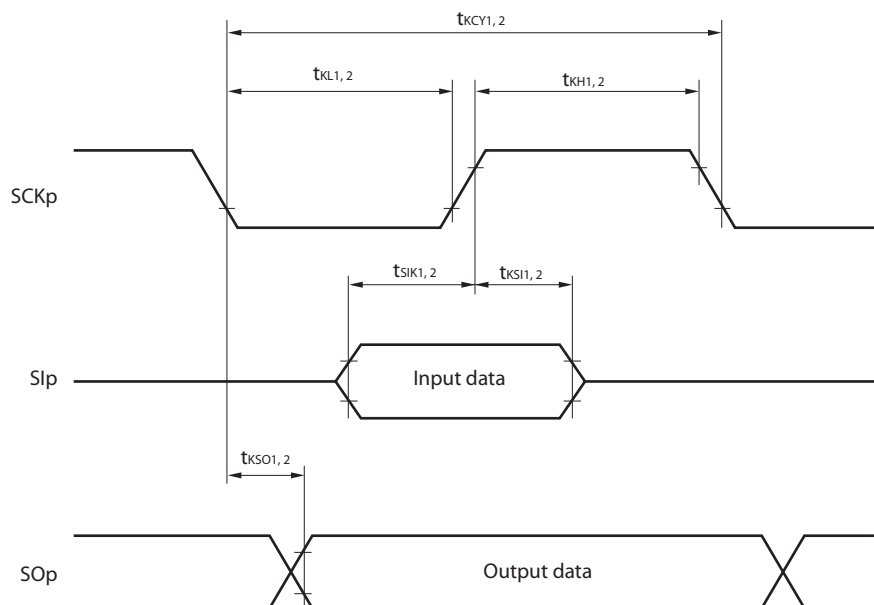
(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = 0\text{ V}$) (1/2)

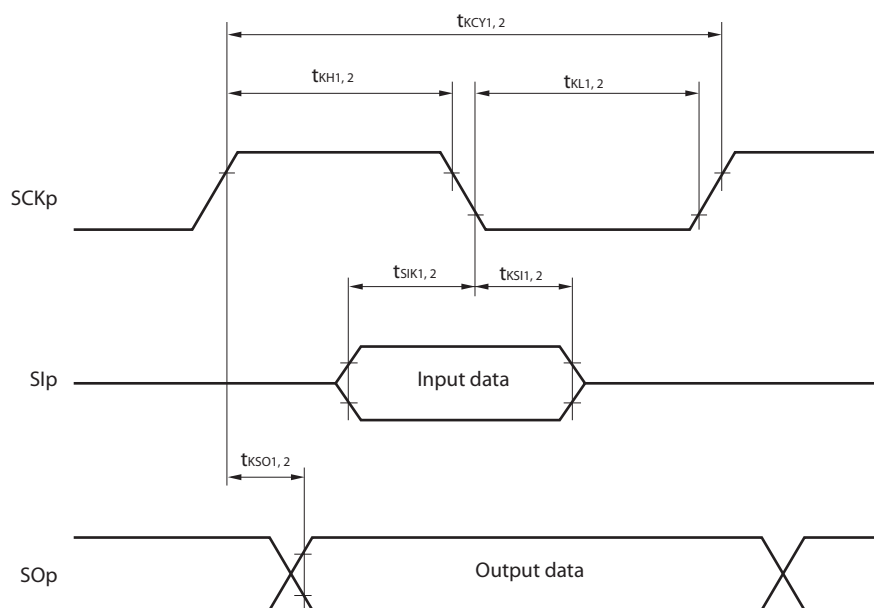
Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		2.1		mA
						$V_{DD} = 3.0\text{ V}$		2.1		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		4.6	7.5	mA
						$V_{DD} = 3.0\text{ V}$		4.6	7.5	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		3.7	5.8	mA
						$V_{DD} = 3.0\text{ V}$		3.7	5.8	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	4.2	mA
						$V_{DD} = 3.0\text{ V}$		2.7	4.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock operation		$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(Notes and Remarks are listed on the next page.)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(4) During communication at same potential (simplified I²C mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		400 ^{Note1}	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$		100 ^{Note1}	
Hold time when SCLr = "L"	t_{LOW}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		
Hold time when SCLr = "H"	t_{HIGH}	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	4600		
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ ^{Note2}		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ ^{Note2}		
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 3\text{ k}\Omega$	0	1420	

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1,2,3	C _{enwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	1,000			Times
Number of data flash rewrites Notes 1,2,3		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ Note 4	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ Note 4	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

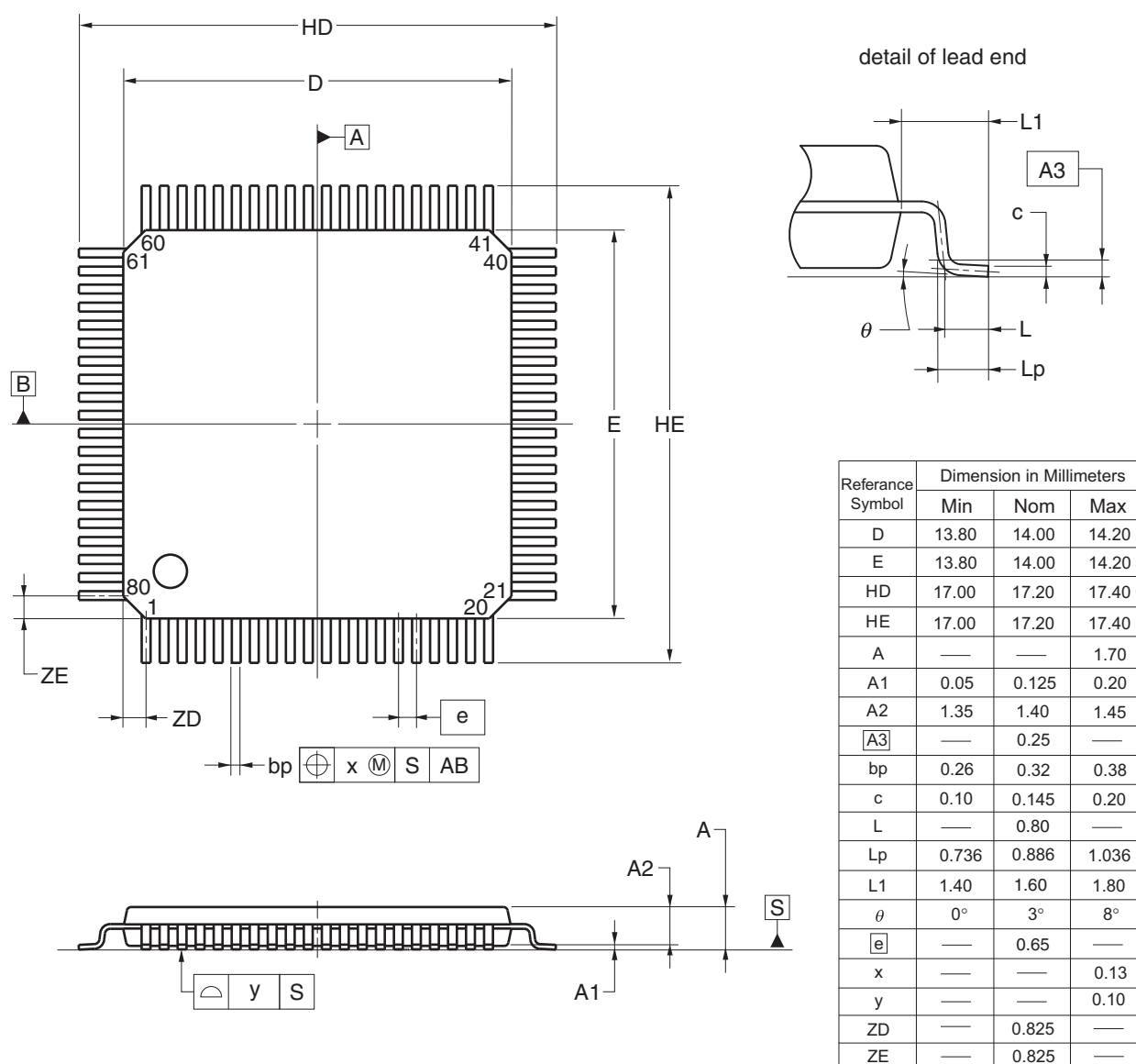
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.12 80-pin Products

R5F100MFAFA, R5F100MGFAFA, R5F100MHAFA, R5F100MJFAFA, R5F100MKAFA, R5F100MLAFA
 R5F101MFAFA, R5F101MGFAFA, R5F101MHAFA, R5F101MJFAFA, R5F101MKAFA, R5F101MLAFA
 R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
 R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA
 R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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Revision History	RL78/G13 Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 29, 2012	-	First Edition issued
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.
		59, 63, 67	Descriptions of Note 8 in a table corrected.
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.
3.00	Aug 02, 2013	1	Modification of 1.1 Features
		3	Modification of 1.2 List of Part Numbers
		4 to 15	Modification of Table 1-1. List of Ordering Part Numbers, note, and caution
		16 to 32	Modification of package type in 1.3.1 to 1.3.14
		33	Modification of description in 1.4 Pin Identification
		48, 50, 52	Modification of caution, table, and note in 1.6 Outline of Functions
		55	Modification of description in table of Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$)
		57	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics
		57	Modification of table in 2.2.2 On-chip oscillator characteristics
		58	Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics
		59	Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics
		63	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		64	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		65	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		66	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
		68	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		70	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products
		72	Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		74	Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products
		75	Modification of (4) Peripheral Functions (Common to all products)
		77	Modification of table in 2.4 AC Characteristics
		78, 79	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		80	Modification of figures of AC Timing Test Points and External System Clock Timing