



Welcome to [E-XFL.COM](#)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

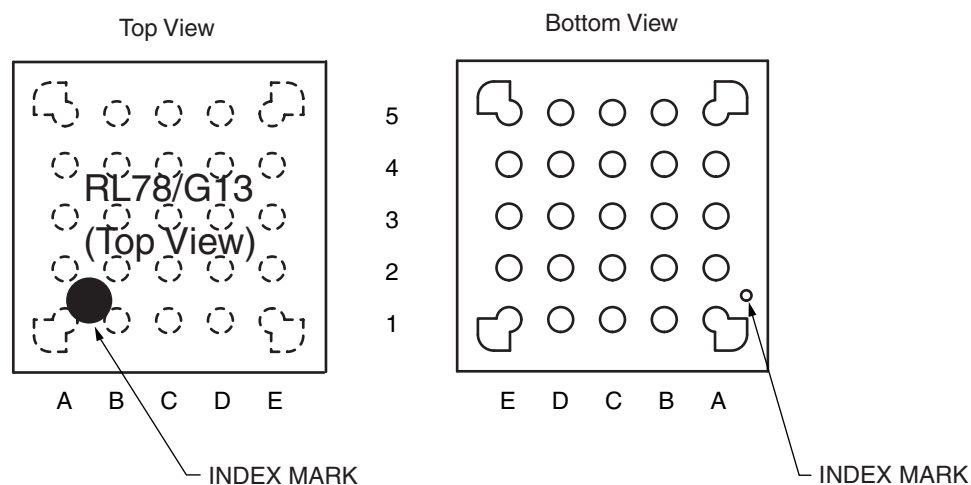
#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lfdfb-30">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lfdfb-30</a>

## 1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

&lt;R&gt;



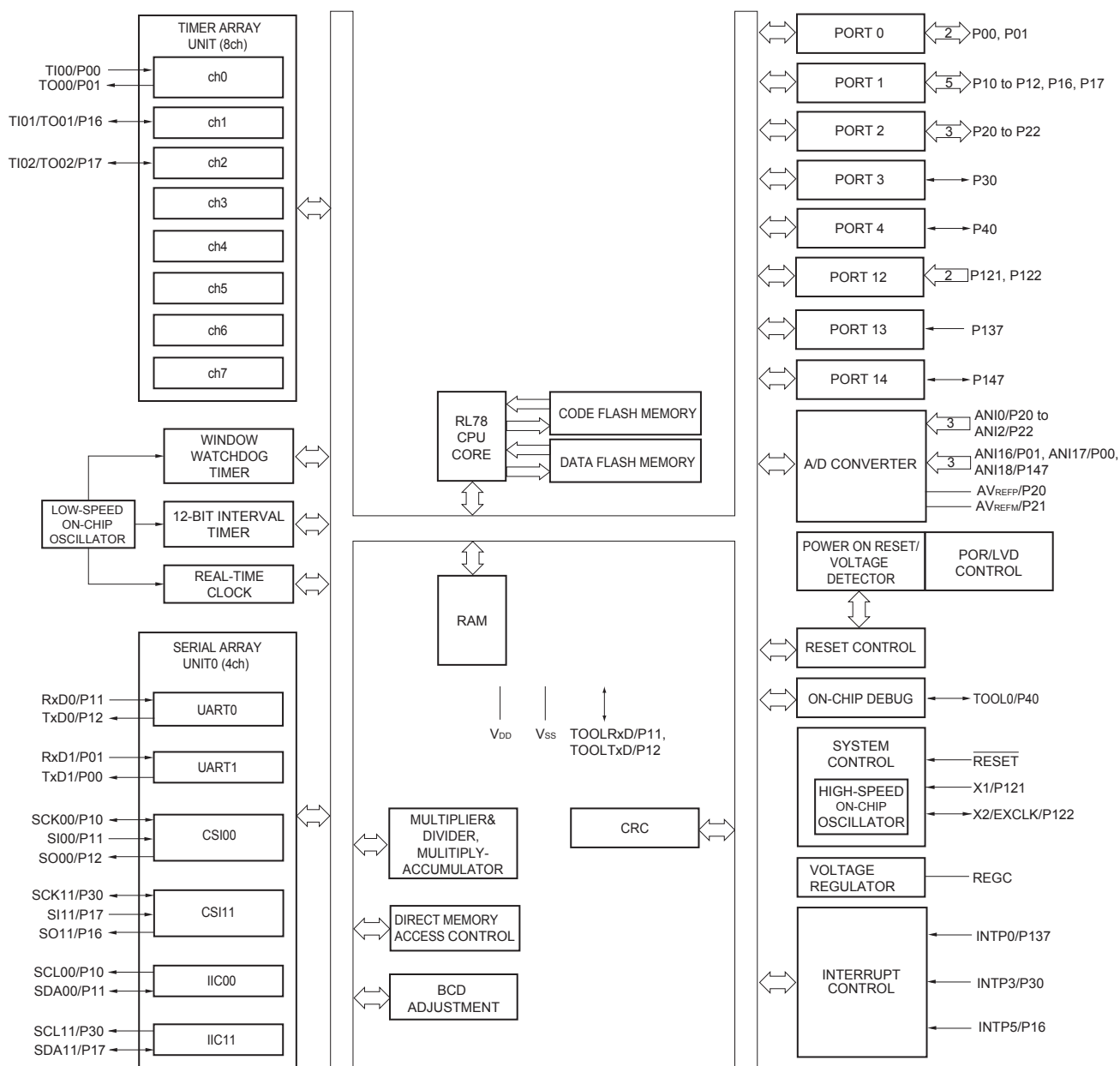
	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AV <sub>REFM</sub>	P10/SCK00/ SCL00	4
3	P121/X1	V <sub>DD</sub>	P20/ANI0/ AV <sub>REFP</sub>	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V <sub>SS</sub>	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

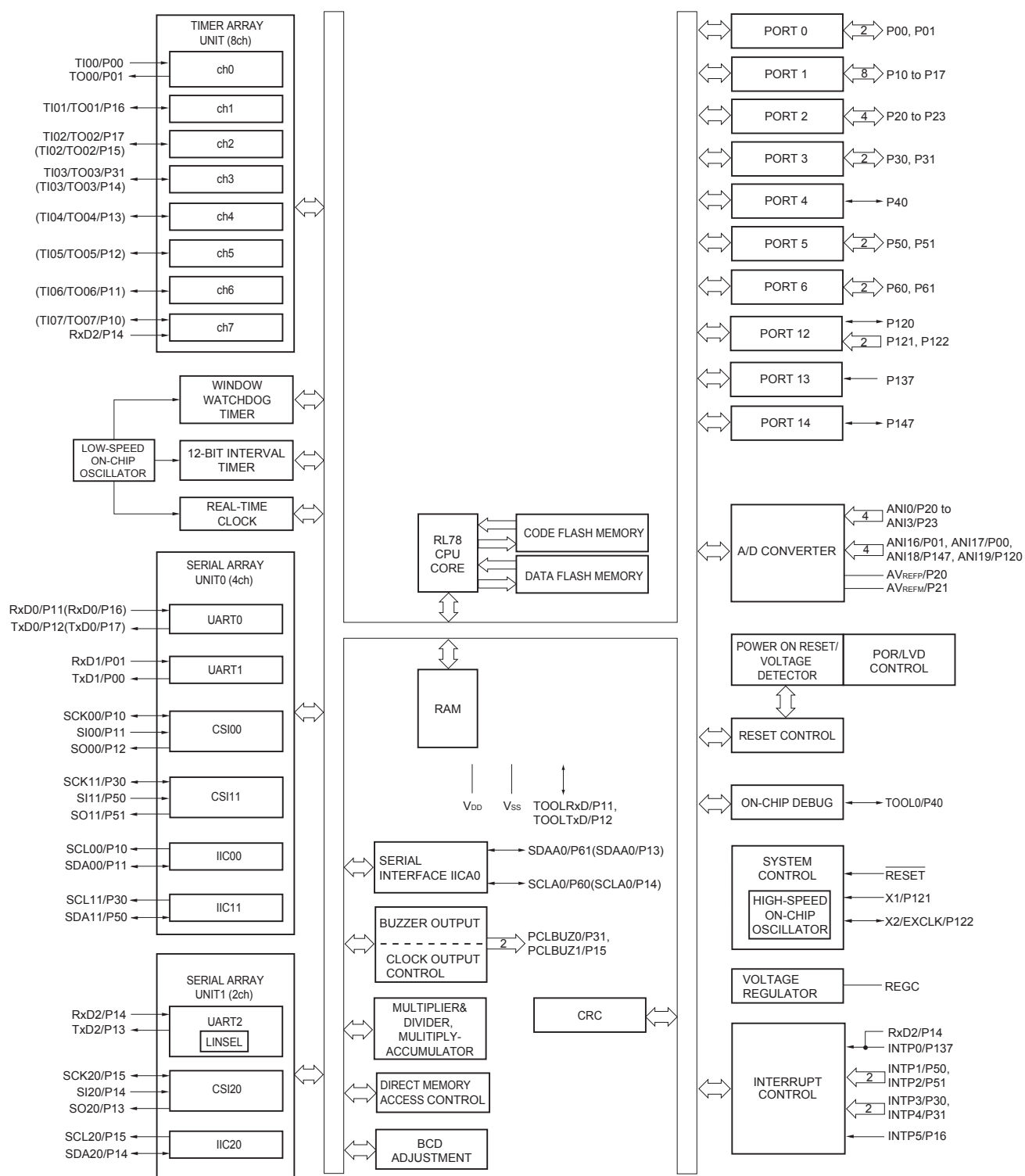
**Remark** For pin identification, see 1.4 Pin Identification.

## 1.5 Block Diagram

### 1.5.1 20-pin products

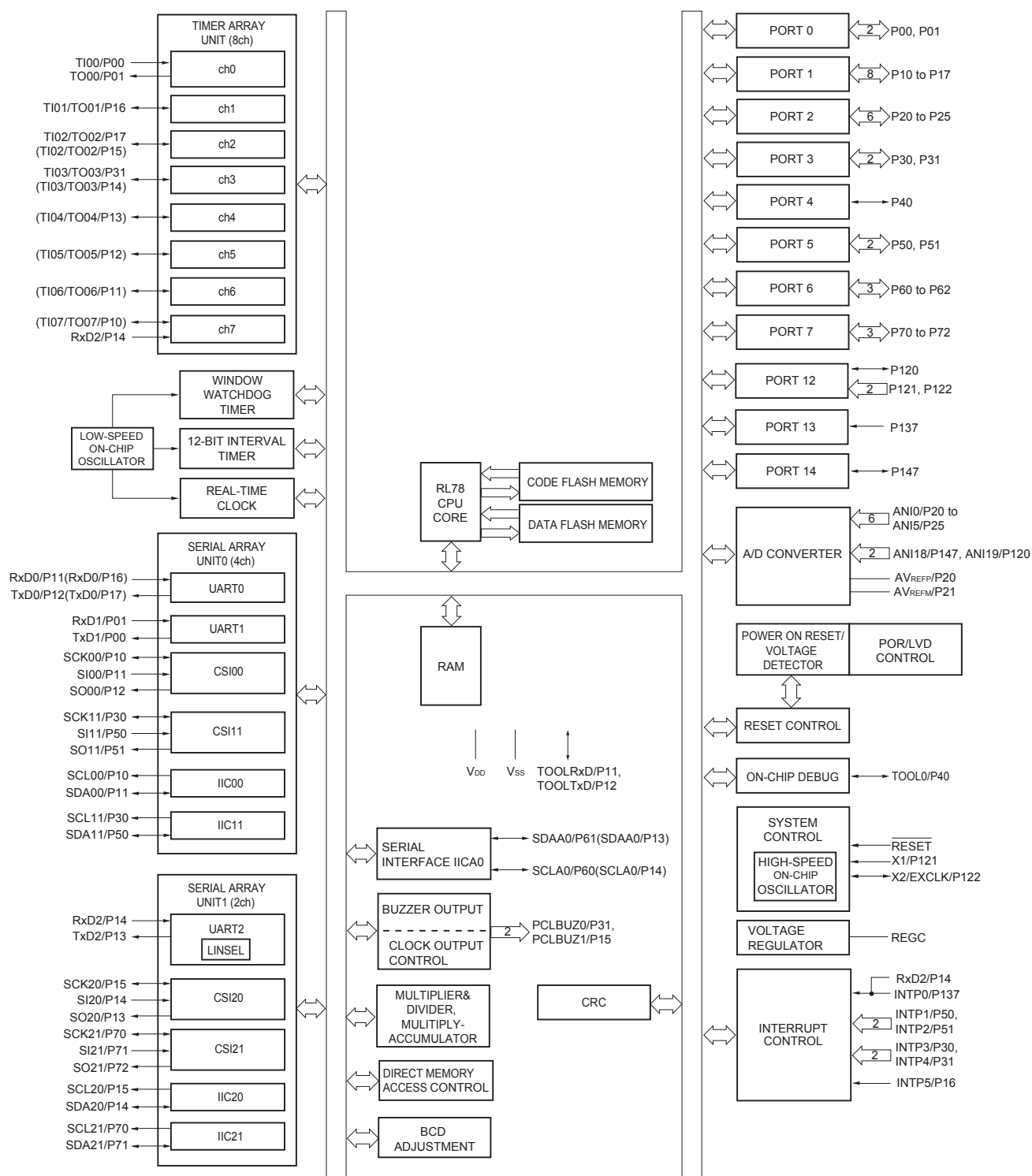


## 1.5.4 30-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.6 36-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <sup>Note 1</sup>	$\text{I}_{\text{DD1}}$	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 32\text{ MHz}$ <sup>Note 3</sup>	Basic operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		2.6	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		2.6	mA
					Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		6.1	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		6.1	mA
				$f_{\text{IH}} = 24\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		4.8	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		4.8	mA
				$f_{\text{IH}} = 16\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		3.5	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		3.5	mA
			LS (low-speed main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 8\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		1.5	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$		1.5	mA
			LV (low-voltage main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 4\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$		1.5	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$		1.5	mA
			HS (high-speed main) mode <sup>Note 5</sup>	$f_{\text{MX}} = 20\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		3.9	mA
						Resonator connection		4.1	mA
				$f_{\text{MX}} = 20\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		3.9	mA
						Resonator connection		4.1	mA
				$f_{\text{MX}} = 10\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		2.5	mA
						Resonator connection		2.5	mA
				$f_{\text{MX}} = 10\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		2.5	mA
						Resonator connection		2.5	mA
			LS (low-speed main) mode <sup>Note 5</sup>	$f_{\text{MX}} = 8\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		1.4	mA
						Resonator connection		1.4	mA
				$f_{\text{MX}} = 8\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 2.0\text{ V}$	Normal operation	Square wave input		1.4	mA
						Resonator connection		1.4	mA
			Subsystem clock operation	$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		5.4	$\mu\text{A}$
						Resonator connection		5.5	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		5.5	$\mu\text{A}$
						Resonator connection		5.6	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		5.6	$\mu\text{A}$
						Resonator connection		5.7	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.9	$\mu\text{A}$
						Resonator connection		6.0	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		6.6	$\mu\text{A}$
						Resonator connection		6.7	$\mu\text{A}$

(Notes and Remarks are listed on the next page.)

## (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.4 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 38		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
		1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		—		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t <sub>SIK1</sub>	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t <sub>KSI1</sub>	1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t <sub>KSO1</sub>	1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			25		25		25	ns
		1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			—		25		25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

3. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> < 4.0 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.
6. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

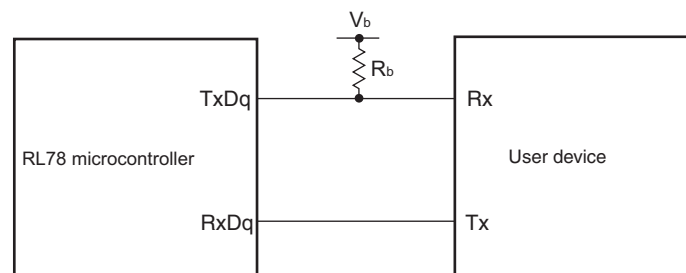
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the Rx<sub>Dq</sub> pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the Tx<sub>Dq</sub> pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)





**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	t <sub>KCY2</sub> /2 - 12		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	t <sub>KCY2</sub> /2 - 18		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 3</sup>	t <sub>SIK2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
Slp hold time (from SCKp↑) <sup>Note 4</sup>	t <sub>KS12</sub>		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		ns
Delay time from SCKp↓ to SOp output <sup>Note 5</sup>	t <sub>KSO2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ		2/f <sub>MCK</sub> + 120		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ		2/f <sub>MCK</sub> + 214		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns

**Notes** 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

&lt;R&gt;

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
  2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (4/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	$\text{V}_{\text{OH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	$\text{V}_{\text{OH2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	$\text{V}_{\text{OL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	$\text{V}_{\text{OL2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	$\text{V}_{\text{OL3}}$	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	250		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	500		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2 – 24		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2 – 36		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	t <sub>KCY1</sub> /2 – 76		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	66		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	66		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	113		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI1</sub>		38		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO1</sub>	C = 30 pF <sup>Note 4</sup>		50	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	$f_{SCL}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		400 <sup>Note1</sup>	kHz
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$		100 <sup>Note1</sup>	
Hold time when SCLr = "L"	$t_{LOW}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		
Hold time when SCLr = "H"	$t_{HIGH}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		
Data setup time (reception)	$t_{SU:DAT}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{MCK} + 220$ <sup>Note2</sup>		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	$1/f_{MCK} + 580$ <sup>Note2</sup>		
Data hold time (transmission)	$t_{HD:DAT}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	0	1420	

**Notes** 1. The value must also be equal to or less than  $f_{MCK}/4$ .2. Set the  $f_{MCK}$  value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

## (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V})$ 

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Reception	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$		$f_{MCK}/12$ <sup>Note 1</sup>	bps
			Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$		2.6	Mbps
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$		$f_{MCK}/12$ <sup>Note 1</sup>	bps
			Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$		2.6	Mbps
			$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$		$f_{MCK}/12$ <sup>Notes 1,2</sup>	bps
			Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$ , $f_{MCK} = f_{CLK}$		2.6	Mbps

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

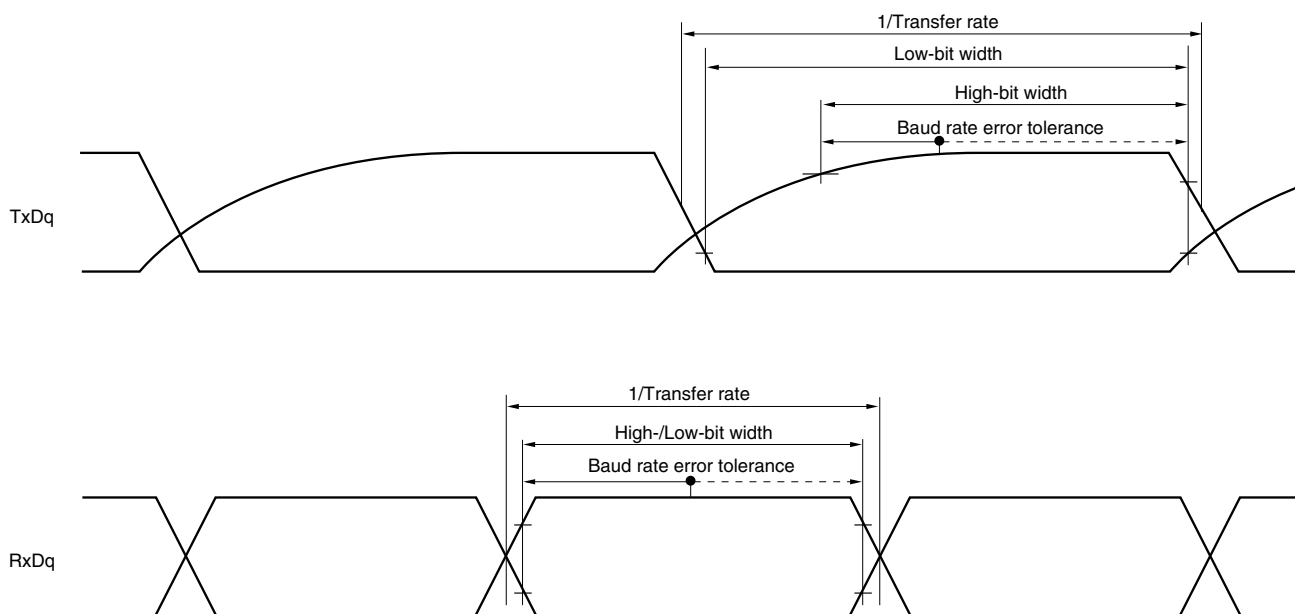
- 2.** The following conditions are required for low voltage interface when  $EV_{DD0} < V_{DD}$ .  
 $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$  : MAX. 1.3 Mbps

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

**Remarks 1.**  $V_b[V]$ : Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.**  $f_{MCK}$ : Serial array unit operation clock frequency

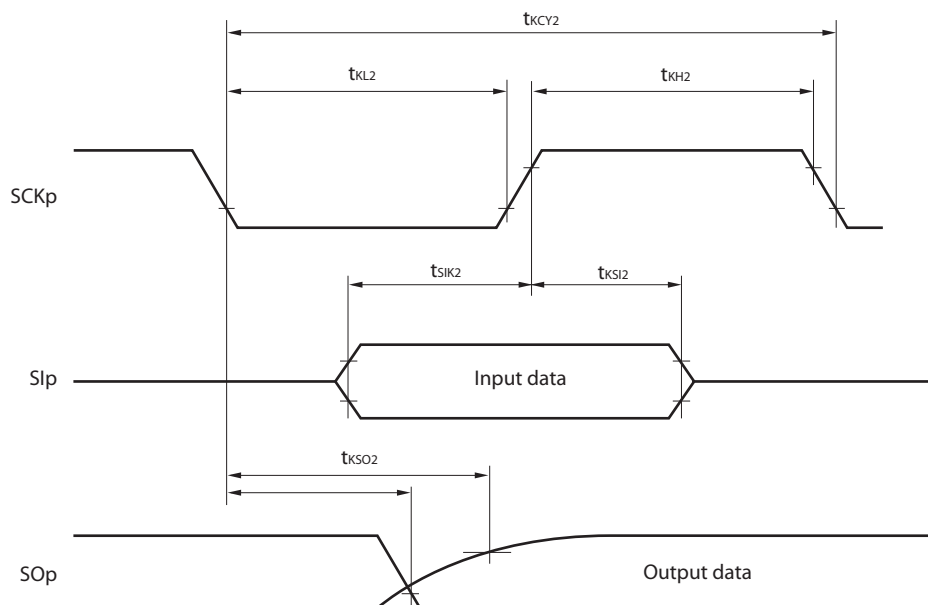
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

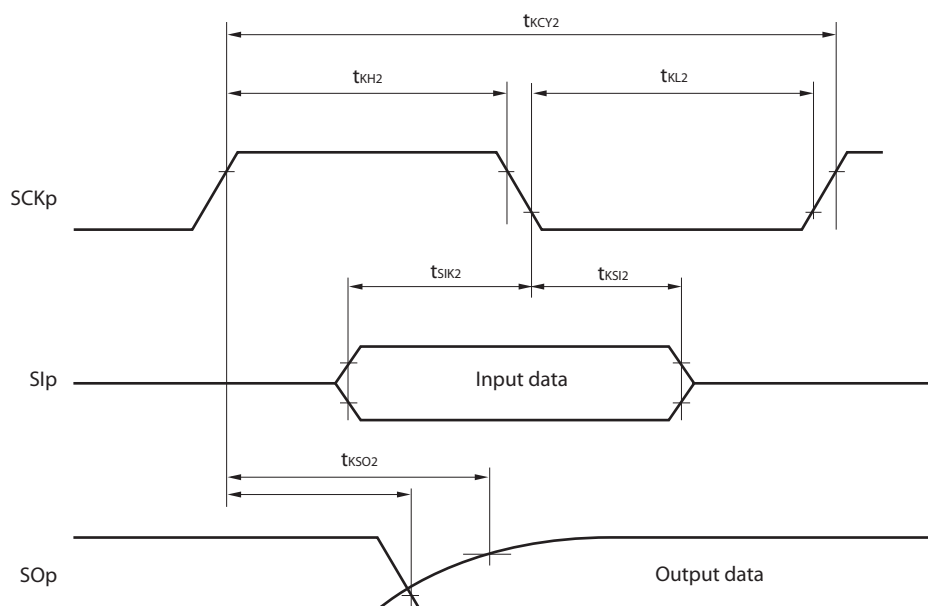
**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.



(3) When reference voltage (+) =  $V_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) =  $V_{SS}$  (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

( $T_A = -40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $V_{DD}$ , Reference voltage (–) =  $V_{SS}$ )

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	$\pm 7.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	E <sub>FS</sub>	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 0.60$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 4.0$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			$\pm 2.0$	LSB
Analog input voltage	$V_{AIN}$	ANI0 to ANI14		0		$V_{DD}$	V
		ANI16 to ANI26		0		$EV_{DD0}$	V
		Internal reference voltage output ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{BGR}$ <sup>Note 3</sup>			V
		Temperature sensor output voltage ( $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , HS (high-speed main) mode)		$V_{TMPS25}$ <sup>Note 3</sup>			V

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

## 3.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V <sub>LVD0</sub>	Power supply rise time	3.90	4.06	4.22	V
			Power supply fall time	3.83	3.98	4.13	V
		V <sub>LVD1</sub>	Power supply rise time	3.60	3.75	3.90	V
			Power supply fall time	3.53	3.67	3.81	V
		V <sub>LVD2</sub>	Power supply rise time	3.01	3.13	3.25	V
			Power supply fall time	2.94	3.06	3.18	V
		V <sub>LVD3</sub>	Power supply rise time	2.90	3.02	3.14	V
			Power supply fall time	2.85	2.96	3.07	V
		V <sub>LVD4</sub>	Power supply rise time	2.81	2.92	3.03	V
			Power supply fall time	2.75	2.86	2.97	V
		V <sub>LVD5</sub>	Power supply rise time	2.70	2.81	2.92	V
			Power supply fall time	2.64	2.75	2.86	V
		V <sub>LVD6</sub>	Power supply rise time	2.61	2.71	2.81	V
			Power supply fall time	2.55	2.65	2.75	V
		V <sub>LVD7</sub>	Power supply rise time	2.51	2.61	2.71	V
			Power supply fall time	2.45	2.55	2.65	V
Minimum pulse width		t <sub>LW</sub>		300			μs
Detection delay time						300	μs

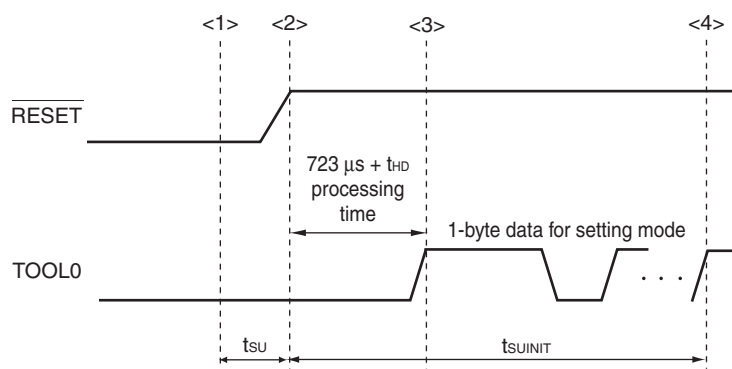
**LVD Detection Voltage of Interrupt & Reset Mode****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{PDR} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V <sub>LVDD0</sub>	V <sub>POC2</sub> , V <sub>POC1</sub> , V <sub>POC0</sub> = 0, 1, 1, falling reset voltage		2.64	2.75	2.86	V
	V <sub>LVDD1</sub>	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	V <sub>LVDD2</sub>	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	V <sub>LVDD3</sub>	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

## 3.10 Timing of Entry to Flash Memory Programming Modes

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	$t_{\text{SUNIT}}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	$t_{\text{SU}}$	POR and LVD reset must be released before the external reset is released.	10			$\mu\text{s}$
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	$t_{\text{HD}}$	POR and LVD reset must be released before the external reset is released.	1			ms



&lt;1&gt; The low level is input to the TOOL0 pin.

&lt;2&gt; The external reset is released (POR and LVD reset must be released before the external reset is released.).

&lt;3&gt; The TOOL0 pin is set to the high level.

&lt;4&gt; Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark**  $t_{\text{SUNIT}}$ : Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

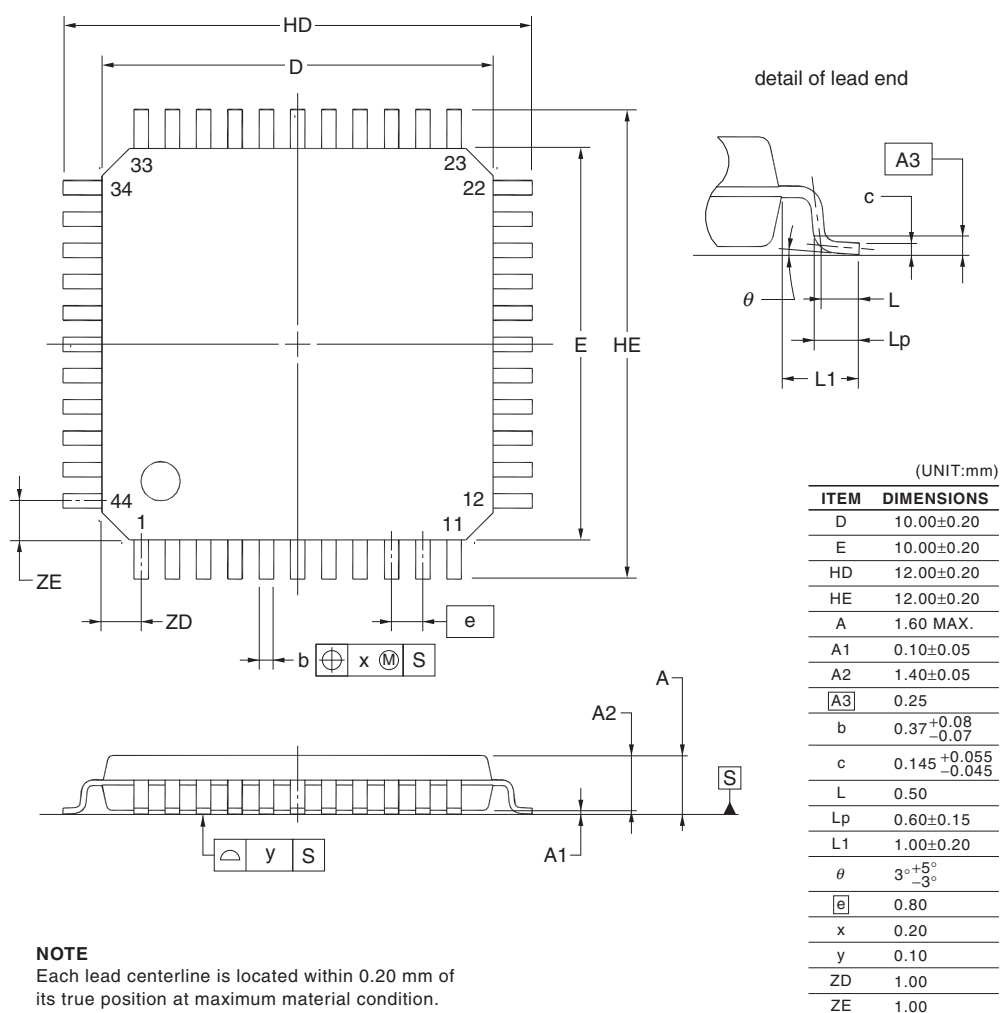
$t_{\text{SU}}$ : Time to release the external reset after the TOOL0 pin is set to the low level

$t_{\text{HD}}$ : Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

## 4.8 44-pin Products

R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP,  
 R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP  
 R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP,  
 R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP  
 R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP,  
 R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP  
 R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP,  
 R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP  
 R5F100FAGFP, R5F100FCGFP, R5F100FDGFP, R5F100FEGFP, R5F100FFGFP, R5F100FGGFP,  
 R5F100FHGFP, R5F100FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			<del>ACK</del> corrected to ACK
			<del>ACK</del> corrected to ACK

All trademarks and registered trademarks are the property of their respective owners.

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.