## Details

| | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 48 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 12K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 12x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lgafa-v0 |

## 1.2  List of Part Numbers

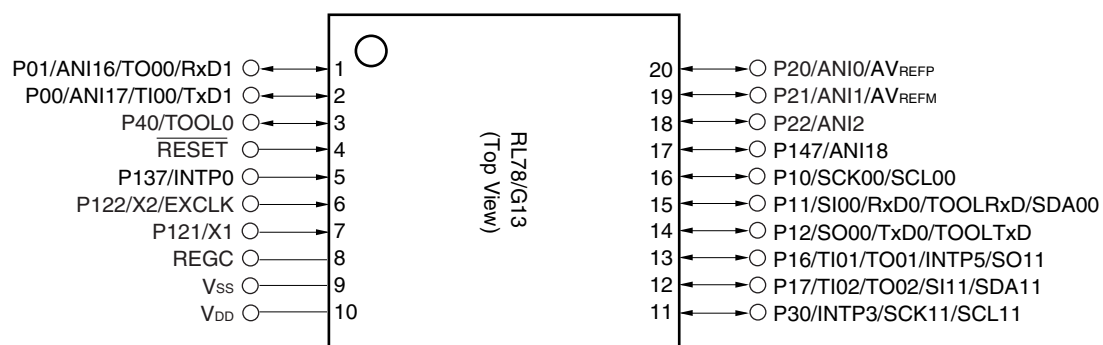**Figure 1-1.  Part Number, Memory Size, and Package of RL78/G13**

Part No.　R 5 F 1 0 0 L E A x x x F B #V0

Packaging specification
  #U0 : Tray (HWQFN,VFBGA,WFLGA)
  #V0 : Tray (LFQFP,LQFP,LSSOP)
  #W0 : Embossed Tape (HWQFN,VFBGA,WFLGA)
  #X0 : Embossed Tape (LFQFP, LQFP, LSSOP)

Package type:
  SP: LSSOP, 0.65 mm pitch
  FP : LFQFP, 0.80 mm pitch
  FA : LFQFP, 0.65 mm pitch
  FB : LFQFP, 0.50 mm pitch
  NA : HWQFN, 0.50 mm pitch
  LA : WFLGA, 0.50 mm pitch [Note 1]
  BG : VFBGA, 0.40 mm pitch [Note 1]

ROM number (Omitted with blank products)

Fields of application:
  A : Consumer applications, operating ambient temperature : -40˚C to +85˚C
  D : Industrial applications, operating ambient temperature : -40˚C to +85˚C
  G : Industrial applications, operating ambient temperature : -40˚C to +105˚C

ROM capacity:
  A :　 16 KB
  C :　 32 KB
  D :　 48 KB
  E :　 64 KB
  F :　 96 KB
  G : 128 KB
  H : 192 KB
  J : 256 KB
  K : 384 KB [Note 2]
  L : 512 KB [Note 2]

Pin count:
  6 :　20-pin
  7 :　24-pin
  8 :　25-pin [Note 1]
  A :　30-pin
  B :　32-pin
  C :　36-pin [Note 1]
  E :　40-pin
  F :　44-pin
  G :　48-pin
  J :　52-pin
  L :　64-pin
  M :　80-pin
  P :　100-pin
  S : 128-pin [Note 2]

RL78/G13 group
  100 : Data flash is provided
  101 : Data flash is not provided [Note 2]

Memory type:
  F : Flash memory

Renesas MCU

Renesas semiconductor product

**Notes**　**1.**　Products only for "A: Consumer applications (T$_A$ = −40 to +85°C)", and "G: Industrial applications (T$_A$ = −40 to +105°C)"

　　　　**2.**　Products only for "A: Consumer applications (T$_A$ = −40 to +85°C)", and "D: Industrial applications (T$_A$ = −40 to +85°C)"

## 1.3 Pin Configuration (Top View)

### 1.3.1 20-pin products
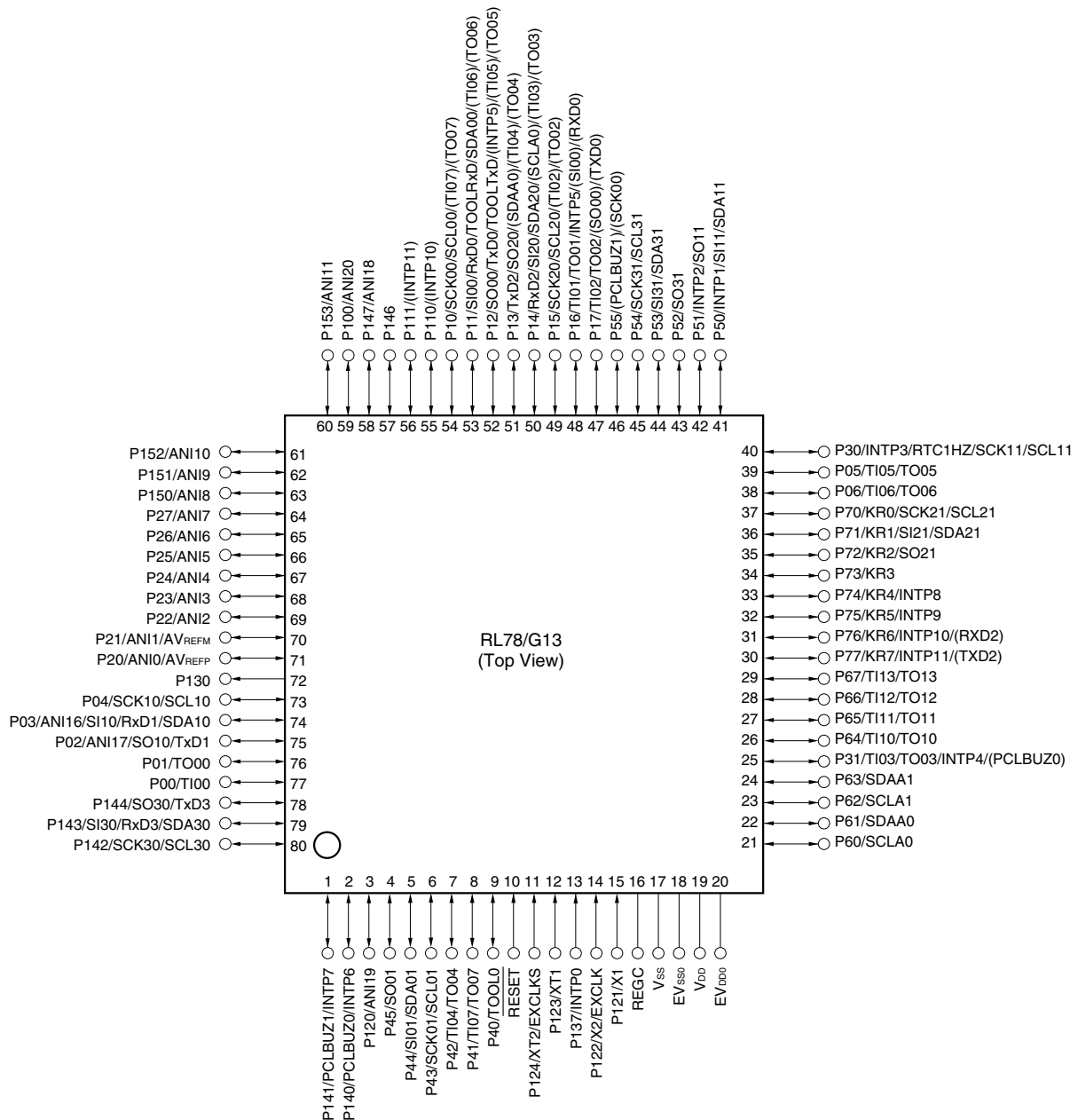
- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Pin layout (RL78/G13 Top View):

Left side (pins 1–10):
1. P01/ANI16/TO00/RxD1
2. P00/ANI17/TI00/TxD1
3. P40/TOOL0
4. $\overline{\text{RESET}}$
5. P137/INTP0
6. P122/X2/EXCLK
7. P121/X1
8. REGC
9. $V_{SS}$
10. $V_{DD}$

Right side (pins 20–11):
20. P20/ANI0/AV$_{REFP}$
19. P21/ANI1/AV$_{REFM}$
18. P22/ANI2
17. P147/ANI18
16. P10/SCK00/SCL00
15. P11/SI00/RxD0/TOOLRxD/SDA00
14. P12/SO00/TxD0/TOOLTxD
13. P16/TI01/TO01/INTP5/SO11
12. P17/TI02/TO02/SI11/SDA11
11. P30/INTP3/SCK11/SCL11

**Caution**    **Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).**

**Remark**    For pin identification, see **1.4 Pin Identification**.

### 1.3.12  80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
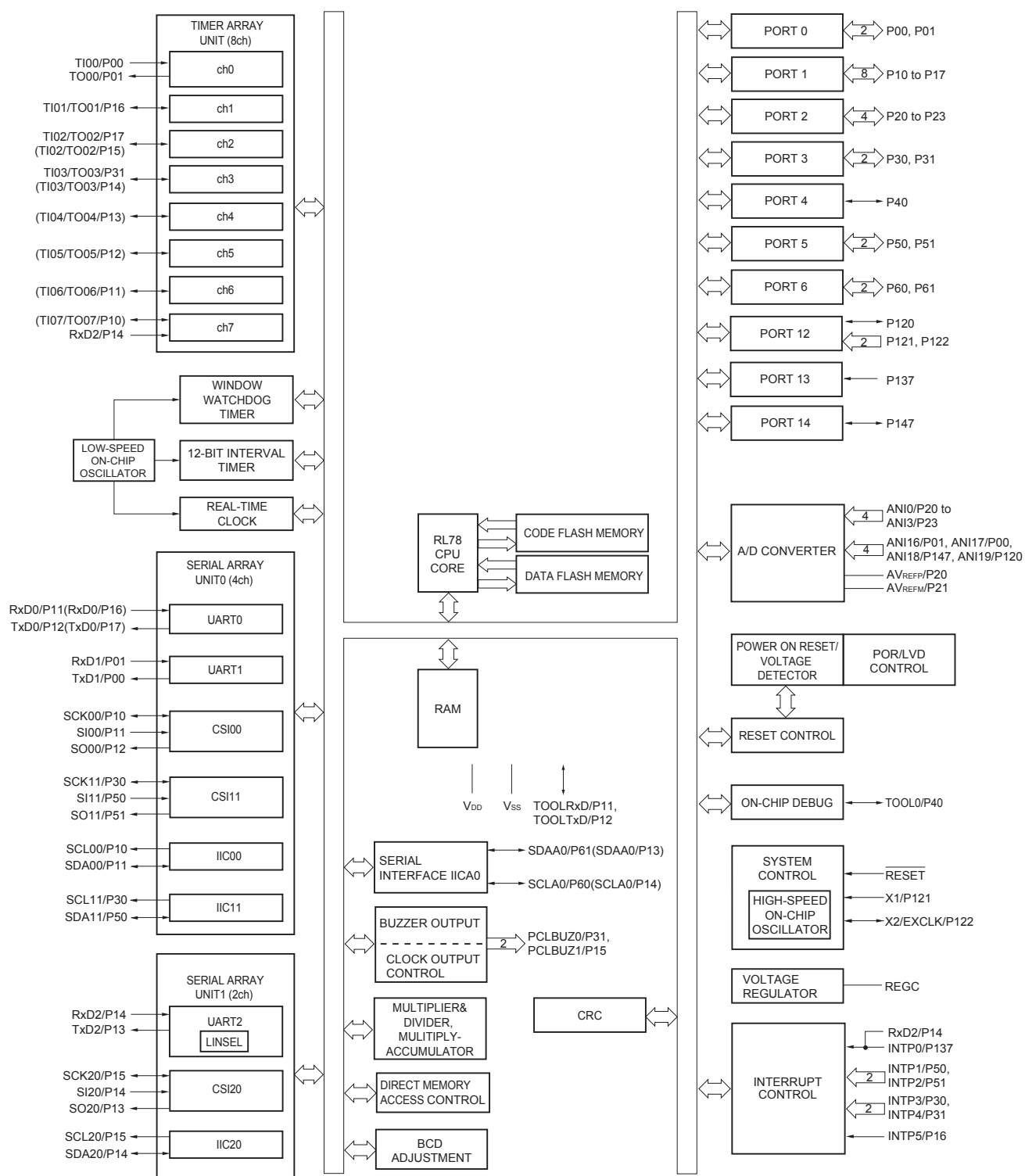- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

RL78/G13 (Top View)

Top pins (60–41):
- 60 P153/ANI11
- 59 P100/ANI20
- 58 P147/ANI18
- 57 P146
- 56 P111/(INTP11)
- 55 P110/(INTP10)
- 54 P10/SCK00/SCL00/(TI07)/(TO07)
- 53 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 52 P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)
- 51 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 50 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 49 P15/SCK20/SCL20/(TI02)/(TO02)
- 48 P16/TI01/TO01/INTP5/(SI00)/(RXD0)
- 47 P17/TI02/TO02/(SO00)/(TXD0)
- 46 P55/(PCLBUZ1)/(SCK00)
- 45 P54/SCK31/SCL31
- 44 P53/SI31/SDA31
- 43 P52/SO31
- 42 P51/INTP2/SO11
- 41 P50/INTP1/SI11/SDA11

Left pins (61–80):
- 61 P152/ANI10
- 62 P151/ANI9
- 63 P150/ANI8
- 64 P27/ANI7
- 65 P26/ANI6
- 66 P25/ANI5
- 67 P24/ANI4
- 68 P23/ANI3
- 69 P22/ANI2
- 70 P21/ANI1/AVREFM
- 71 P20/ANI0/AVREFP
- 72 P130
- 73 P04/SCK10/SCL10
- 74 P03/ANI16/SI10/RxD1/SDA10
- 75 P02/ANI17/SO10/TxD1
- 76 P01/TO00
- 77 P00/TI00
- 78 P144/SO30/TxD3
- 79 P143/SI30/RxD3/SDA30
- 80 P142/SCK30/SCL30

Right pins (40–21):
- 40 P30/INTP3/RTC1HZ/SCK11/SCL11
- 39 P05/TI05/TO05
- 38 P06/TI06/TO06
- 37 P70/KR0/SCK21/SCL21
- 36 P71/KR1/SI21/SDA21
- 35 P72/KR2/SO21
- 34 P73/KR3
- 33 P74/KR4/INTP8
- 32 P75/KR5/INTP9
- 31 P76/KR6/INTP10/(RXD2)
- 30 P77/KR7/INTP11/(TXD2)
- 29 P67/TI13/TO13
- 28 P66/TI12/TO12
- 27 P65/TI11/TO11
- 26 P64/TI10/TO10
- 25 P31/TI03/TO03/INTP4/(PCLBUZ0)
- 24 P63/SDAA1
- 23 P62/SCLA1
- 22 P61/SDAA0
- 21 P60/SCLA0

Bottom pins (1–20):
- 1 P141/PCLBUZ1/INTP7
- 2 P140/PCLBUZ0/INTP6
- 3 P120/ANI19
- 4 P45/SO01
- 5 P44/SI01/SDA01
- 6 P43/SCK01/SCL01
- 7 P42/TI04/TO04
- 8 P41/TI07/TO07
- 9 P40/TOOL0
- 10 RESET
- 11 P124/XT2/EXCLKS
- 12 P123/XT1
- 13 P137/INTP0
- 14 P122/X2/EXCLK
- 15 P121/X1
- 16 REGC
- 17 VSS
- 18 EVSS0
- 19 VDD
- 20 EVDD0

**Cautions 1. Make EVSS0 pin the same potential as VSS pin.**

**2. Make VDD pin the potential that is higher than EVDD0 pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

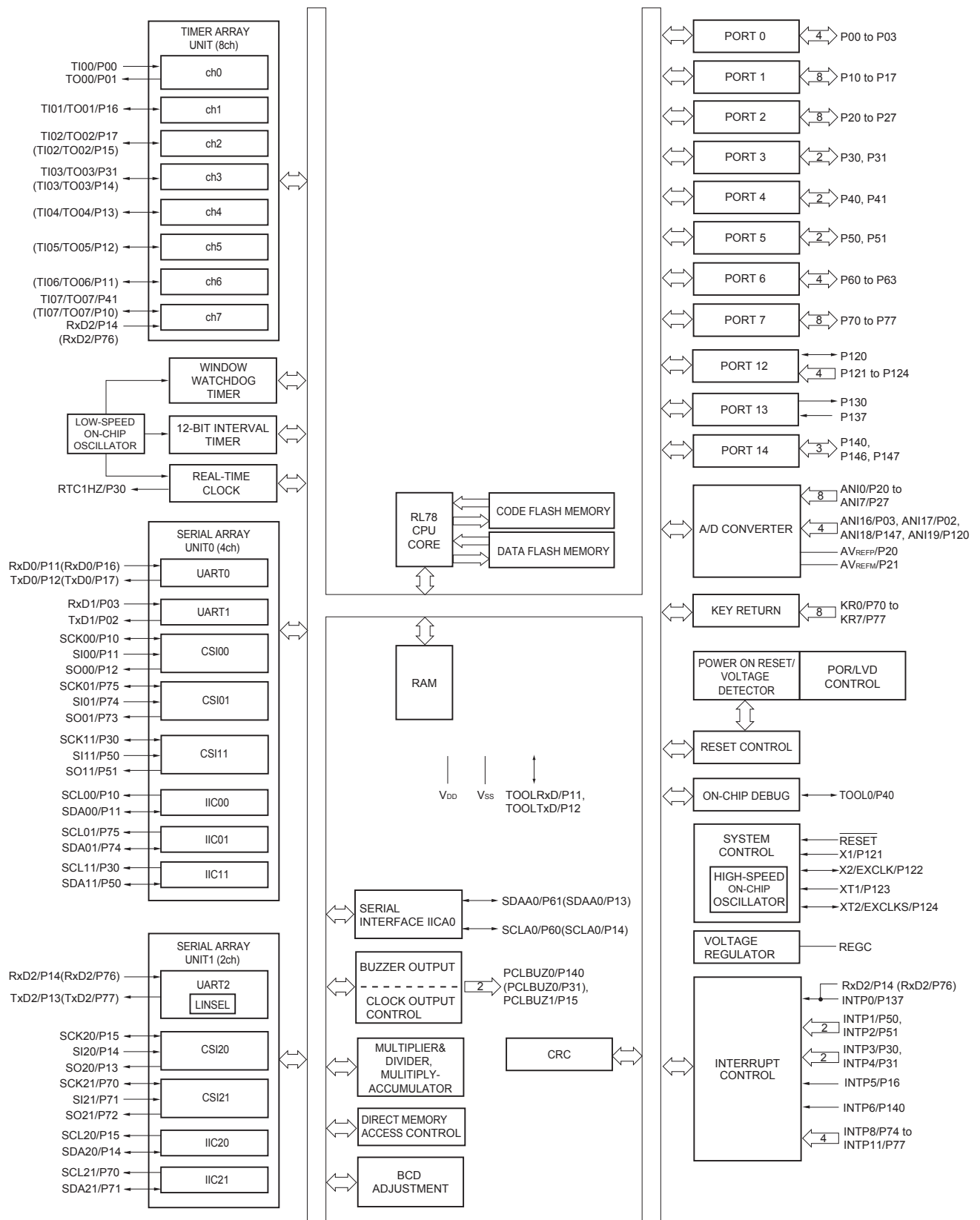**Remarks 1.** For pin identification, see **1.4  Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.4  30-pin products



**Remark**  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.10  52-pin products

TIMER ARRAY UNIT (8ch)
- TI00/P00, TO00/P01 — ch0
- TI01/TO01/P16 — ch1
- TI02/TO02/P17 (TI02/TO02/P15) — ch2
- TI03/TO03/P31 (TI03/TO03/P14) — ch3
- (TI04/TO04/P13) — ch4
- (TI05/TO05/P12) — ch5
- (TI06/TO06/P11) — ch6
- TI07/TO07/P41 (TI07/TO07/P10) — ch7
- RxD2/P14 (RxD2/P76)

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR → 12-BIT INTERVAL TIMER

RTC1HZ/P30 → REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)
- RxD0/P11(RxD0/P16), TxD0/P12(TxD0/P17) — UART0
- RxD1/P03, TxD1/P02 — UART1
- SCK00/P10, SI00/P11, SO00/P12 — CSI00
- SCK01/P75, SI01/P74, SO01/P73 — CSI01
- SCK11/P30, SI11/P50, SO11/P51 — CSI11
- SCL00/P10, SDA00/P11 — IIC00
- SCL01/P75, SDA01/P74 — IIC01
- SCL11/P30, SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)
- RxD2/P14(RxD2/P76), TxD2/P13(TxD2/P77) — UART2 (LINSEL)
- SCK20/P15, SI20/P14, SO20/P13 — CSI20
- SCK21/P70, SI21/P71, SO21/P72 — CSI21
- SCL20/P15, SDA20/P14 — IIC20
- SCL21/P70, SDA21/P71 — IIC21

RL78 CPU CORE
- CODE FLASH MEMORY
- DATA FLASH MEMORY

RAM

VDD, VSS, TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 → SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL → 2 → PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 4 — P00 to P03
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 2 — P40, P41
PORT 5 — 2 — P50, P51
PORT 6 — 4 — P60 to P63
PORT 7 — 8 — P70 to P77
PORT 12 — P120, 4 — P121 to P124
PORT 13 — P130, P137
PORT 14 — 3 — P140, P146, P147

A/D CONVERTER
- 8 — ANI0/P20 to ANI7/P27
- 4 — ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120
- AVREFP/P20
- AVREFM/P21

KEY RETURN — 8 — KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL / HIGH-SPEED ON-CHIP OSCILLATOR
- RESET
- X1/P121
- X2/EXCLK/P122
- XT1/P123
- XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- RxD2/P14 (RxD2/P76)
- INTP0/P137
- 2 — INTP1/P50, INTP2/P51
- 2 — INTP3/P30, INTP4/P31
- INTP5/P16
- INTP6/P140
- 4 — INTP8/P74 to INTP11/P77

**Remark**  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 2.1 Absolute Maximum Ratings

**Absolute Maximum Ratings (T$_A$ = 25°C) (1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | V$_{DD}$ | | −0.5 to +6.5 | V |
| | EV$_{DD0}$, EV$_{DD1}$ | EV$_{DD0}$ = EV$_{DD1}$ | −0.5 to +6.5 | V |
| | EV$_{SS0}$, EV$_{SS1}$ | EV$_{SS0}$ = EV$_{SS1}$ | −0.5 to +0.3 | V |
| REGC pin input voltage | V$_{IREGC}$ | REGC | −0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1] | V |
| Input voltage | V$_{I1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| | V$_{I2}$ | P60 to P63 (N-ch open-drain) | −0.3 to +6.5 | V |
| | V$_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| Output voltage | V$_{O1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3 [Note 2] | V |
| | V$_{O2}$ | P20 to P27, P150 to P156 | −0.3 to V$_{DD}$ +0.3 [Note 2] | V |
| Analog input voltage | V$_{AI1}$ | ANI16 to ANI26 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3] | V |
| | V$_{AI2}$ | ANI0 to ANI14 | −0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3] | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

    **2.** Must be 6.5 V or lower.

    **3.** Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin**.**

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

    **2.** AV$_{REF}$ (+) : + side reference voltage of the A/D converter.

    **3.** V$_{SS}$ : Reference voltage

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency (f$_X$)**Note** | Ceramic resonator/ crystal resonator | 2.7 V ≤ V$_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ V$_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ V$_{DD}$ < 2.4 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ V$_{DD}$ < 1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency (f$_X$)**Note** | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note**  Indicates only permissible oscillator frequency ranges.  Refer to AC Characteristics for instruction execution time.  Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution**   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark**   When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

### 2.2.2 On-chip oscillator characteristics

**(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency **Notes 1, 2** | f$_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | −20 to +85 °C | 1.8 V ≤ V$_{DD}$ ≤ 5.5 V | −1.0 | | +1.0 | % |
| | | | 1.6 V ≤ V$_{DD}$ < 1.8 V | −5.0 | | +5.0 | % |
| | | −40 to −20 °C | 1.8 V ≤ V$_{DD}$ ≤ 5.5 V | −1.5 | | +1.5 | % |
| | | | 1.6 V ≤ V$_{DD}$ < 1.8 V | −5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | f$_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | −15 | | +15 | % |

**Notes 1.**  High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

  **2.**  This indicates the oscillator characteristics only.  Refer to AC Characteristics for instruction execution time.

**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | V$_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −10.0 mA | EV$_{DD0}$ − 1.5 | | | V |
| | | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA | EV$_{DD0}$ − 0.7 | | | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA | EV$_{DD0}$ − 0.6 | | | V |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA | EV$_{DD0}$ − 0.5 | | | V |
| | | | 1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OH1}$ = −1.0 mA | EV$_{DD0}$ − 0.5 | | | V |
| | V$_{OH2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 $\mu$A | V$_{DD}$ − 0.5 | | | V |
| Output voltage, low | V$_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 20 mA | | | 1.3 | V |
| | | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | V$_{OL2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 $\mu$A | | | 0.4 | V |
| | V$_{OL3}$ | P60 to P63 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution** **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/2)**

| Parameter | Symbol | | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | I$_{DD2}$ [Note 2] | HALT mode | HS (high-speed main) mode[Note 7] | f$_{IH}$ = 32 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.54 | 1.63 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.54 | 1.63 | mA |
| | | | | f$_{IH}$ = 24 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.44 | 1.28 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.44 | 1.28 | mA |
| | | | | f$_{IH}$ = 16 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.40 | 1.00 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.40 | 1.00 | mA |
| | | | LS (low-speed main) mode[Note 7] | f$_{IH}$ = 8 MHz [Note 4] | V$_{DD}$ = 3.0 V | | 260 | 530 | μA |
| | | | | | V$_{DD}$ = 2.0 V | | 260 | 530 | μA |
| | | | LV (low-voltage main) mode [Note 7] | f$_{IH}$ = 4 MHz [Note 4] | V$_{DD}$ = 3.0 V | | 420 | 640 | μA |
| | | | | | V$_{DD}$ = 2.0 V | | 420 | 640 | μA |
| | | | HS (high-speed main) mode[Note 7] | f$_{MX}$ = 20 MHz[Note 3], V$_{DD}$ = 5.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | f$_{MX}$ = 20 MHz[Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 0.28 | 1.00 | mA |
| | | | | | Resonator connection | | 0.45 | 1.17 | mA |
| | | | | f$_{MX}$ = 10 MHz[Note 3], V$_{DD}$ = 5.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | | f$_{MX}$ = 10 MHz[Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 0.19 | 0.60 | mA |
| | | | | | Resonator connection | | 0.26 | 0.67 | mA |
| | | | LS (low-speed main) mode[Note 7] | f$_{MX}$ = 8 MHz[Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | | f$_{MX}$ = 8 MHz[Note 3], V$_{DD}$ = 2.0 V | Square wave input | | 95 | 330 | μA |
| | | | | | Resonator connection | | 145 | 380 | μA |
| | | | Subsystem clock operation | f$_{SUB}$ = 32.768 kHz[Note 5] T$_A$ = −40°C | Square wave input | | 0.25 | 0.57 | μA |
| | | | | | Resonator connection | | 0.44 | 0.76 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz[Note 5] T$_A$ = +25°C | Square wave input | | 0.30 | 0.57 | μA |
| | | | | | Resonator connection | | 0.49 | 0.76 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz[Note 5] T$_A$ = +50°C | Square wave input | | 0.37 | 1.17 | μA |
| | | | | | Resonator connection | | 0.56 | 1.36 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz[Note 5] T$_A$ = +70°C | Square wave input | | 0.53 | 1.97 | μA |
| | | | | | Resonator connection | | 0.72 | 2.16 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz[Note 5] T$_A$ = +85°C | Square wave input | | 0.82 | 3.37 | μA |
| | | | | | Resonator connection | | 1.01 | 3.56 | μA |
| | I$_{DD3}$ [Note 6] | STOP mode[Note 8] | T$_A$ = −40°C | | | | 0.18 | 0.50 | μA |
| | | | T$_A$ = +25°C | | | | 0.23 | 0.50 | μA |
| | | | T$_A$ = +50°C | | | | 0.30 | 1.10 | μA |
| | | | T$_A$ = +70°C | | | | 0.46 | 1.90 | μA |
| | | | T$_A$ = +85°C | | | | 0.75 | 3.30 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

**(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | I$_{DD2}$ [Note 2] | HALT mode | HS (high-speed main) mode [Note 7] | f$_{IH}$ = 32 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.62 | 1.86 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.62 | 1.86 | mA |
| | | | | f$_{IH}$ = 24 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.50 | 1.45 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.50 | 1.45 | mA |
| | | | | f$_{IH}$ = 16 MHz [Note 4] | V$_{DD}$ = 5.0 V | | 0.44 | 1.11 | mA |
| | | | | | V$_{DD}$ = 3.0 V | | 0.44 | 1.11 | mA |
| | | | LS (low-speed main) mode [Note 7] | f$_{IH}$ = 8 MHz [Note 4] | V$_{DD}$ = 3.0 V | | 290 | 620 | $\mu$A |
| | | | | | V$_{DD}$ = 2.0 V | | 290 | 620 | $\mu$A |
| | | | LV (low-voltage main) mode [Note 7] | f$_{IH}$ = 4 MHz [Note 4] | V$_{DD}$ = 3.0 V | | 440 | 680 | $\mu$A |
| | | | | | V$_{DD}$ = 2.0 V | | 440 | 680 | $\mu$A |
| | | | HS (high-speed main) mode [Note 7] | f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 0.31 | 1.08 | mA |
| | | | | | Resonator connection | | 0.48 | 1.28 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 0.21 | 0.63 | mA |
| | | | | | Resonator connection | | 0.28 | 0.71 | mA |
| | | | LS (low-speed main) mode [Note 7] | f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V | Square wave input | | 110 | 360 | $\mu$A |
| | | | | | Resonator connection | | 160 | 420 | $\mu$A |
| | | | | f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V | Square wave input | | 110 | 360 | $\mu$A |
| | | | | | Resonator connection | | 160 | 420 | $\mu$A |
| | | | Subsystem clock operation | f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C | Square wave input | | 0.28 | 0.61 | $\mu$A |
| | | | | | Resonator connection | | 0.47 | 0.80 | $\mu$A |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C | Square wave input | | 0.34 | 0.61 | $\mu$A |
| | | | | | Resonator connection | | 0.53 | 0.80 | $\mu$A |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C | Square wave input | | 0.41 | 2.30 | $\mu$A |
| | | | | | Resonator connection | | 0.60 | 2.49 | $\mu$A |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C | Square wave input | | 0.64 | 4.03 | $\mu$A |
| | | | | | Resonator connection | | 0.83 | 4.22 | $\mu$A |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C | Square wave input | | 1.09 | 8.04 | $\mu$A |
| | | | | | Resonator connection | | 1.28 | 8.23 | $\mu$A |
| | I$_{DD3}$ [Note 6] | STOP mode [Note 8] | T$_A$ = −40°C | | | | 0.19 | 0.52 | $\mu$A |
| | | | T$_A$ = +25°C | | | | 0.25 | 0.52 | $\mu$A |
| | | | T$_A$ = +50°C | | | | 0.32 | 2.21 | $\mu$A |
| | | | T$_A$ = +70°C | | | | 0.55 | 3.94 | $\mu$A |
| | | | T$_A$ = +85°C | | | | 1.00 | 7.95 | $\mu$A |

(**Notes** and **Remarks** are listed on the next page.)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | | $f_{MCK}$/6 Note 1 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | $f_{MCK}$/6 Notes 1 to 3 | | $f_{MCK}$/6 Notes 1, 2 | | $f_{MCK}$/6 Notes 1, 2 | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $EV_{DD0}$≥$V_b$.

**3.** The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.

2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

**4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

HS (high-speed main) mode:　　　32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)

　　　　　　　　　　　　　　　　16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)

LS (low-speed main) mode:　　　8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)

LV (low-voltage main) mode:　　4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution**　**Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.**　$V_b$[V]: Communication line voltage

**2.**　q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.**　$f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

**4.**　UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SIp setup time (to SCKp↑) [Note 1] | t$_{SIK1}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 81 | | 479 | | 479 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 177 | | 479 | | 479 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 479 | | 479 | | 479 | | ns |
| SIp hold time (from SCKp↑) [Note 1] | t$_{KSI1}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 19 | | 19 | | 19 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 19 | | 19 | | 19 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 19 | | 19 | | 19 | | ns |
| Delay time from SCKp↓ to SOp output [Note 1] | t$_{KSO1}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | | 100 | | 100 | | 100 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | | 195 | | 195 | | 195 | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | | 483 | | 483 | | 483 | ns |

Notes    1.   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2.   Use it with EV$_{DD0}$ ≥ V$_b$.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the page after the next page.)

**(2) When reference voltage (+) = $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, 1.6 V ≤ $AV_{REFP}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (–) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | 1.2 | ±8.5 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution Target ANI pin : ANI16 to ANI26 | 3.6 V ≤ $V_{DD}$ ≤ 5.5 V | 2.125 | | 39 | $\mu$s |
| | | | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | $\mu$s |
| | | | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | $\mu$s |
| | | | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V | 57 | | 95 | $\mu$s |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±0.60 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±6.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution $EV_{DD0}$ = $AV_{REFP}$ = $V_{DD}$ [Notes 3, 4] | 1.8 V ≤ $AV_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| | | | 1.6 V ≤ $AV_{REFP}$ ≤ 5.5 V [Note 5] | | | ±2.5 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI16 to ANI26 | | 0 | | $AV_{REFP}$ and $EV_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

    **2.** This value is indicated as a ratio (%FSR) to the full-scale value.

    **3.** When $AV_{REFP}$ < $V_{DD}$, the MAX. values are as follows.

        Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

        Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

        Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

    **4.** When $AV_{REFP}$ < $EV_{DD0}$ ≤ $V_{DD}$, the MAX. values are as follows.

        Overall error: Add ±4.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

        Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

        Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when $AV_{REFP}$ = $V_{DD}$.

    **5.** When the conversion time is set to 57 $\mu$s (min.) and 95 $\mu$s (max.).

**Notes 1.** Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$.  The values below the MAX. column include the peripheral operation current.  However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped.  When AMPHS1 = 1 (Ultra-low power consumption oscillation).  However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode:  2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

**Remarks 1.** f$_{MX}$:  High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** f$_{IH}$:  High-speed on-chip oscillator clock frequency

**3.** f$_{SUB}$:  Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

**Notes 1.** Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$.  The values below the MAX. column include the peripheral operation current.  However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped.  When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).  The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode:  2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

                                           2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.


**Remarks 1.** f$_{MX}$:  High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** f$_{IH}$:  High-speed on-chip oscillator clock frequency

**3.** f$_{SUB}$:  Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

**(5)  Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}$/12 [Note 1] | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}$/12 [Note 1] | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |
| | | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}$/12 [Notes 1,2] | bps |
| | | | | Theoretical value of the maximum transfer rate $f_{CLK}$ = 32 MHz, $f_{MCK}$ = $f_{CLK}$ | | 2.6 | Mbps |

**Notes 1.**  Transfer rate in the SNOOZE mode is 4800 bps only.

**2.**  The following conditions are required for low voltage interface when $EV_{DD0}$ < $V_{DD}$.

2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

**Caution**   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.**  $V_b$[V]: Communication line voltage

**2.**  q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.**  $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**4.**  UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**

**(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↓) [Note] | t$_{SIK1}$ | 4.0 V ≤ EV$_{DD}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 88 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 88 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 220 | | ns |
| SIp hold time (from SCKp↓) [Note] | t$_{KSI1}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | 38 | | ns |
| Delay time from SCKp↑ to SOp output [Note] | t$_{KSO1}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | | 50 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | | 50 | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | | 50 | ns |

**Note**    When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution   Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**Notes 1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

    **2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    **3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    **4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.  The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

**CSI mode connection diagram (during communication at different potential)**
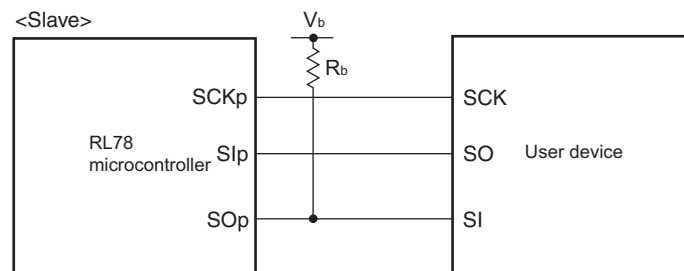


**Remarks 1.** R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

    **2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02,

        10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

    **3.** f$_{MCK}$: Serial array unit operation clock frequency

        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

        m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

    **4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

### 3.5.2 Serial interface IICA

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Standard Mode | | Fast Mode | | |
| | | | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK}$ ≥ 3.5 MHz | – | – | 0 | 400 | kHz |
| | | Standard mode: $f_{CLK}$ ≥ 1 MHz | 0 | 100 | – | – | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | | 4.7 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | | 4.0 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | | 4.7 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | | 4.0 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | | 250 | | 100 | | ns |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | | 0 | 3.45 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | | 4.0 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | | 4.7 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

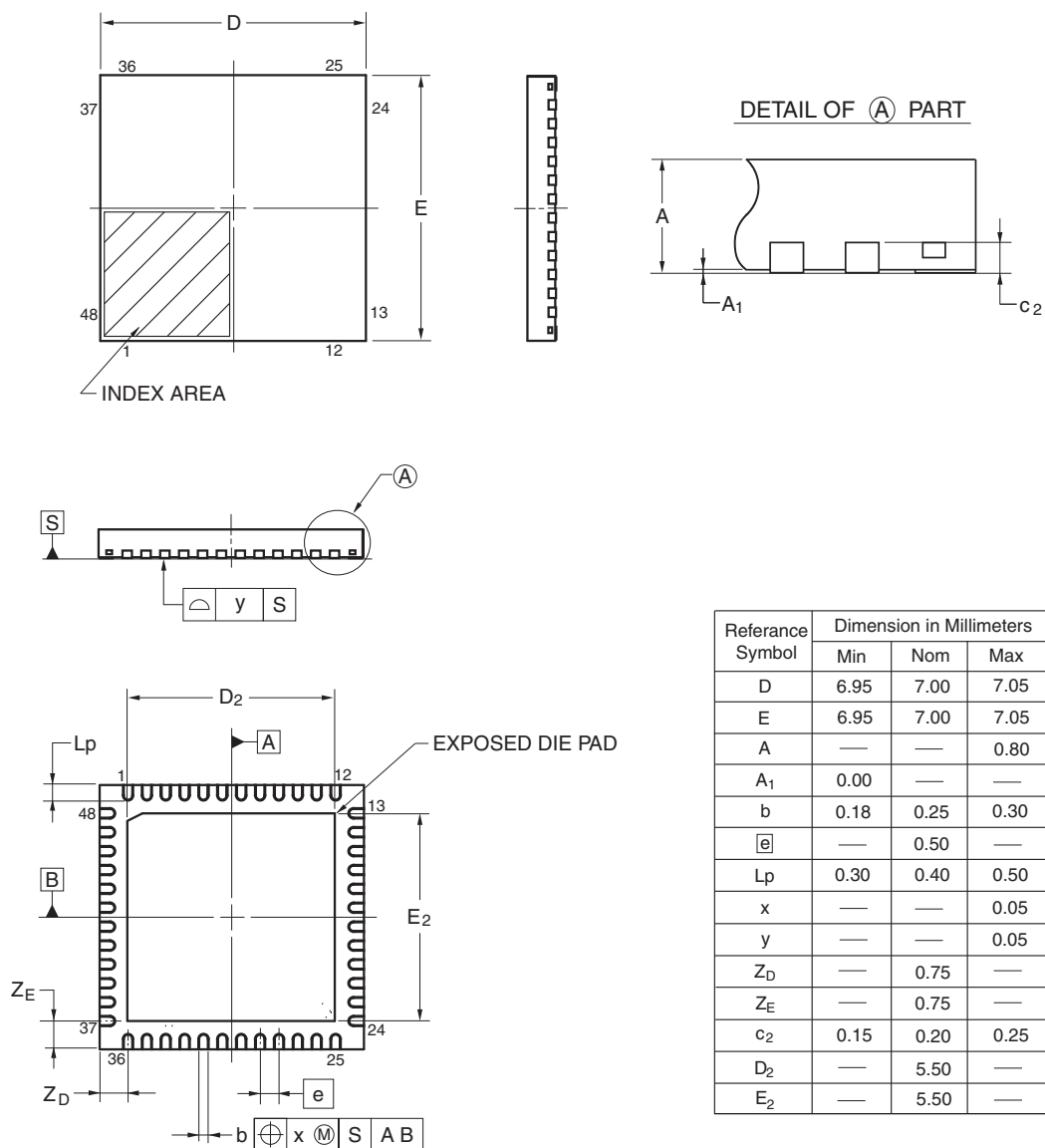Standard mode:   $C_b$ = 400 pF, $R_b$ = 2.7 kΩ
Fast mode:        $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

**IICA serial transfer timing**
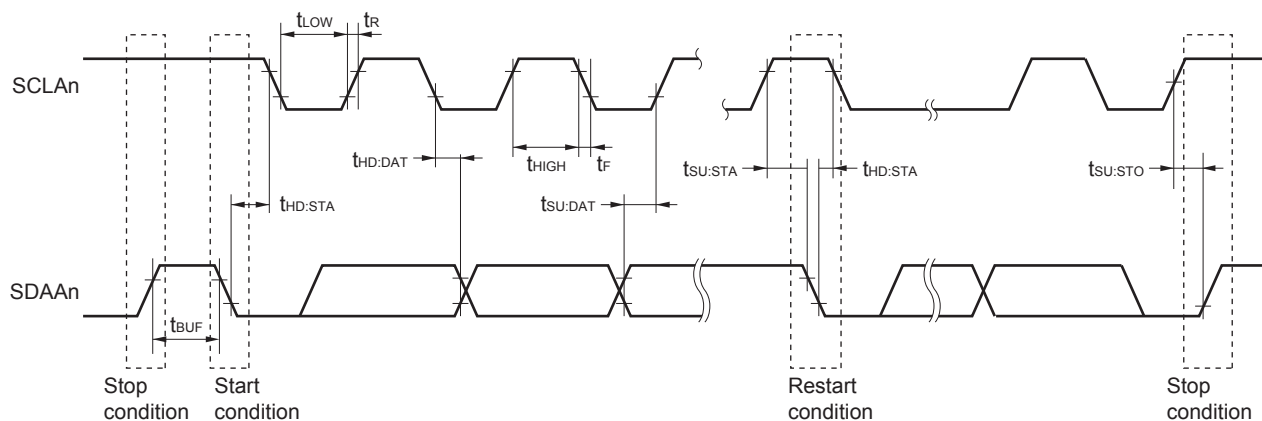


**Remark**    n = 0, 1

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
R5F100GHGNA, R5F100GJGNA

| JEITA Package code | RENESAS code | Previous code | MASS(TYP.)[g] |
|---|---|---|---|
| P-HWQFN48-7x7-0.50 | PWQN0048KB-A | 48PJN-A<br>P48K8-50-5B4-6 | 0.13 |

DETAIL OF $Ⓐ$ PART

INDEX AREA

EXPOSED DIE PAD

| Referance<br>Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 6.95 | 7.00 | 7.05 |
| E | 6.95 | 7.00 | 7.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| $\boxed{e}$ | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 5.50 | — |
| $E_2$ | — | 5.50 | — |