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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

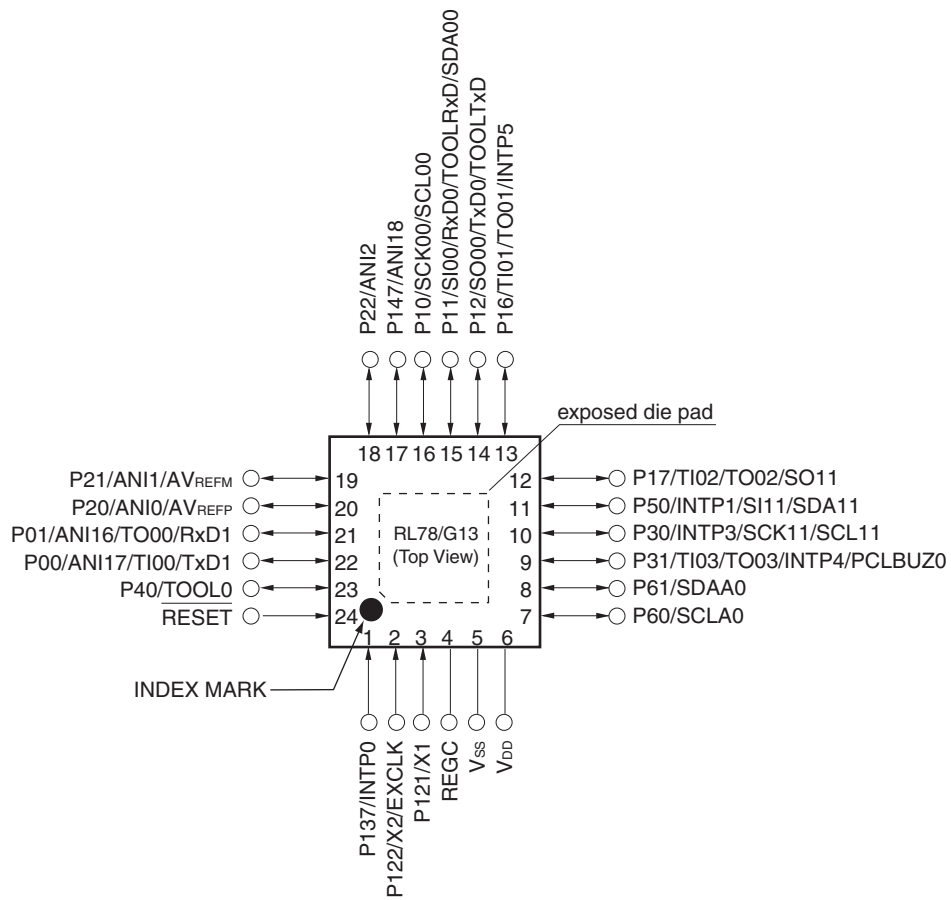| Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lgafb-50

Table 1-1. List of Ordering Part Numbers

(2/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
25 pins	25-pin plastic WFLGA (3 × 3 mm, 0.5 mm pitch)	Mounted	A	R5F1008AALA#U0, R5F1008CALA#U0, R5F1008DALA#U0, R5F1008EALA#U0 R5F1008AALA#W0, R5F1008CALA#W0, R5F1008DALA#W0, R5F1008EALA#W0
			G	R5F1008AGLA#U0, R5F1008CGLA#U0, R5F1008DGLA#U0, R5F1008EGLA#U0 R5F1008AGLA#W0, R5F1008CGLA#W0, R5F1008DGLA#W0, R5F1008EGLA#W0
		Not mounted	A	R5F1018AALA#U0, R5F1018CALA#U0, R5F1018DALA#U0, R5F1018EALA#U0 R5F1018AALA#W0, R5F1018CALA#W0, R5F1018DALA#W0, R5F1018EALA#W0
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F100AAASP#V0, R5F100ACASP#V0, R5F100ADASP#V0, R5F100AEASP#V0, R5F100AFASP#V0, R5F100AGASP#V0 R5F100AAASP#X0, R5F100ACASP#X0, R5F100ADASP#X0, R5F100AEASP#X0, R5F100AFASP#X0, R5F100AGASP#X0
			D	R5F100AADSP#V0, R5F100ACDSP#V0, R5F100ADDSP#V0, R5F100AEDSP#V0, R5F100AFDSP#V0, R5F100AGDSP#V0 R5F100AADSP#X0, R5F100ACDSP#X0, R5F100ADDSP#X0, R5F100AEDSP#X0, R5F100AFDSP#X0, R5F100AGDSP#X0
			G	R5F100AAGSP#V0, R5F100ACGSP#V0, R5F100ADGSP#V0,R5F100AEGSP#V0, R5F100AFGSP#V0, R5F100AGGSP#V0 R5F100AAGSP#X0, R5F100ACGSP#X0, R5F100ADGSP#X0,R5F100AEGSP#X0, R5F100AFGSP#X0, R5F100AGGSP#X0
		Not mounted	A	R5F101AAASP#V0, R5F101ACASP#V0, R5F101ADASP#V0, R5F101AEASP#V0, R5F101AFASP#V0, R5F101AGASP#V0 R5F101AAASP#X0, R5F101ACASP#X0, R5F101ADASP#X0, R5F101AEASP#X0, R5F101AFASP#X0, R5F101AGASP#X0
			D	R5F101AADSP#V0, R5F101ACDSP#V0, R5F101ADDSP#V0, R5F101AEDSP#V0, R5F101AFDSP#V0, R5F101AGDSP#V0 R5F101AADSP#X0, R5F101ACDSP#X0, R5F101ADDSP#X0, R5F101AEDSP#X0, R5F101AFDSP#X0, R5F101AGDSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	Mounted	A	R5F100BAANA#U0, R5F100BCANA#U0, R5F100BDANA#U0, R5F100BEANA#U0, R5F100BFANA#U0, R5F100BGANA#U0 R5F100BAANA#W0, R5F100BCANA#W0, R5F100BDANA#W0, R5F100BEANA#W0, R5F100BFANA#W0, R5F100BGANA#W0
			D	R5F100BADNA#U0, R5F100BCDNA#U0, R5F100BDDNA#U0, R5F100BEDNA#U0, R5F100BFDNA#U0, R5F100BGDNA#U0 R5F100BADNA#W0, R5F100BCDNA#W0, R5F100BDDNA#W0, R5F100BEDNA#W0, R5F100BFDNA#W0, R5F100BGDNA#W0
			G	R5F100BAGNA#U0, R5F100BCGNA#U0, R5F100BDGNA#U0, R5F100BEGNA#U0, R5F100BFGNA#U0, R5F100BGGNA#U0 R5F100BAGNA#W0, R5F100BCGNA#W0, R5F100BDGNA#W0, R5F100BEGNA#W0, R5F100BFGNA#W0, R5F100BGGNA#W0
		Not mounted	A	R5F101BAANA#U0, R5F101BCANA#U0, R5F101BDANA#U0, R5F101BEANA#U0, R5F101BFANA#U0, R5F101BGANA#U0 R5F101BAANA#W0, R5F101BCANA#W0, R5F101BDANA#W0, R5F101BEANA#W0, R5F101BFANA#W0, R5F101BGANA#W0
			D	R5F101BADNA#U0, R5F101BCDNA#U0, R5F101BDDNA#U0, R5F101BEDNA#U0, R5F101BFDNA#U0, R5F101BGDNA#U0 R5F101BADNA#W0, R5F101BCDNA#W0, R5F101BDDNA#W0, R5F101BEDNA#W0, R5F101BFDNA#W0, R5F101BGDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 24-pin products
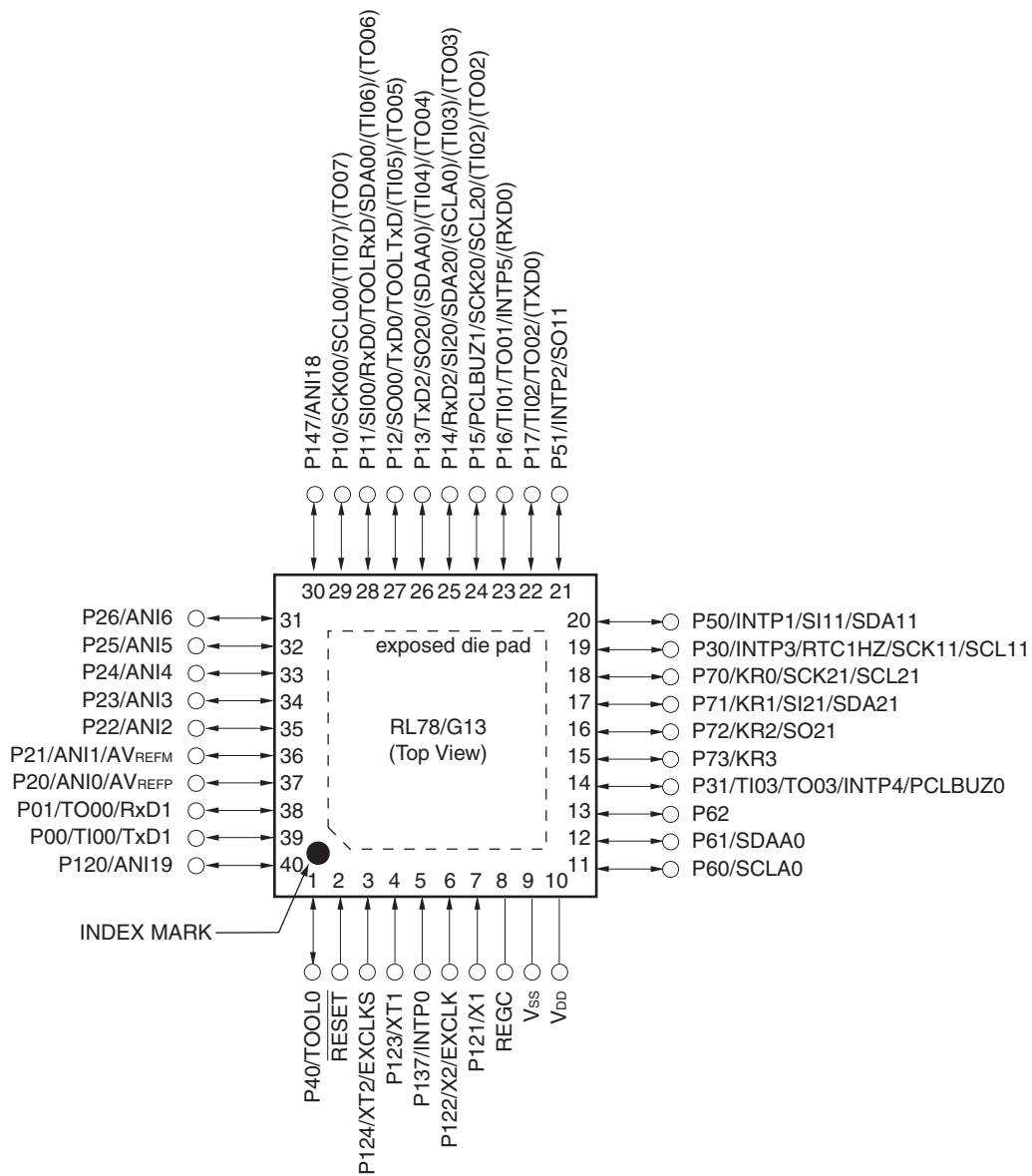
- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

Top labels (pins 18–13):
P22/ANI2
P147/ANI18
P10/SCK00/SCL00
P11/SI00/RxD0/TOOLRxD/SDA00
P12/SO00/TxD0/TOOLTxD
P16/TI01/TO01/INTP5

exposed die pad

RL78/G13
(Top View)

INDEX MARK

Left side:
P21/ANI1/AV$_{REFM}$ 19
P20/ANI0/AV$_{REFP}$ 20
P01/ANI16/TO00/RxD1 21
P00/ANI17/TI00/TxD1 22
P40/TOOL0 23
RESET 24

Top pins: 18 17 16 15 14 13
Bottom pins: 1 2 3 4 5 6

Right side:
12 P17/TI02/TO02/SO11
11 P50/INTP1/SI11/SDA11
10 P30/INTP3/SCK11/SCL11
9 P31/TI03/TO03/INTP4/PCLBUZ0
8 P61/SDAA0
7 P60/SCLA0

Bottom labels (pins 1–6):
P137/INTP0
P122/X2/EXCLK
P121/X1
REGC
V$_{SS}$
V$_{DD}$

Caution **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks 1. For pin identification, see **1.4 Pin Identification**.
    2. It is recommended to connect an exposed die pad to Vss.

1.3.7 40-pin products

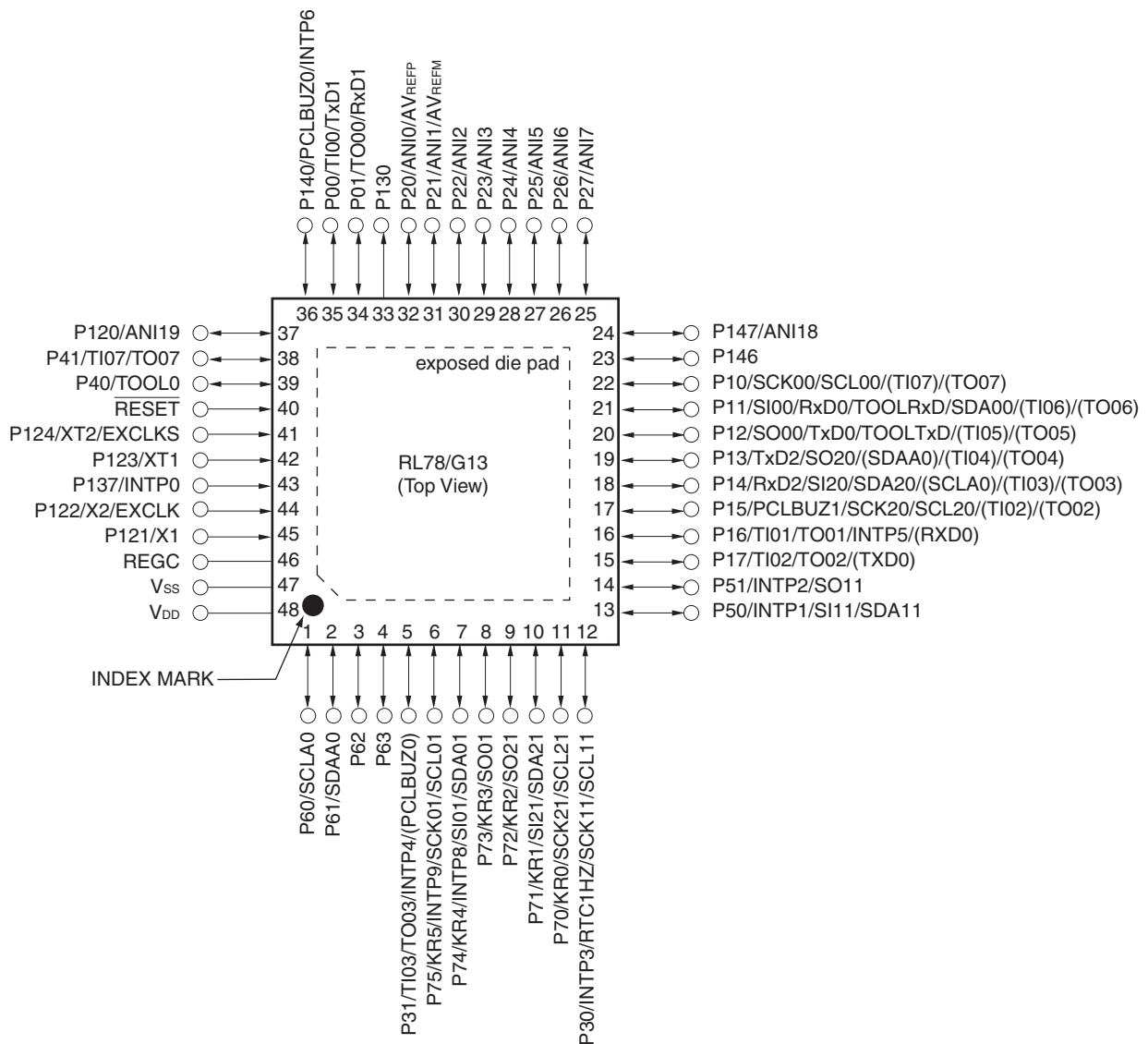- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to Vss.
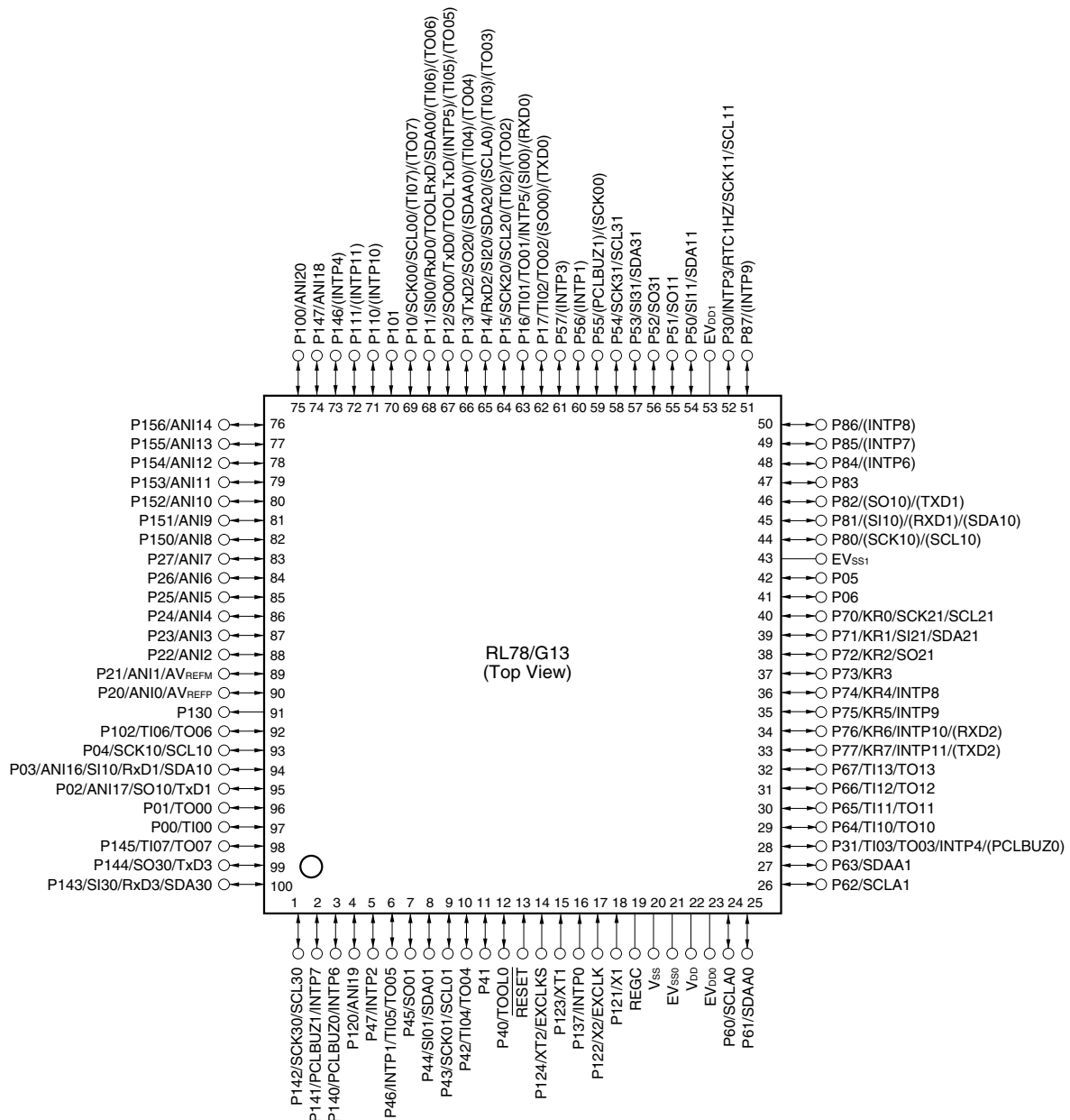
- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Top pins (left to right):
P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Pin numbers top: 36 35 34 33 32 31 30 29 28 27 26 25

Left side pins:
- 37 P120/ANI19
- 38 P41/TI07/TO07
- 39 P40/TOOL0
- 40 $\overline{\text{RESET}}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 V$_{SS}$
- 48 V$_{DD}$

exposed die pad

RL78/G13
(Top View)

INDEX MARK

Right side pins:
- 24 P147/ANI18
- 23 P146
- 22 P10/SCK00/SCL00/(TI07)/(TO07)
- 21 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 P16/TI01/TO01/INTP5/(RXD0)
- 15 P17/TI02/TO02/(TXD0)
- 14 P51/INTP2/SO11
- 13 P50/INTP1/SI11/SDA11

Pin numbers bottom: 1 2 3 4 5 6 7 8 9 10 11 12

Bottom pins (left to right):
P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

      2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

      3. It is recommended to connect an exposed die pad to Vss.
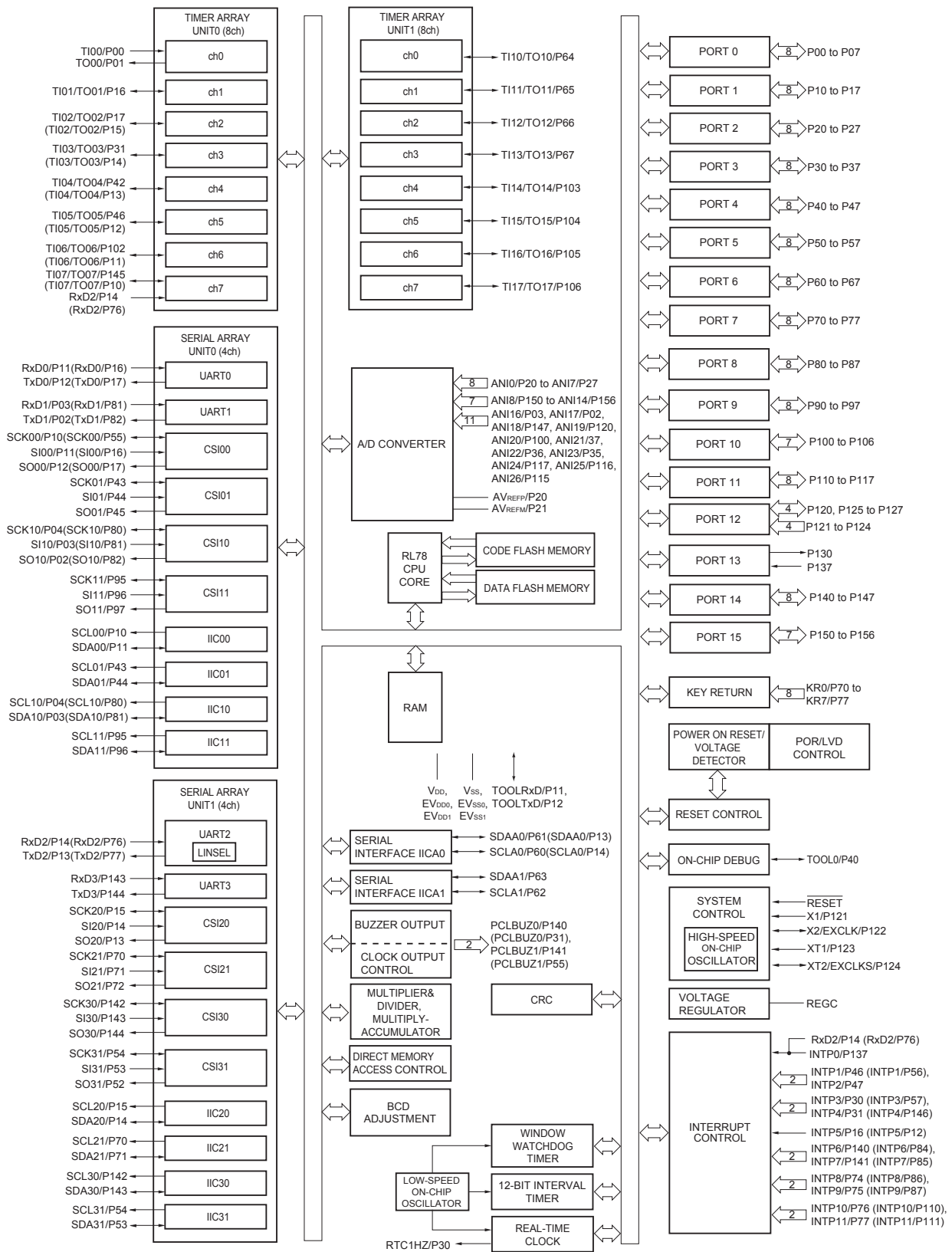
1.3.13　100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)

Cautions 1. Make EVSS0, EVSS1 pins the same potential as VSS pin.

2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the VSS, EVSS0 and EVSS1 pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products

Remark   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 16[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)									
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)									
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		31 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		34 (N-ch O.D. I/O [V_{DD} withstand voltage]: 11)		38 (N-ch O.D. I/O [V_{DD} withstand voltage]: 13)		48 (N-ch O.D. I/O [V_{DD} withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	–		–		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3 [Note2]), 8 channels (PWM outputs: 7 [Note2][Note3])		5 channels (PWM outputs: 4 [Note2]), 8 channels (PWM outputs: 7 [Note2]) [Note 3]						8 channels (PWM outputs: 7 [Note2])	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)									

Notes 1.   The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = E to G, J, L):   Start address FF300H
R5F100xE, R5F101xE (x = E to G, J, L):   Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L):   Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L):   Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −10.0 mA	EV$_{DD0}$ − 1.5			V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OH1}$ = −1.0 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 20 mA			1.3	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL1}$ = 0.3 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V
			1.6 V ≤ EV$_{DD0}$ < 5.5 V, I$_{OL3}$ = 1.0 mA			0.4	V

Caution **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
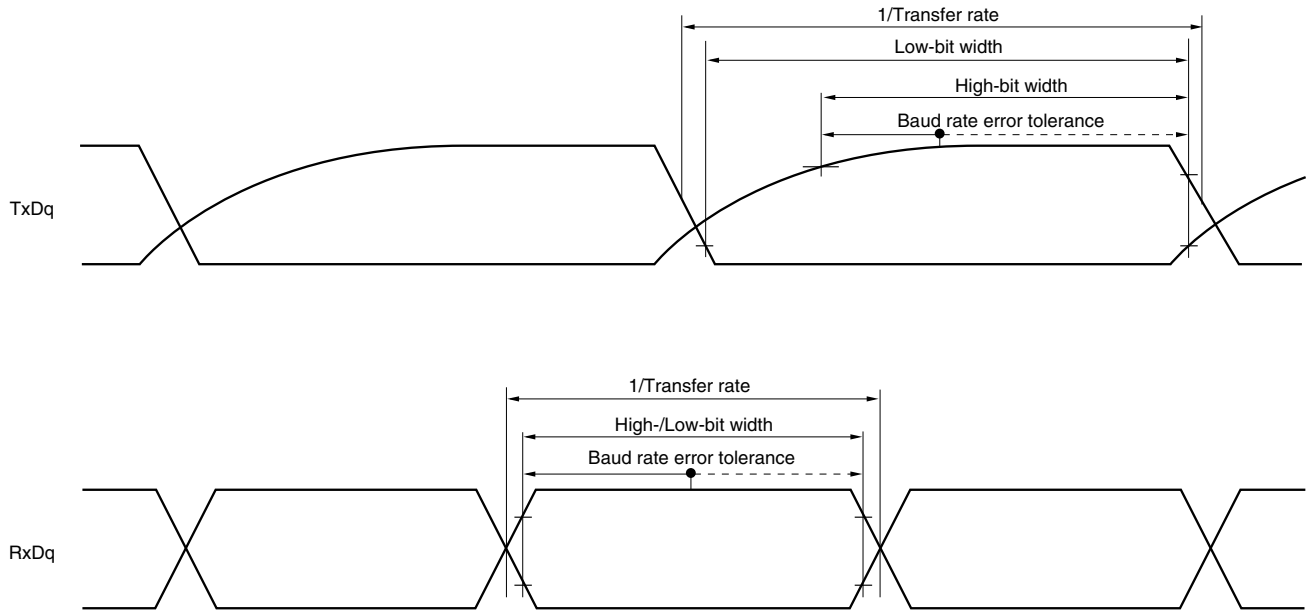
(4) Peripheral Functions (Common to all products)

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$ [Note 1]				0.20		μA
RTC operating current	I$_{RTC}$ [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I$_{IT}$ [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 5]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ [Notes 1, 6]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$ [Note 1]				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		μA
LVD operating current	I$_{LVI}$ [Notes 1, 7]				0.08		μA
Self-programming operating current	I$_{FSP}$ [Notes 1, 9]				2.50	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 8]				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed [Note 10]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V$_{DD}$.

   2. When high speed on-chip oscillator and high-speed system clock are stopped.

   3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added. I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

   4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

   5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

UART mode bit width (during communication at different potential) (reference)

TxDq

1/Transfer rate
Low-bit width
High-bit width
Baud rate error tolerance

RxDq

1/Transfer rate
High-/Low-bit width
Baud rate error tolerance

Remarks 1. $R_b[\Omega]$:Communication line (TxDq) pull-up resistance,

$C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} ≥ 4/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note], C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ − 75		$t_{KCY1}/2$ − 75		$t_{KCY1}/2$ − 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ − 170		$t_{KCY1}/2$ − 170		$t_{KCY1}/2$ − 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note], C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ − 458		$t_{KCY1}/2$ − 458		$t_{KCY1}/2$ − 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ − 12		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ − 18		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V[Note], C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		$t_{KCY1}/2$ − 50		ns

Note   Use it with EV_{DD0} ≥ V_b.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(Remarks are listed two pages after the next page.)

CSI mode connection diagram (during communication at different potential)

<Master>

RL78 microcontroller

SCKp — V_b — R_b — SCK
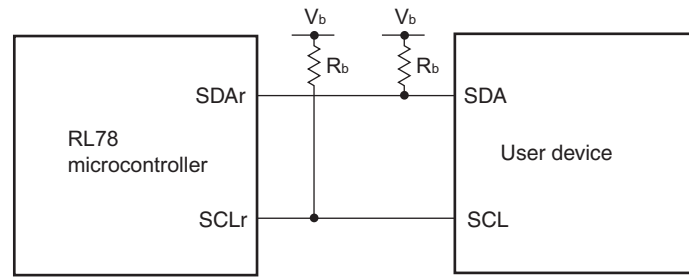
SIp — SO — User device

SOp — V_b — R_b — SI

Remarks 1. $R_b[\Omega]$:Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = −40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)
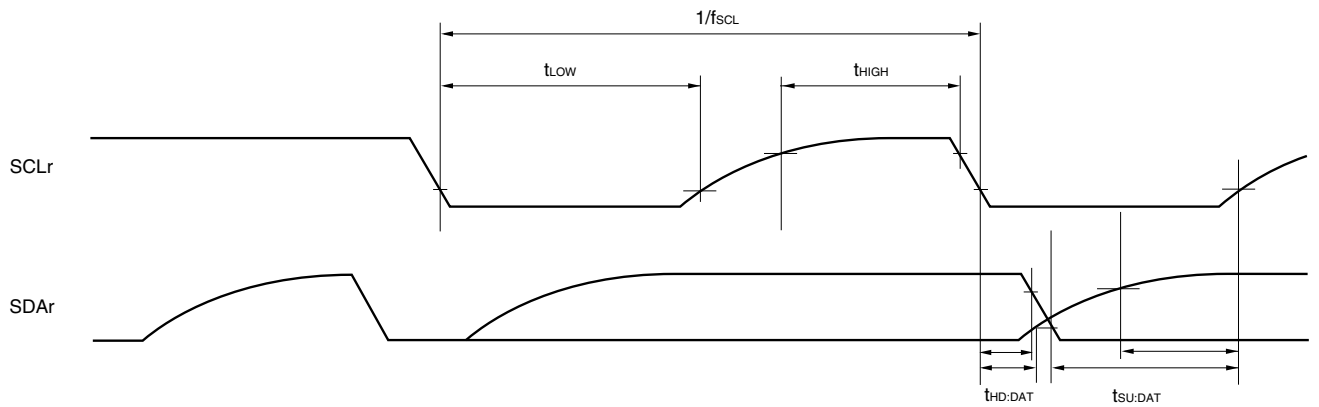
Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	14/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	20/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	24 MHz < f$_{MCK}$	48/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

Simplified I^{2}C mode connection diagram (during communication at different potential)

Simplified I^{2}C mode serial transfer timing (during communication at different potential)

Remarks **1.** R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr)
load capacitance, V$_b$[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01, 02, 10, 12, 13)

(2) I²C fast mode

(TA = −40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{CLK} \geq 3.5$ MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EVDD0 ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		100		100		100		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V		1.3		1.3		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.
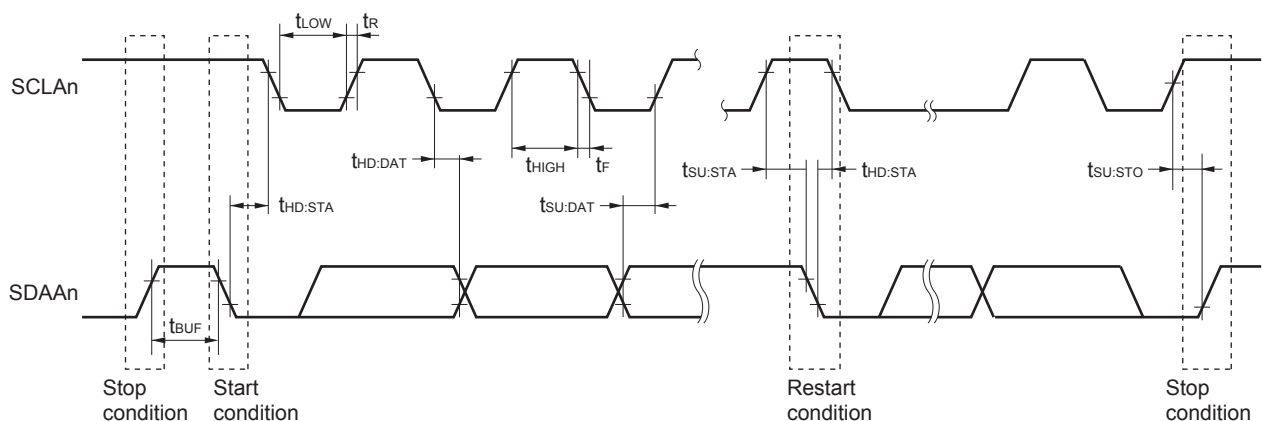
<R>

2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b = 320$ pF, $R_b = 1.1$ kΩ

(3) I²C fast mode plus

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode plus: f$_{CLK}$ ≥ 10 MHz	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	1000	—		—		kHz
Setup time of restart condition	t$_{SU:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μS
Hold time[Note 1]	t$_{HD:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μS
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μS
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μS
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		50		—		—		μS
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	0.45	—		—		μS
Setup time of stop condition	t$_{SU:STO}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.26		—		—		μS
Bus-free time	t$_{BUF}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0.5		—		—		μS

Notes **1.** The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

      Fast mode plus: C$_b$ = 120 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing

Remark n = 0, 1

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV$_{DD0}$		EV$_{DD0}$	V
	V$_{IH2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	2.2		EV$_{DD0}$	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	2.0		EV$_{DD0}$	V
			TTL input buffer 2.4 V ≤ EV$_{DD0}$ < 3.3 V	1.5		EV$_{DD0}$	V
	V$_{IH3}$	P20 to P27, P150 to P156		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P63		0.7EV$_{DD0}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV$_{DD0}$	V
	V$_{IL2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ EV$_{DD0}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P27, P150 to P156		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60 to P63		0		0.3EV$_{DD0}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{RESET}$		0		0.2V$_{DD}$	V

Caution The maximum value of V$_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV$_{DD0}$, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.6 **Note 2**	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 **Note 4**	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 6**	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

 * This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.4 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

 * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 **Note 2**		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 340 **Note 2**		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 760 **Note 2**		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 760 **Note 2**		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 570 **Note 2**		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

       2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

3.8 Flash Memory Programming Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	2.4 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1,2,3	C_{erwr}	Retained for 20 years T_A = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1,2,3		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C Note 4	100,000			
		Retained for 20 years T_A = 85°C Note 4	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.The retaining years are until next rewrite after the rewrite.

    2. When using flash memory programmer and Renesas Electronics self programming library.

    3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

    4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps