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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

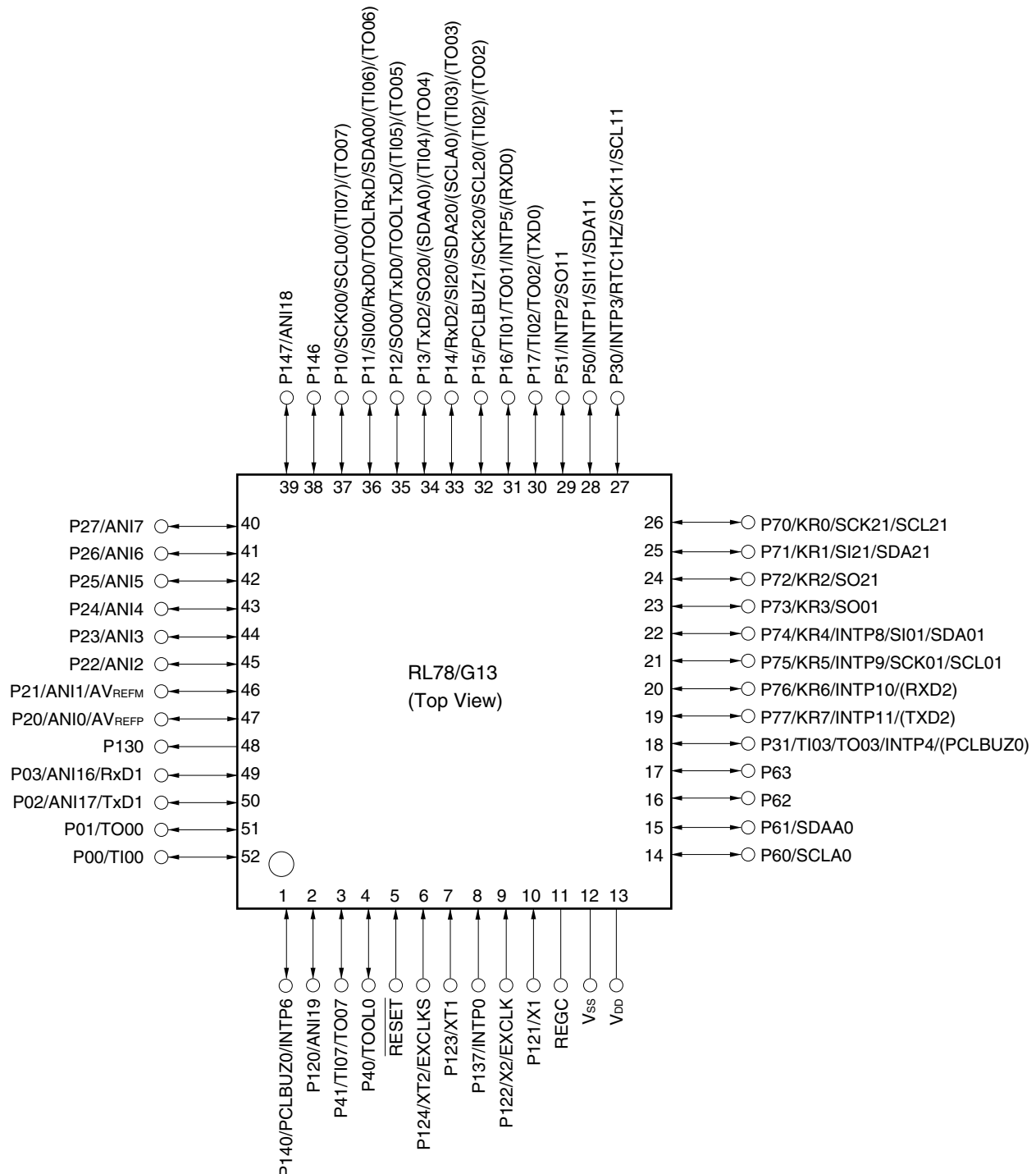
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lgdfb-x0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lgdfb-x0</a>

## 1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)

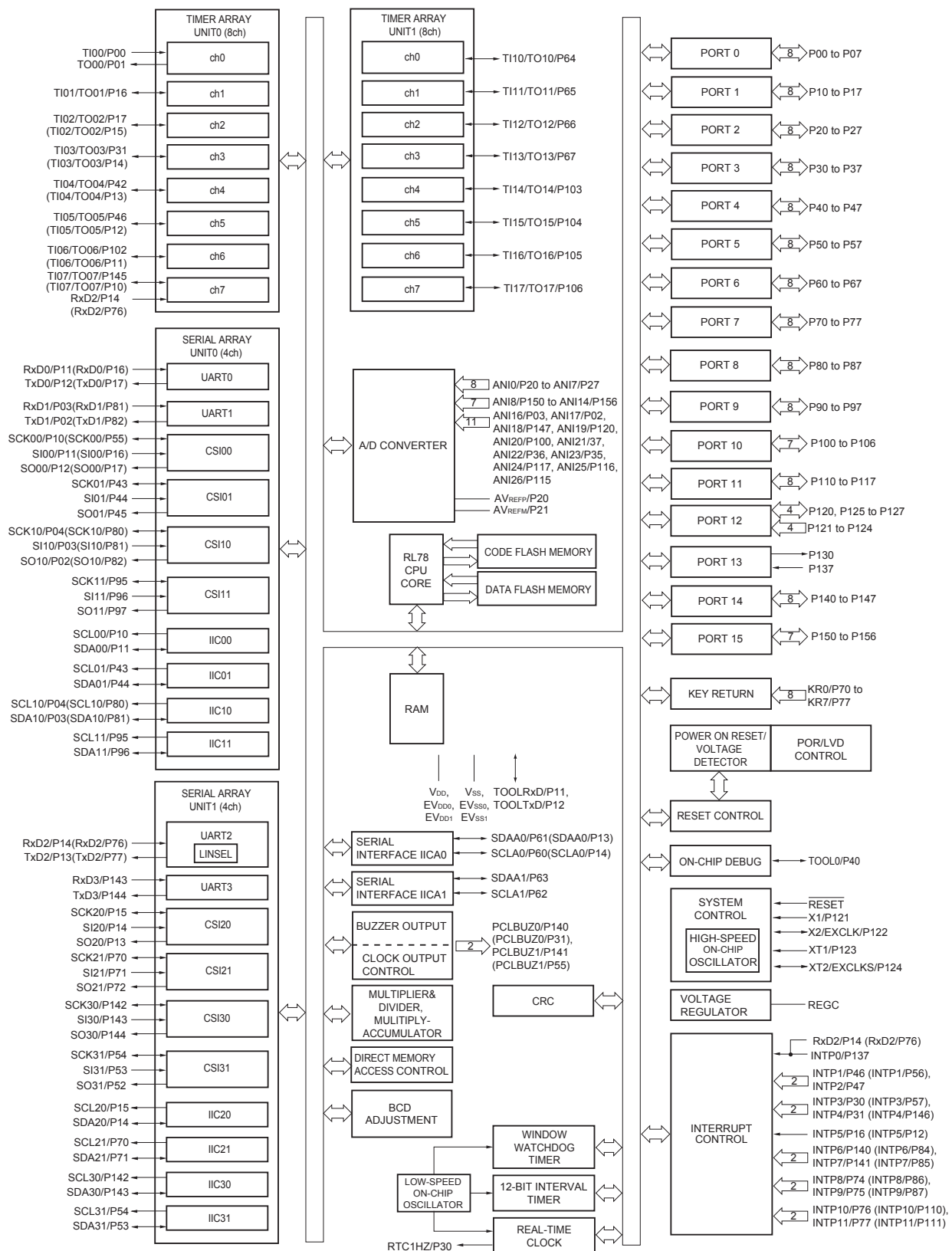


**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.14 128-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		<ul style="list-style-type: none"><li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f<sub>MAIN</sub> = 20 MHz operation)</li><li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f<sub>SUB</sub> = 32.768 kHz operation)</li></ul>					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products]					
		<ul style="list-style-type: none"><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li></ul>					
	I <sup>2</sup> C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		<ul style="list-style-type: none"><li>16 bits × 16 bits = 32 bits (Unsigned or signed)</li><li>32 bits ÷ 32 bits = 32 bits (Unsigned)</li><li>16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)</li></ul>					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		<ul style="list-style-type: none"><li>Reset by RESET pin</li><li>Internal reset by watchdog timer</li><li>Internal reset by power-on-reset</li><li>Internal reset by voltage detector</li><li>Internal reset by illegal instruction execution <sup>Note</sup></li><li>Internal reset by RAM parity error</li><li>Internal reset by illegal-memory access</li></ul>					
Power-on-reset circuit		<ul style="list-style-type: none"><li>Power-on-reset: 1.51 V (TYP.)</li><li>Power-down-reset: 1.50 V (TYP.)</li></ul>					
Voltage detector		<ul style="list-style-type: none"><li>Rising edge : 1.67 V to 4.06 V (14 stages)</li><li>Falling edge : 1.63 V to 3.98 V (14 stages)</li></ul>					
On-chip debug function		Provided					
Power supply voltage		V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)					
Operating ambient temperature		T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications ) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)					

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

&lt;R&gt;

**Note** The following conditions are required for low voltage interface when  $E_{VDD0} < V_{DD}$

$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$  : MIN. 125 ns

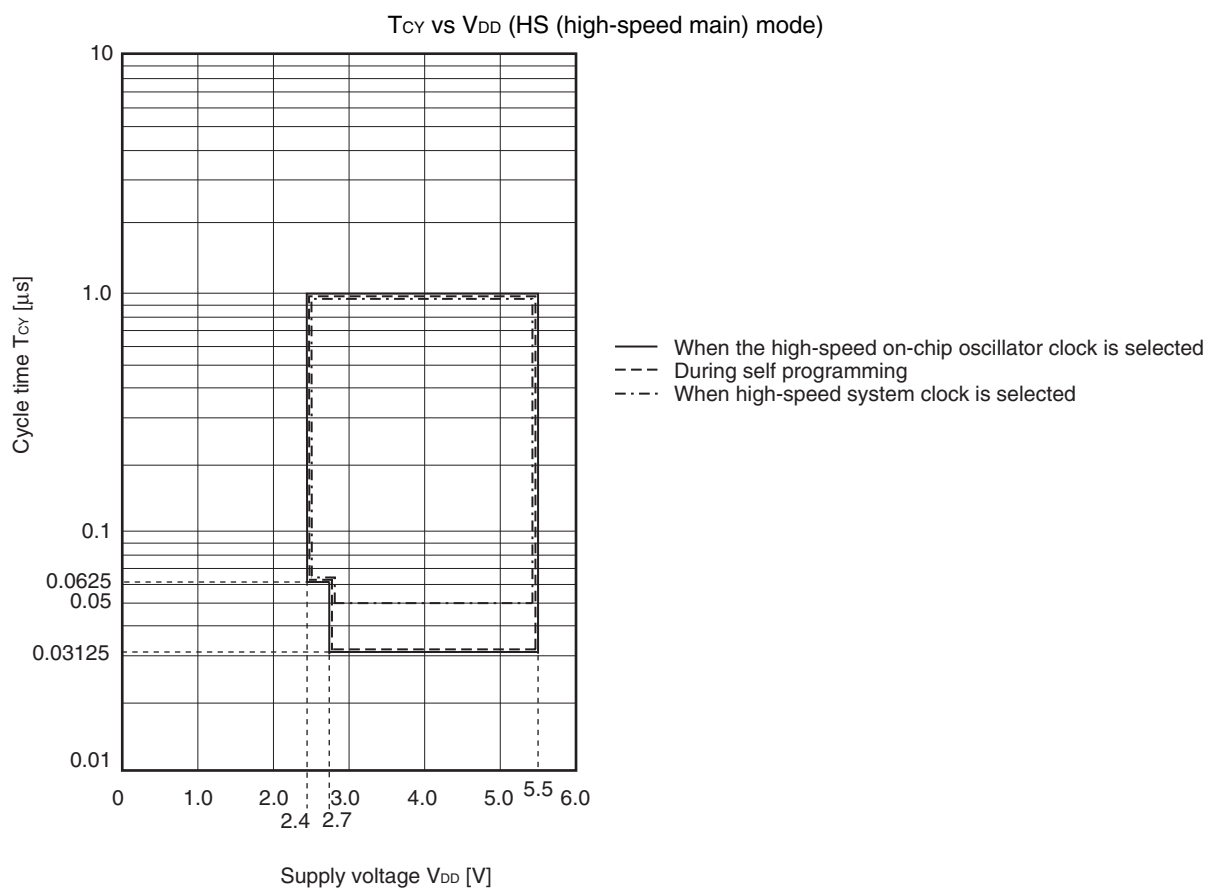
$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$  : MIN. 250 ns

**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number ( $m = 0, 1$ ), n: Channel number ( $n = 0$  to  $7$ ))

### Minimum Instruction Execution Time during Main System Clock Operation



## (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

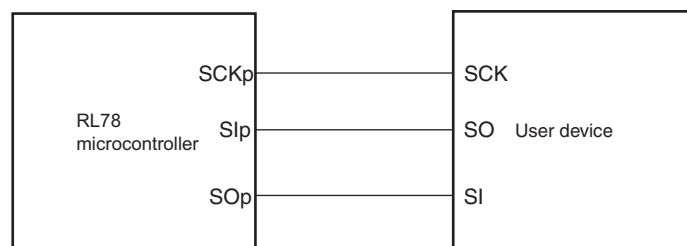
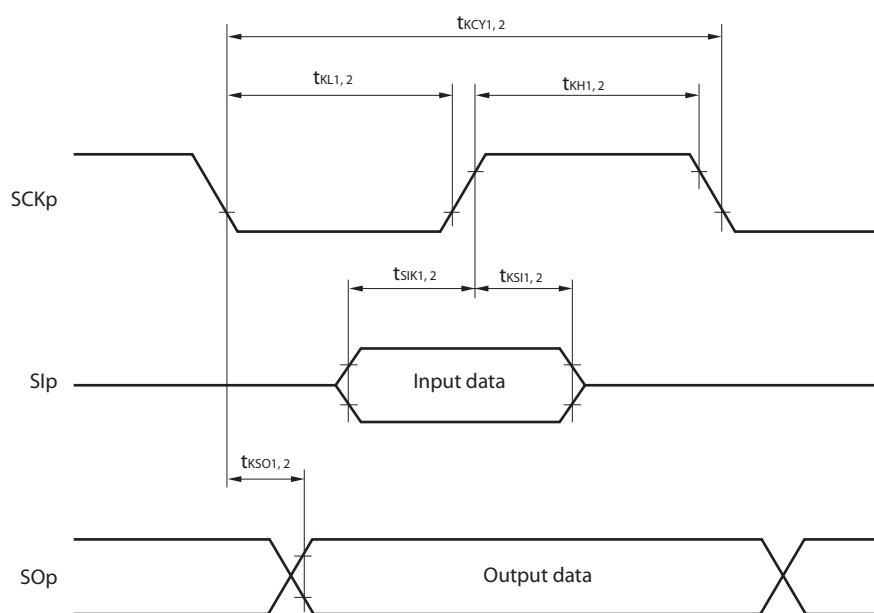
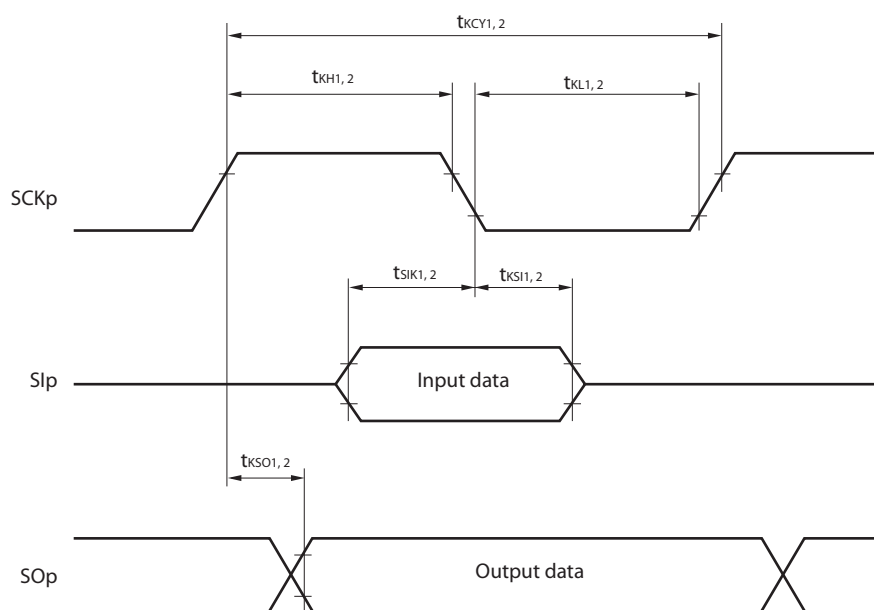
(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK2</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +2 0		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +3 0		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +4 0		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI2</sub>	1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +3 1		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> + 250		1/f <sub>MCK</sub> + 250		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO2</sub>	C = 30 pF <sup>Note 4</sup>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 44		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 75		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110		2/f <sub>MCK</sub> + 110	ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220	ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		2/f <sub>MCK</sub> + 220		2/f <sub>MCK</sub> + 220	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

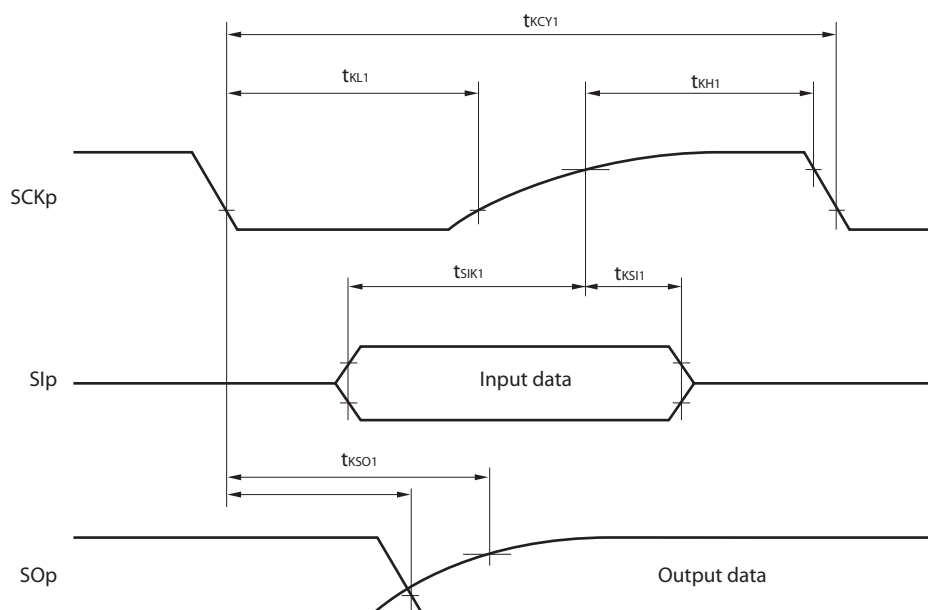
**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

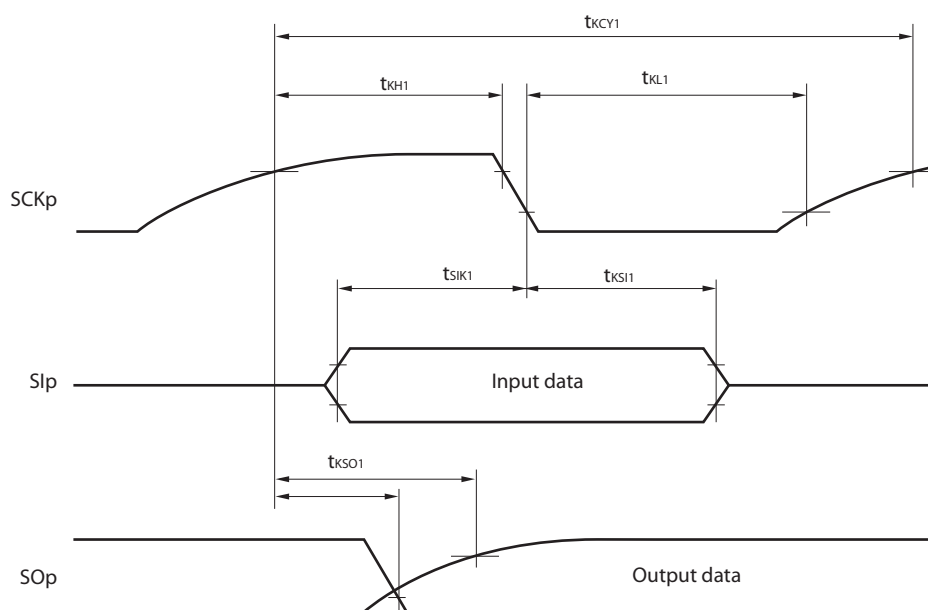
**CSI mode connection diagram (during communication at same potential)**
**CSI mode serial transfer timing (during communication at same potential)**  
 (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

**CSI mode serial transfer timing (during communication at same potential)**  
 (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)


- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
  2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



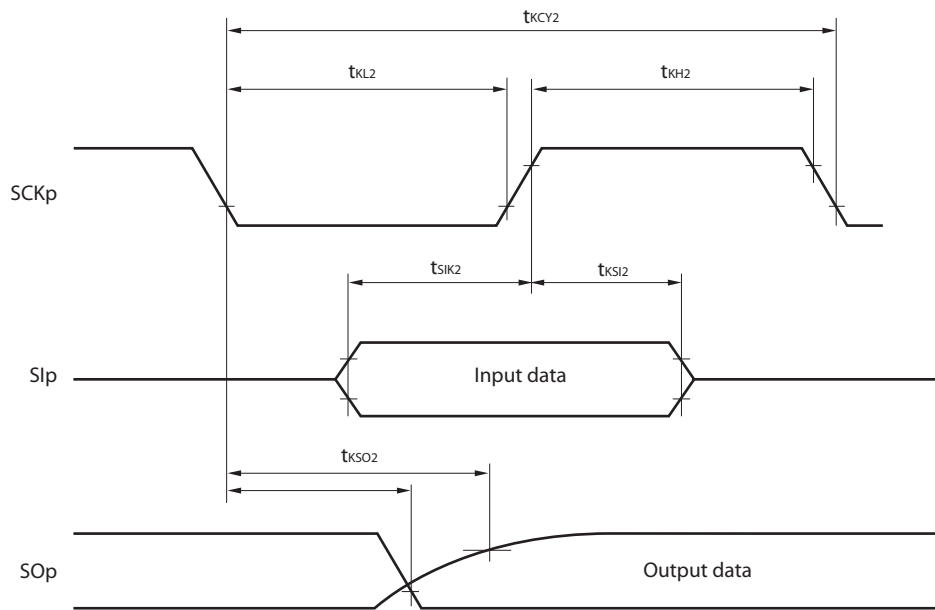
**CSI mode serial transfer timing (master mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



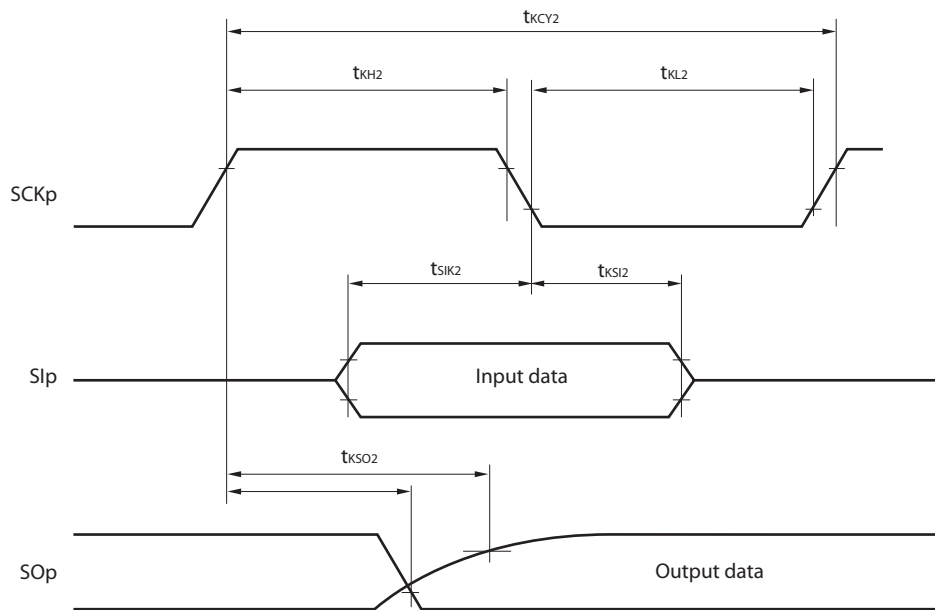
- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t <sub>SU:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
Data hold time (transmission)	t <sub>HD:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	ns

**Notes** 1. The value must also be equal to or less than f<sub>MCK</sub>/4.2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.3. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(3) When reference voltage (+) = V<sub>DD</sub> (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V<sub>SS</sub> (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V, Reference voltage (+) = V<sub>DD</sub>, Reference voltage (-) = V<sub>SS</sub>)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>		1.2	±10.5	LSB
Conversion time	t <sub>CONV</sub>	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	17		39	μs
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	57		95	μs
Conversion time	t <sub>CONV</sub>	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V <sub>DD</sub> ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V	17		39	μs
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±0.85	%FSR
Full-scale error <sup>Notes 1, 2</sup>	E <sub>FS</sub>	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±0.85	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±6.5	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V <small>Note 3</small>			±2.5	LSB
Analog input voltage	V <sub>AIN</sub>	ANI0 to ANI14	0			V <sub>DD</sub>	V
		ANI16 to ANI26	0			EV <sub>DD0</sub>	V
		Internal reference voltage (2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V, HS (high-speed main) mode)	V <sub>BGR</sub> <sup>Note 4</sup>				V
		Temperature sensor output voltage (2.4 V ≤ V <sub>DD</sub> ≤ 5.5 V, HS (high-speed main) mode)	V <sub>TMPS25</sub> <sup>Note 4</sup>				V

**Notes** 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

## 2.8 Flash Memory Programming Characteristics

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f <sub>CLK</sub>	1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	C <sub>erwr</sub>	Retained for 20 years T <sub>A</sub> = 85°C	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years T <sub>A</sub> = 25°C		1,000,000		
		Retained for 5 years T <sub>A</sub> = 85°C	100,000			
		Retained for 20 years T <sub>A</sub> = 85°C	10,000			

**Notes** 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

### 3.2 Oscillator Characteristics

#### 3.2.1 X1, XT1 oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
XT1 clock oscillation frequency ( $f_x$ ) <sup>Note</sup>	Crystal resonator		32	32.768	35	kHz

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

**Remark** When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

#### 3.2.2 On-chip oscillator characteristics

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency <sup>Notes 1, 2</sup>	$f_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		$-20$ to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		+1.0	%
		$-40$ to $-20^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
		$+85$ to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	$f_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (4/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	$\text{V}_{\text{OH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	$\text{V}_{\text{OH2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	$\text{V}_{\text{OL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	$\text{V}_{\text{OL2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	$\text{V}_{\text{OL3}}$	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(TA = -40 to +105°C,  $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = V_{SS0} = 0\text{ V}$ ) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 7	f <sub>IH</sub> = 32 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.54	2.90	mA	
					V <sub>DD</sub> = 3.0 V		0.54	2.90	mA	
				f <sub>IH</sub> = 24 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.44	2.30	mA	
					V <sub>DD</sub> = 3.0 V		0.44	2.30	mA	
				f <sub>IH</sub> = 16 MHz Note 4	V <sub>DD</sub> = 5.0 V		0.40	1.70	mA	
					V <sub>DD</sub> = 3.0 V		0.40	1.70	mA	
			HS (high-speed main) mode Note 7	f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 5.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f <sub>MX</sub> = 20 MHz Note 3, V <sub>DD</sub> = 3.0 V	Square wave input		0.28	1.90	mA	
					Resonator connection		0.45	2.00	mA	
				f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 5.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
				f <sub>MX</sub> = 10 MHz Note 3, V <sub>DD</sub> = 3.0 V	Square wave input		0.19	1.02	mA	
					Resonator connection		0.26	1.10	mA	
		Subsystem clock operation		f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = −40°C	Square wave input		0.25	0.57	μA	
					Resonator connection		0.44	0.76	μA	
			f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = +25°C	Square wave input		0.30	0.57	μA		
				Resonator connection		0.49	0.76	μA		
			f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = +50°C	Square wave input		0.37	1.17	μA		
				Resonator connection		0.56	1.36	μA		
			f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = +70°C	Square wave input		0.53	1.97	μA		
				Resonator connection		0.72	2.16	μA		
			f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = +85°C	Square wave input		0.82	3.37	μA		
				Resonator connection		1.01	3.56	μA		
		f <sub>SUB</sub> = 32.768 kHz Note 5 T <sub>A</sub> = +105°C	Square wave input		3.01	15.37	μA			
			Resonator connection		3.20	15.56	μA			
	I <sub>DD3</sub> Note 6	STOP mode Note 8	T <sub>A</sub> = −40°C					0.18	0.50	μA
			T <sub>A</sub> = +25°C					0.23	0.50	μA
			T <sub>A</sub> = +50°C					0.30	1.10	μA
			T <sub>A</sub> = +70°C					0.46	1.90	μA
			T <sub>A</sub> = +85°C					0.75	3.30	μA
			T <sub>A</sub> = +105°C					2.94	15.30	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

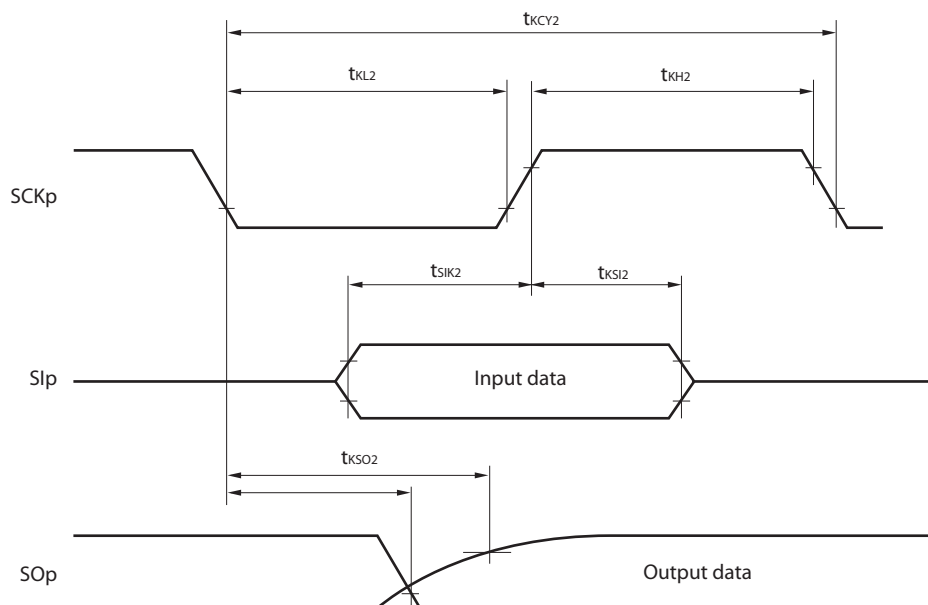
HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

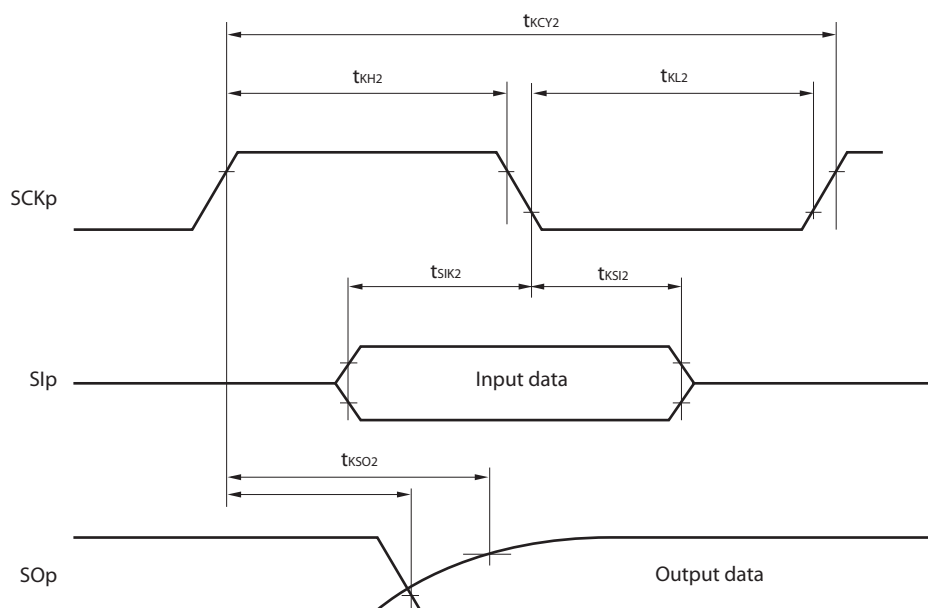
- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



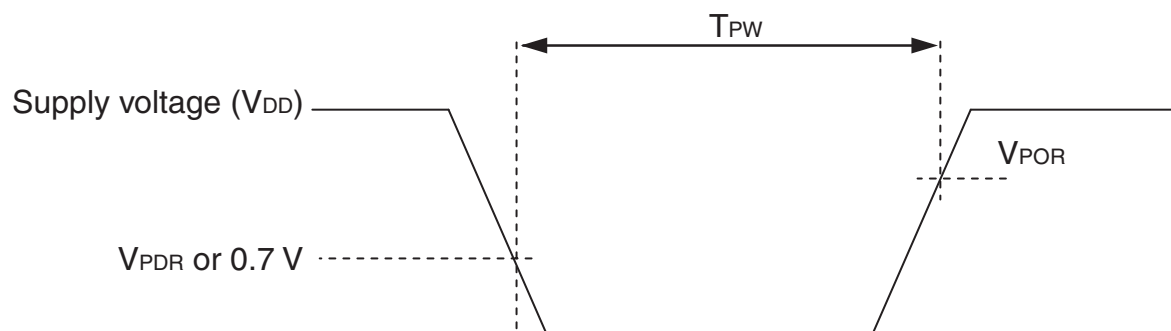
- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.

## 3.6.3 POR circuit characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	$T_{PW}$		300			$\mu\text{s}$

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.6.5 Power supply voltage rising slope characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	$S_{VDD}$				54	V/ms

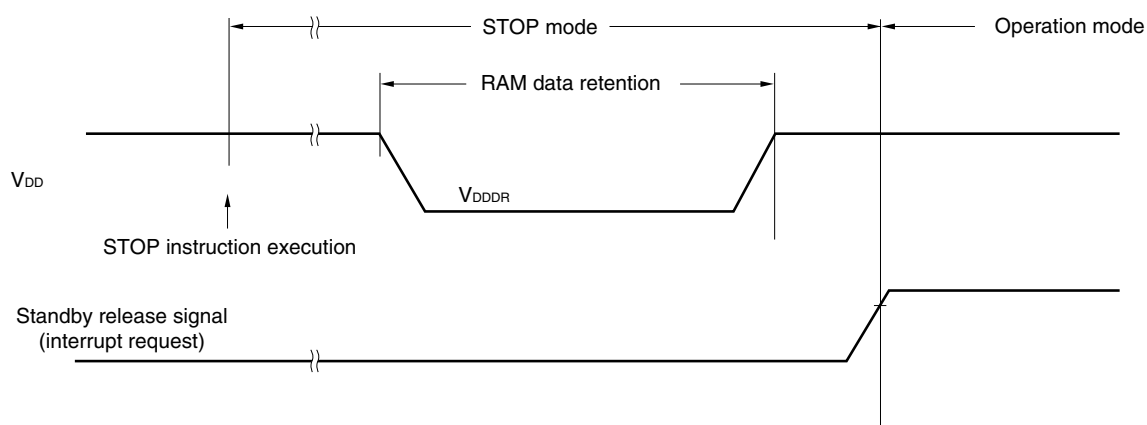
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until  $V_{DD}$  reaches the operating voltage range shown in 3.4 AC Characteristics.

## 3.7 RAM Data Retention Characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.44 <sup>Note</sup>		5.5	V

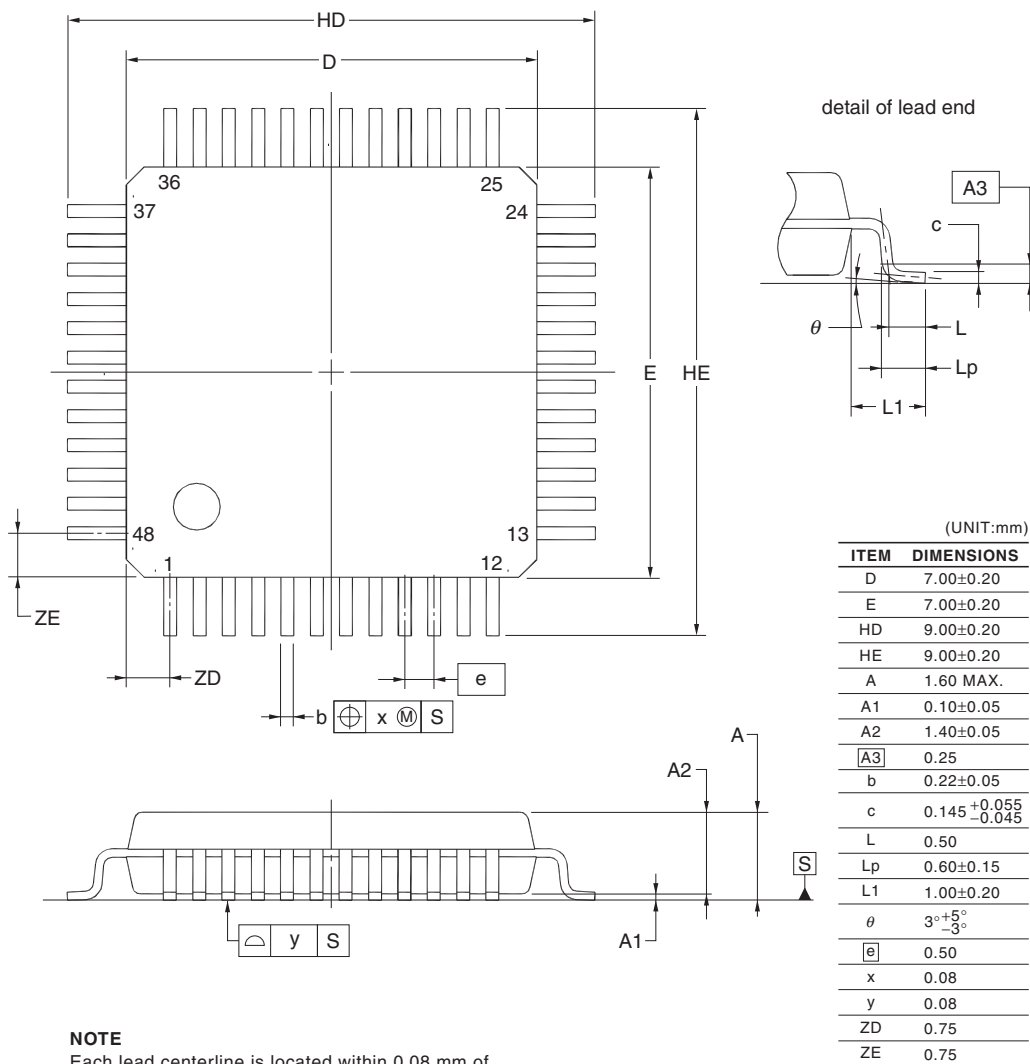
**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



## 4.9 48-pin Products

R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB,  
 R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB  
 R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB,  
 R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB  
 R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB,  
 R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB  
 R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB,  
 R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB  
 R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB,  
 R5F100GHGFB, R5F100GJGFB

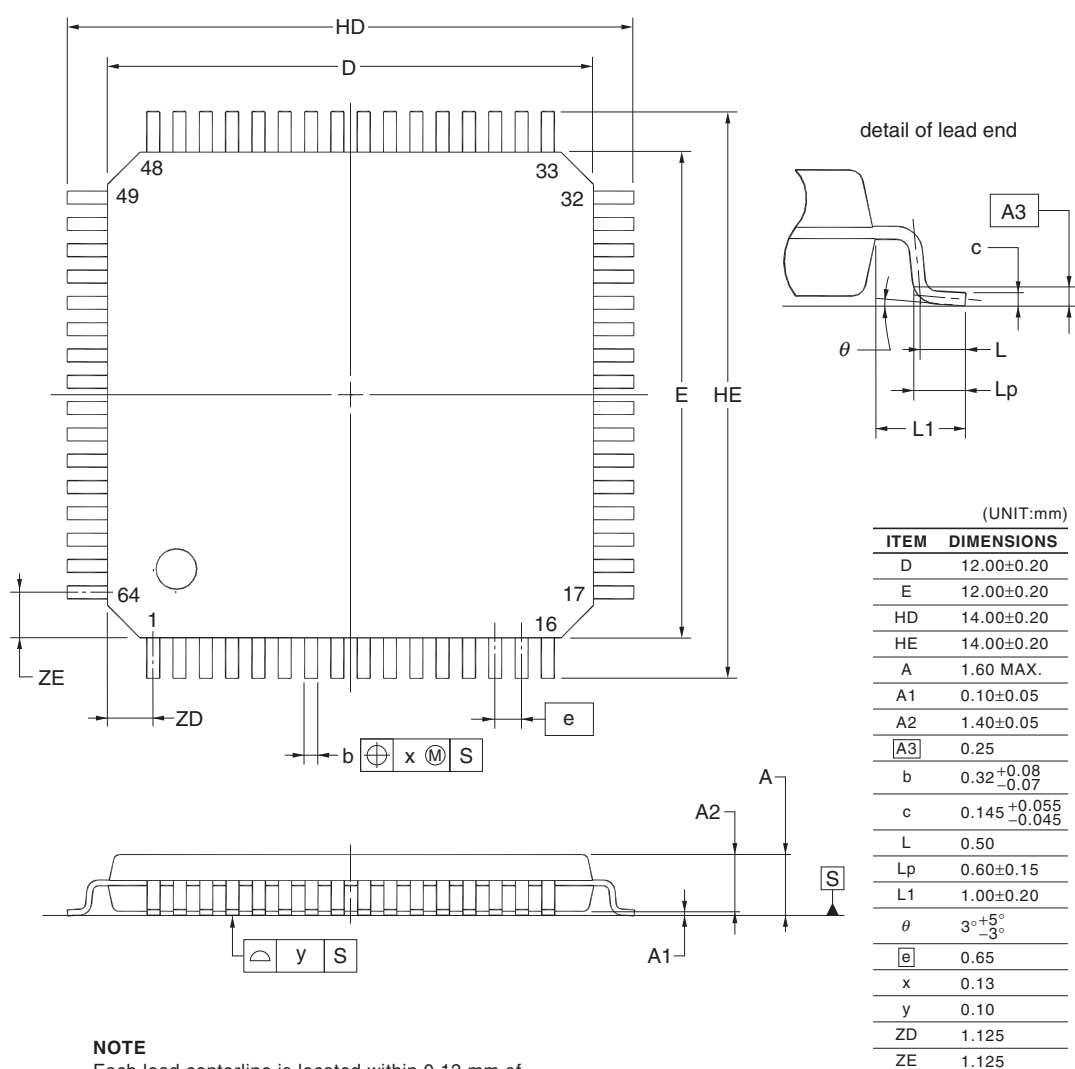
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



## 4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAF, A,  
R5F100LKAFA, R5F100LLAFA  
R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAF, A,  
R5F101LKAFA, R5F101LLAFA  
R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LH DFA, R5F100LJ DFA,  
R5F100LK DFA, R5F100LL DFA  
R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LH DFA, R5F101LJ DFA,  
R5F101LK DFA, R5F101LL DFA  
R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,  
R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

**NOTE**

Each lead centerline is located within 0.13 mm of its true position at maximum material condition.