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What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

| Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lggfa-v0

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJAFA#V0, R5F100LKAFA#V0, R5F100LLAFA#V0
				R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0,
			D	R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJAFA#X0, R5F100LKAFA#X0, R5F100LLAFA#X0
				R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDFA#V0, R5F100LHDFA#V0, R5F100LJDFA#V0, R5F100LKDFA#V0, R5F100LLDFA#V0
			G	R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDFA#X0, R5F100LHDFA#X0, R5F100LJDFA#X0, R5F100LKDFA#X0, R5F100LLDFA#X0
				R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0
				R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0
				R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0
				R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJAFA#V0, R5F101LKAFA#V0, R5F101LLAFA#V0
				R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0,
			D	R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJAFA#X0, R5F101LKAFA#X0, R5F101LLAFA#X0
				R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDFA#V0, R5F101LHDFA#V0, R5F101LJDFA#V0, R5F101LKDFA#V0, R5F101LLDFA#V0
				R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDFA#X0, R5F101LHDFA#X0, R5F101LJDFA#X0, R5F101LKDFA#X0, R5F101LLDFA#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)
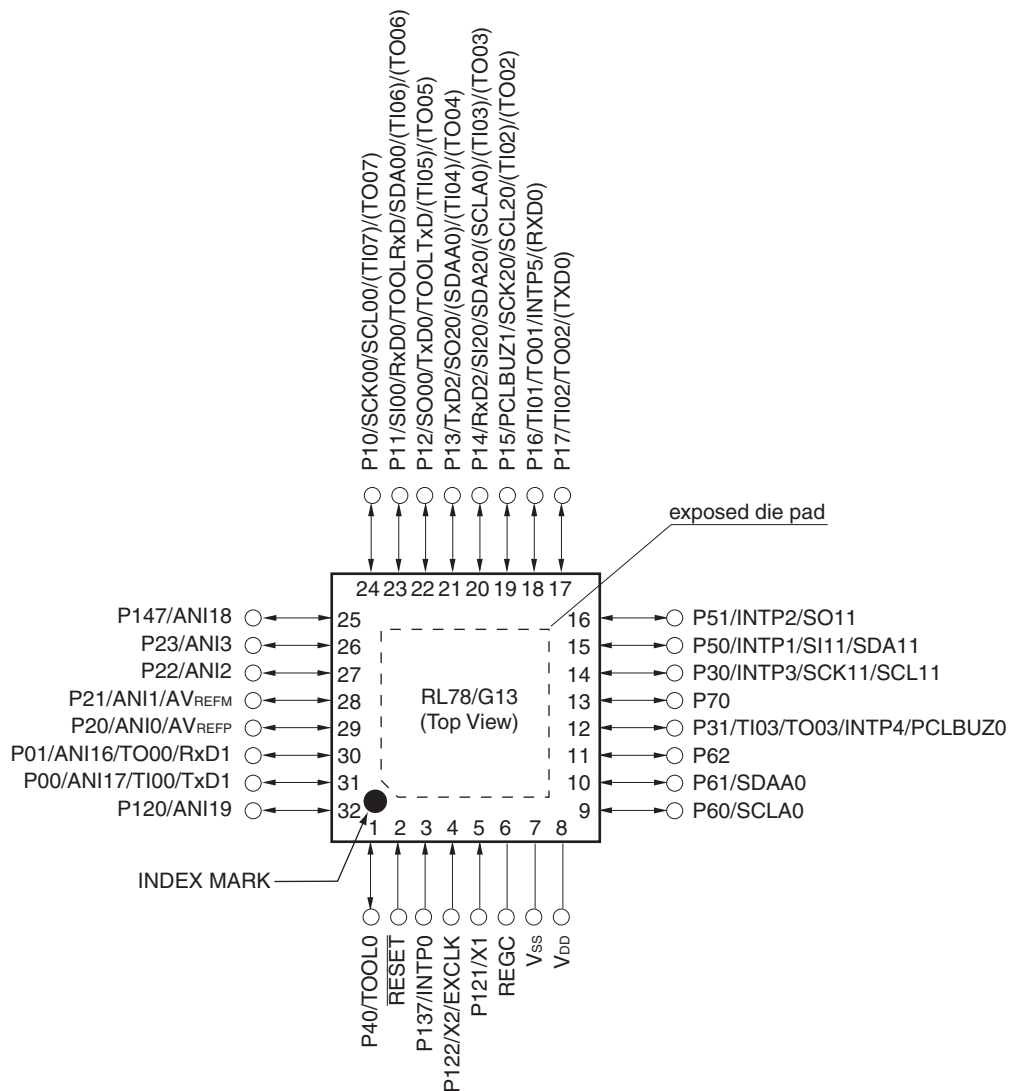
Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
   3. It is recommended to connect an exposed die pad to Vss.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Top pins (left to right):
P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Top pin numbers: 36 35 34 33 32 31 30 29 28 27 26 25

Left side:
- 37 P120/ANI19
- 38 P41/TI07/TO07
- 39 P40/TOOL0
- 40 $\overline{\text{RESET}}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 V$_{SS}$
- 48 V$_{DD}$

Center: exposed die pad, RL78/G13 (Top View)

INDEX MARK

Bottom pin numbers: 1 2 3 4 5 6 7 8 9 10 11 12

Right side:
- 24 P147/ANI18
- 23 P146
- 22 P10/SCK00/SCL00/(TI07)/(TO07)
- 21 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 P16/TI01/TO01/INTP5/(RXD0)
- 15 P17/TI02/TO02/(TXD0)
- 14 P51/INTP2/SO11
- 13 P50/INTP1/SI11/SDA11

Bottom pins (left to right):
P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11
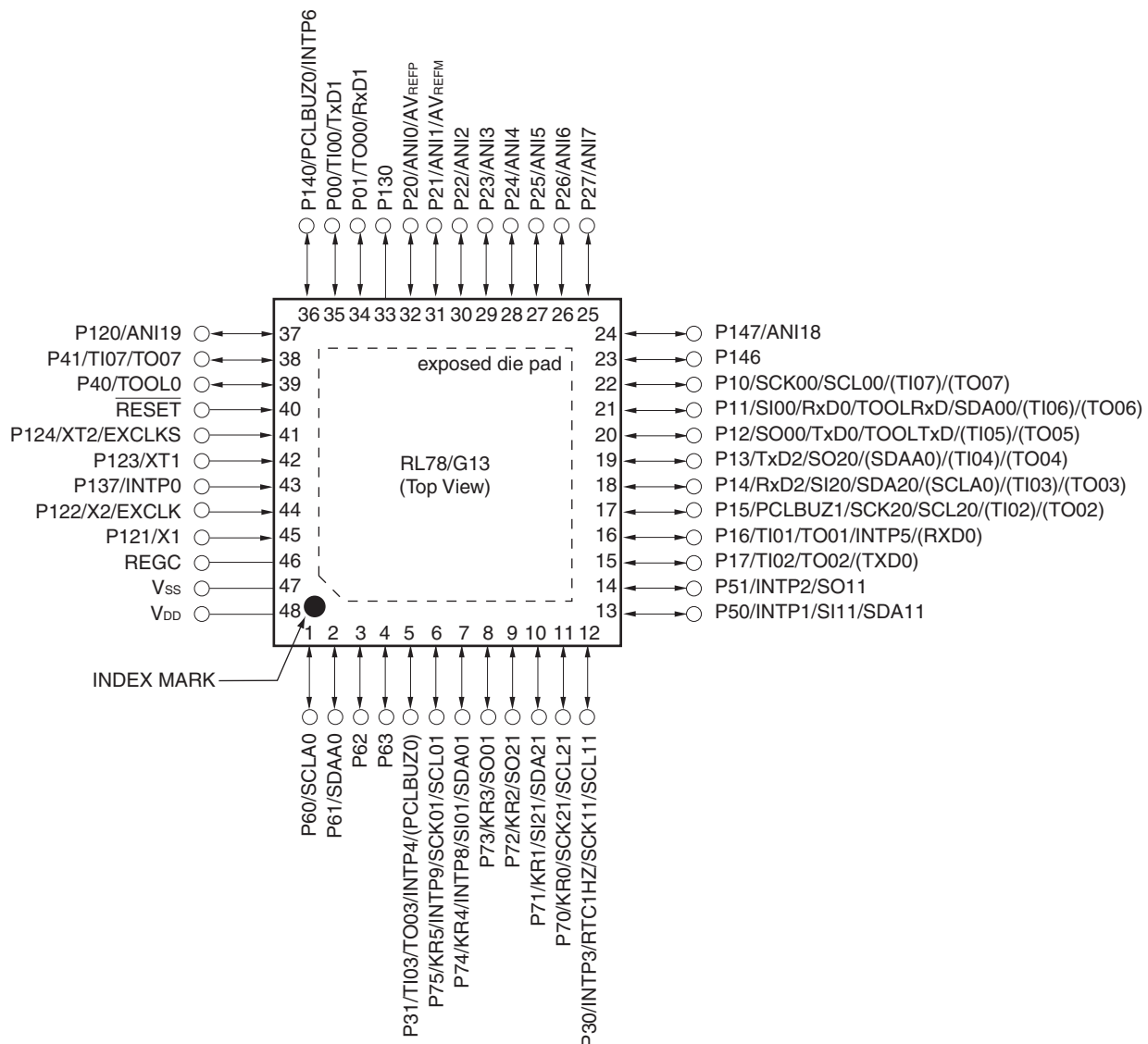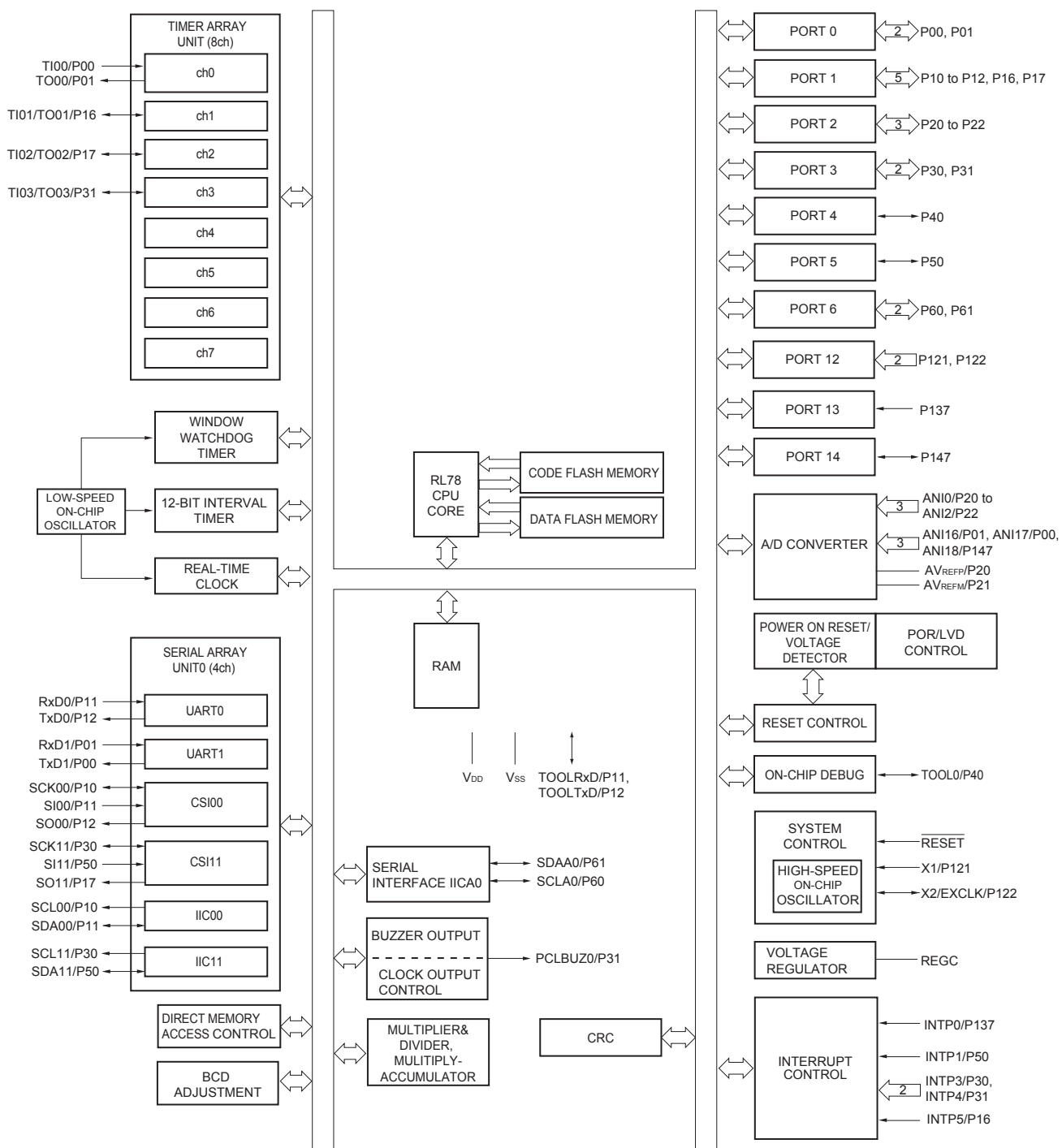
Caution   **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**
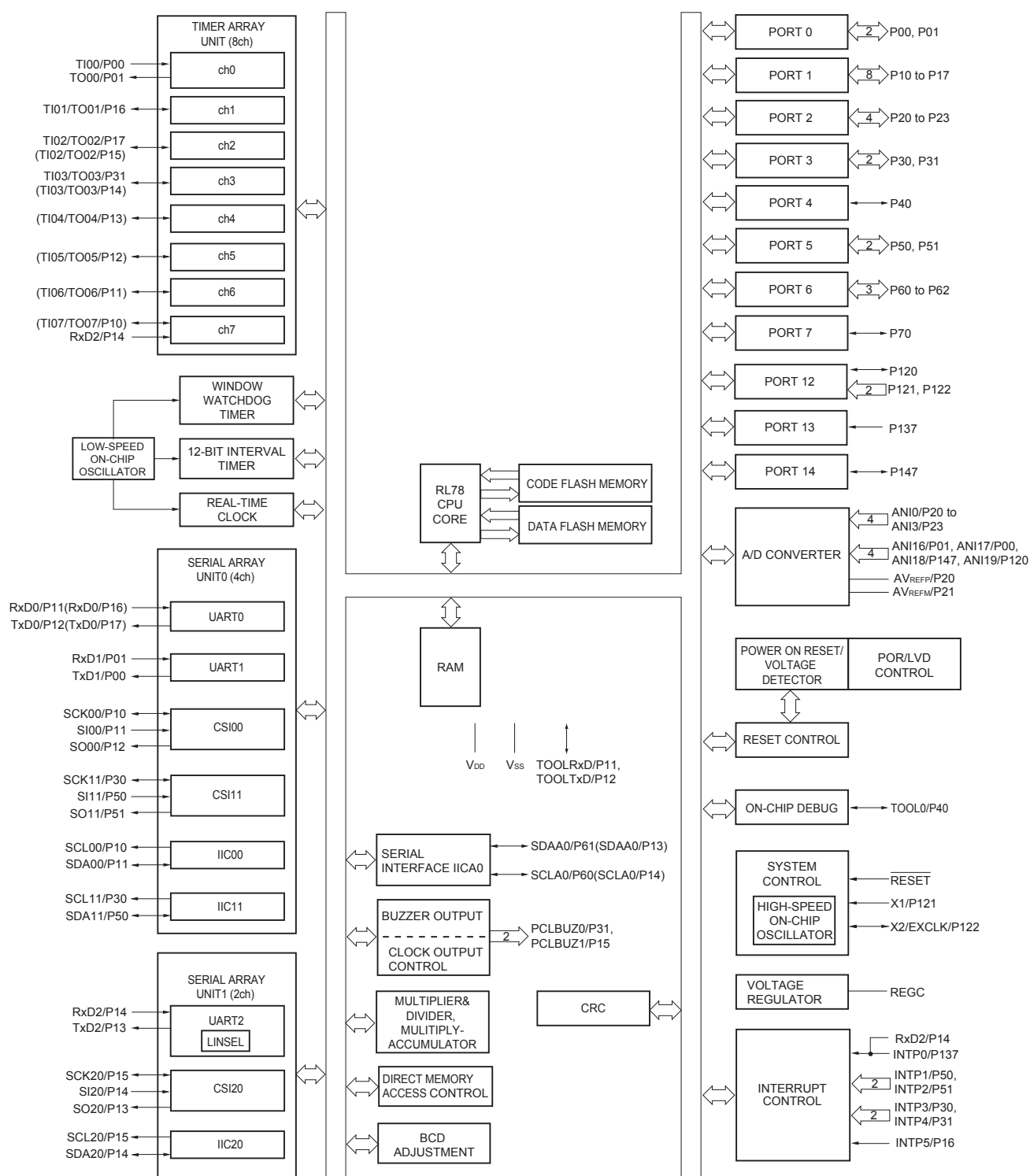
Remarks 1.   For pin identification, see **1.4 Pin Identification**.

      2.   Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

      3.   It is recommended to connect an exposed die pad to V$_{ss}$.

1.5.2 24-pin products

1.5.5 32-pin products

TIMER ARRAY UNIT (8ch)
- TI00/P00, TO00/P01 — ch0
- TI01/TO01/P16 — ch1
- TI02/TO02/P17 (TI02/TO02/P15) — ch2
- TI03/TO03/P31 (TI03/TO03/P14) — ch3
- (TI04/TO04/P13) — ch4
- (TI05/TO05/P12) — ch5
- (TI06/TO06/P11) — ch6
- (TI07/TO07/P10) RxD2/P14 — ch7

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12-BIT INTERVAL TIMER

REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)
- RxD0/P11(RxD0/P16), TxD0/P12(TxD0/P17) — UART0
- RxD1/P01, TxD1/P00 — UART1
- SCK00/P10, SI00/P11, SO00/P12 — CSI00
- SCK11/P30, SI11/P50, SO11/P51 — CSI11
- SCL00/P10, SDA00/P11 — IIC00
- SCL11/P30, SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)
- RxD2/P14, TxD2/P13 — UART2 (LINSEL)
- SCK20/P15, SI20/P14, SO20/P13 — CSI20
- SCL20/P15, SDA20/P14 — IIC20

RL78 CPU CORE — CODE FLASH MEMORY, DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL — 2 — PCLBUZ0/P31, PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 2 — P00, P01
PORT 1 — 8 — P10 to P17
PORT 2 — 4 — P20 to P23
PORT 3 — 2 — P30, P31
PORT 4 — P40
PORT 5 — 2 — P50, P51
PORT 6 — 3 — P60 to P62
PORT 7 — P70
PORT 12 — P120, 2 — P121, P122
PORT 13 — P137
PORT 14 — P147

A/D CONVERTER
- 4 — ANI0/P20 to ANI3/P23
- 4 — ANI16/P01, ANI17/P00, ANI18/P147, ANI19/P120
- AV$_{REFP}$/P20
- AV$_{REFM}$/P21

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL — RESET, X1/P121, X2/EXCLK/P122 — HIGH-SPEED ON-CHIP OSCILLATOR

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- RxD2/P14
- INTP0/P137
- 2 — INTP1/P50, INTP2/P51
- 2 — INTP3/P30, INTP4/P31
- INTP5/P16

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

Notes **1.** Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks **1.** f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(4) Peripheral Functions (Common to all products)

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$ [Note 1]				0.20		μA
RTC operating current	I$_{RTC}$ [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I$_{IT}$ [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 5]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ [Notes 1, 6]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$ [Note 1]				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		μA
LVD operating current	I$_{LVI}$ [Notes 1, 7]				0.08		μA
Self-programming operating current	I$_{FSP}$ [Notes 1, 9]				2.50	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 8]				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed [Note 10]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added. I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

2.4 AC Characteristics

(T$_A$ = –40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.03125		1	μs
				2.4 V $\leq$ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.25		1	μs
		Subsystem clock (f$_{SUB}$) operation		1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.03125		1	μs
				2.4 V $\leq$ V$_{DD}$ < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	0.25		1	μs
External system clock frequency	f$_{EX}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			1.0		20.0	MHz
		2.4 V $\leq$ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V $\leq$ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
		1.6 V $\leq$ V$_{DD}$ < 1.8 V			1.0		4.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V			24			ns
		2.4 V $\leq$ V$_{DD}$ < 2.7 V			30			ns
		1.8 V $\leq$ V$_{DD}$ < 2.4 V			60			ns
		1.6 V $\leq$ V$_{DD}$ < 1.8 V			120			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns[Note]
TO00 to TO07, TO10 to TO17 output frequency	f$_{TO}$	HS (high-speed main) mode		4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			16	MHz
				2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode		4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			16	MHz
				2.7 V $\leq$ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V $\leq$ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V			4	MHz
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0		1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	1			μs
		INTP1 to INTP11		1.6 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	1			μs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7		1.8 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V	250			ns
				1.6 V $\leq$ EV$_{DD0}$ < 1.8 V	1			μs
RESET low-level width	t$_{RSL}$				10			μs

(**Note** and **Remark** are listed on the next page.)

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 12		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 18		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 38		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		220		220		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI1}$	1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO1}$	1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V C = 30 pF[Note 4]			25		25		25	ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V C = 30 pF[Note 4]			—		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution   Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 **Note 1**		300 **Note 1**		300 **Note 1**	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 **Note 1**		300 **Note 1**		300 **Note 1**	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		400 **Note 1**		300 **Note 1**		300 **Note 1**	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		400 **Note 1**		300 **Note 1**		300 **ote 1**	kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		300 **Note 1**		300 **Note 1**		300 **Note 1**	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V **Note 2**, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	610		610		610		ns

(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (–) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]		1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±0.60	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution EV$_{DD0}$ = AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 5]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI26		0		AV$_{REFP}$ and EV$_{DD0}$	V

Notes 1. Excludes quantization error (±1/2 LSB).
　　　2. This value is indicated as a ratio (%FSR) to the full-scale value.
　　　3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
　　　　　Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　　　Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　　　Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　4. When AV$_{REFP}$ < EV$_{DD0}$ ≤ V$_{DD}$, the MAX. values are as follows.
　　　　　Overall error: Add ±4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　　　Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　　　Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
　　　**5.** When the conversion time is set to 57 μs (min.) and 95 μs (max.).

3.4 AC Characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
		Subsystem clock (f$_{SUB}$) operation		2.4 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	μs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns[Note]
TO00 to TO07, TO10 to TO17 output frequency	f$_{TO}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V				16	MHz
			2.7 V ≤ EV$_{DD0}$ < 4.0 V				8	MHz
			2.4 V ≤ EV$_{DD0}$ < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1			μs
		INTP1 to INTP11	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		1			μs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		250			ns
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$				10			μs

Note The following conditions are required for low voltage interface when EV$_{DD0}$ < V$_{DD}$

2.4V ≤ EV$_{DD0}$ < 2.7 V : MIN. 125 ns

Remark f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
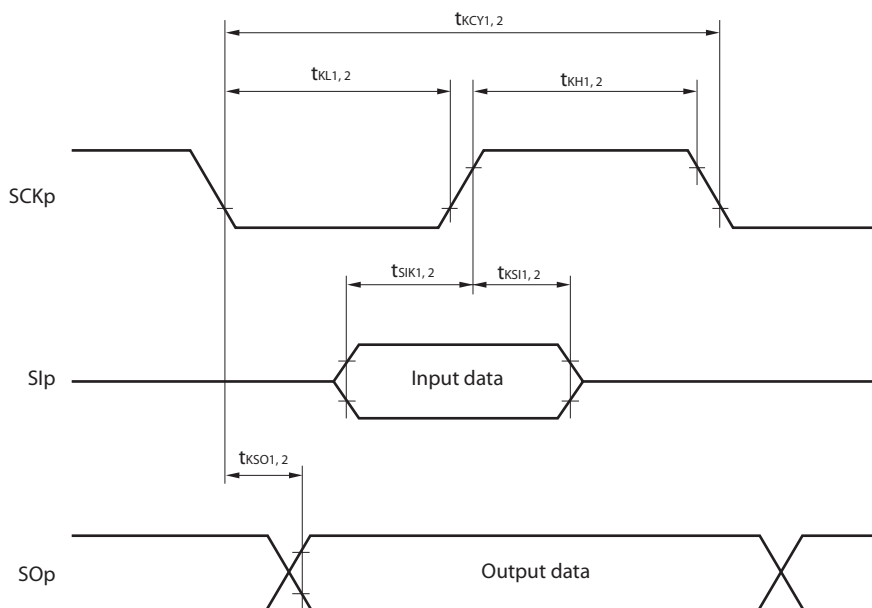
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
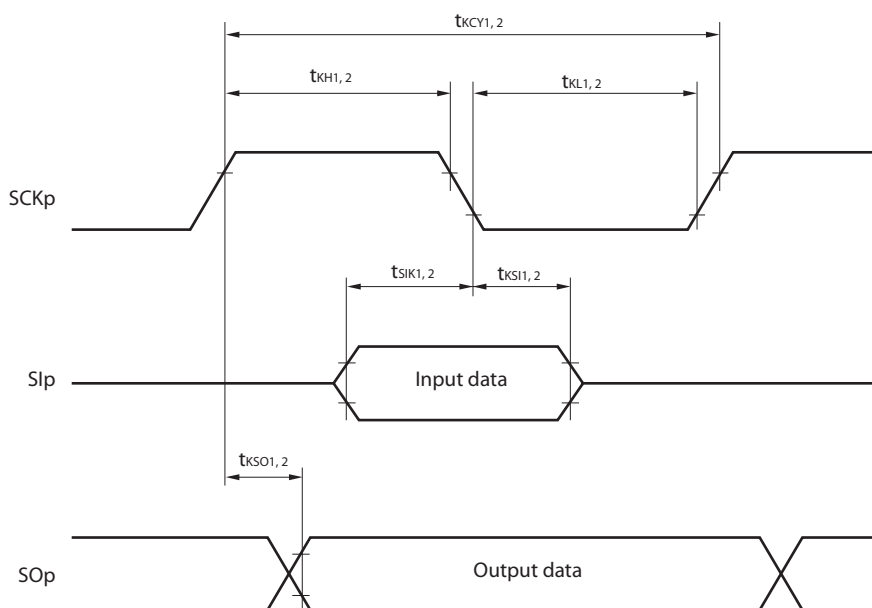
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = –40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Transmission	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		**Note 1**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.6 **Note 2**	Mbps
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		**Note 3**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 **Note 4**	Mbps
			2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		**Note 5**	bps
			Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 **Note 6**	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V and 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.4 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (−) = AV$_{REFM}$ [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).
  2. This value is indicated as a ratio (%FSR) to the full-scale value.
  3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.
  4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.
   Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.
   Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.
   Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

3.6.3 POR circuit characteristics

(T$_A$ = –40 to +105°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	V$_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time
required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is
entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock
operation status control register (CSC).
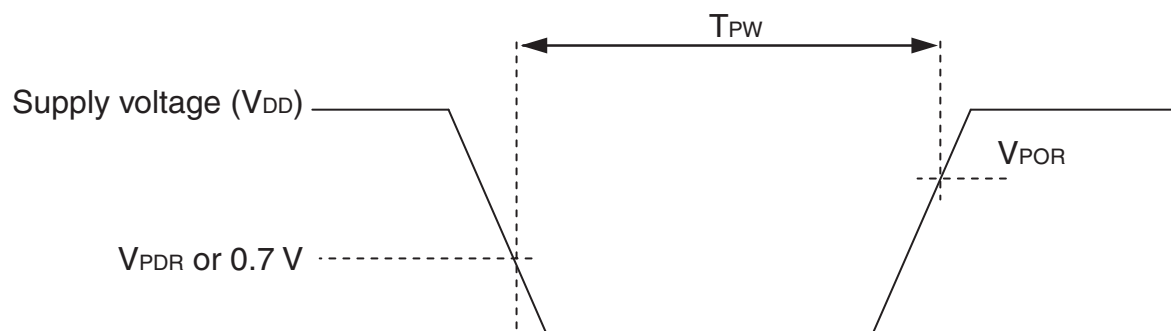
4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

Rev.	Date	Description		
		Page	**Summary**	
1.00	Feb 29, 2012	-	First Edition issued	
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.	
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.	
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.	
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.	
		59, 63, 67	Descriptions of Note 8 in a table corrected.	
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.	
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.	
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.	
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.	
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.	
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.	
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.	
3.00	Aug 02, 2013	1	Modification of 1.1 Features	
		3	Modification of 1.2 List of Part Numbers	
		4 to 15	Modification of Table 1-1. List of Ordering Part Numbers, note, and caution	
		16 to 32	Modification of package type in 1.3.1 to 1.3.14	
		33	Modification of description in 1.4 Pin Identification	
		48, 50, 52	Modification of caution, table, and note in 1.6 Outline of Functions	
		55	Modification of description in table of Absolute Maximum Ratings (T$_A$ = 25°C)	
		57	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics	
		57	Modification of table in 2.2.2 On-chip oscillator characteristics	
		58	Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics	
		59	Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics	
		63	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		64	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		65	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		66	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		68	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products	
		70	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products	
		72	Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products	
		74	Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products	
		75	Modification of (4) Peripheral Functions (Common to all products)	
		77	Modification of table in 2.4 AC Characteristics	
		78, 79	Addition of Minimum Instruction Execution Time during Main System Clock Operation	
		80	Modification of figures of AC Timing Test Points and External System Clock Timing	

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{ACK}$ corrected to ACK
			$\overline{ACK}$ corrected to ACK