Renesas Electronics America Inc - R5F100LHAFB#30 Datasheet

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lhafb-30

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application[Note]	Ordering Part Number
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0
			G	R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0
			D	R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0
			G	R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	A	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0
			D	R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(5/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0 R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0
			D	R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0 R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0
			G	R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0 R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0
		Not mounted	A	R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0 R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0
			D	R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0 R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

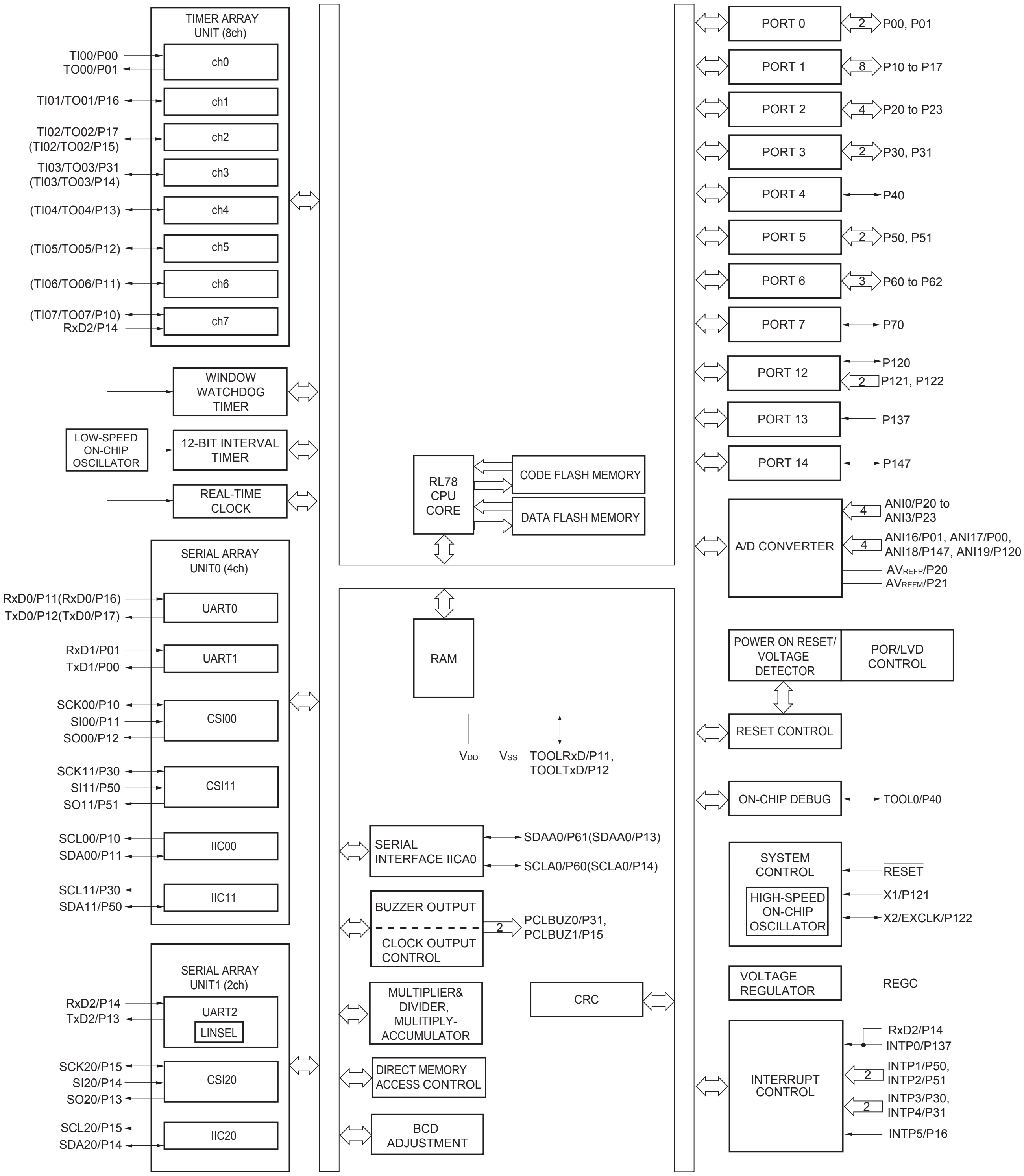
Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.4 Pin Identification

ANI0 to ANI14, ANI16 to ANI26:	Analog input
AV$_{\text{REFM}}$:	A/D converter reference potential (– side) input
AV$_{\text{REFP}}$:	A/D converter reference potential (+ side) input
EV$_{\text{DD0}}$, EV$_{\text{DD1}}$:	Power supply for port
EV$_{\text{SS0}}$, EV$_{\text{SS1}}$:	Ground for port
EXCLK:	External clock input (Main system clock)
EXCLKS:	External clock input (Subsystem clock)
INTP0 to INTP11:	Interrupt request from peripheral
KR0 to KR7:	Key return
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P97:	Port 9
P100 to P106:	Port 10
P110 to P117:	Port 11
P120 to P127:	Port 12
P130, P137:	Port 13
P140 to P147:	Port 14
P150 to P156:	Port 15
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output

REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time clock correction clock (1 Hz) output
RxD0 to RxD3:	Receive data
SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, SCLA0, SCLA1:	Serial clock input/output
SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11, SCL20,SCL21, SCL30, SCL31:	Serial clock output
SDAA0, SDAA1, SDA00, SDA01,SDA10, SDA11, SDA20,SDA21, SDA30, SDA31:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31:	Serial data output
TI00 to TI07, TI10 to TI17:	Timer input
TO00 to TO07, TO10 to TO17:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0 to TxD3:	Transmit data
V$_{\text{DD}}$:	Power supply
V$_{\text{SS}}$:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

1.5.5 32-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4[Note1]		2 to 4[Note1]		2 to 4[Note1]		2 to 12[Note1]		2 to 12[Note1]		2 to 12[Note1]	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)											
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)											
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.											
I/O port	Total	16		20		21		26		28		32	
	CMOS I/O	13 (N-ch O.D. I/O [V_{DD} withstand voltage]: 5)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		15 (N-ch O.D. I/O [V_{DD} withstand voltage]: 6)		21 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		22 (N-ch O.D. I/O [V_{DD} withstand voltage]: 9)		26 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)	
	CMOS input	3		3		3		3		3		3	
	CMOS output	–		–		1		–		–		–	
	N-ch O.D. I/O (withstand voltage: 6 V)	–		2		2		2		3		3	
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel[Note 2]											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2[Note 3])		4 channels (PWM outputs: 3[Note 3])				4 channels (PWM outputs: 3[Note 3]), 8 channels (PWM outputs: 7[Note 3])[Note 4]					
	RTC output	–											

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V_{DD} < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f_X)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ V_{DD} < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ V_{DD} ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ V_{DD} < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV_{DD0} ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V_{DD} ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T_A = −40 to +85°C, 2.7 V $\leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		1150		1150		ns
			2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 120		$t_{KCY1}/2$ – 120		$t_{KCY1}/2$ – 120		ns
SCKp low-level width	t_{KL1}	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ – 7		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 10		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		479		ns
		2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V $\leq EV_{DD0} \leq$ 5.5 V, 2.7 V $\leq V_b \leq$ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V $\leq EV_{DD0}$ < 4.0 V, 2.3 V $\leq V_b \leq$ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(**Notes, Caution,** and **Remarks** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ $4/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ – 75		$t_{KCY1}/2$ – 75		$t_{KCY1}/2$ – 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 170		$t_{KCY1}/2$ – 170		$t_{KCY1}/2$ – 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ – 458		$t_{KCY1}/2$ – 458		$t_{KCY1}/2$ – 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		$t_{KCY1}/2$ – 12		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		$t_{KCY1}/2$ – 18		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V **Note**, C_b = 30 pF, R_b = 5.5 kΩ		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		$t_{KCY1}/2$ – 50		ns

Note Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

($T_A = -40$ to $+85°C$, $1.8\ V \le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5\ V$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) $^{\text{Note 1}}$	t_{SIK1}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 30\ pF$, $R_b = 1.4\ k\Omega$	81		479		479		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$	177		479		479		ns
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V^{\text{Note 2}}$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$	479		479		479		ns
SIp hold time (from SCKp↑) $^{\text{Note 1}}$	t_{KSI1}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 30\ pF$, $R_b = 1.4\ k\Omega$	19		19		19		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$	19		19		19		ns
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V^{\text{Note 2}}$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$	19		19		19		ns
Delay time from SCKp↓ to SOp output $^{\text{Note 1}}$	t_{KSO1}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 30\ pF$, $R_b = 1.4\ k\Omega$		100		100		100	ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 30\ pF$, $R_b = 2.7\ k\Omega$		195		195		195	ns
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V^{\text{Note 2}}$, $C_b = 30\ pF$, $R_b = 5.5\ k\Omega$		483		483		483	ns

Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
2. Use it with $EV_{DD0} \ge V_b$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)

($T_A = -40$ to +85°C, $1.8\ V \le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5\ V$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$		1000 Note 1		300 Note 1		300 Note 1	kHz
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$		1000 Note 1		300 Note 1		300 Note 1	kHz
		$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 100\ pF$, $R_b = 2.8\ k\Omega$		400 Note 1		300 Note 1		300 Note 1	kHz
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 100\ pF$, $R_b = 2.7\ k\Omega$		400 Note 1		300 Note 1		300 ote 1	kHz
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 2, $C_b = 100\ pF$, $R_b = 5.5\ k\Omega$		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$	475		1550		1550		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$	475		1550		1550		ns
		$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 100\ pF$, $R_b = 2.8\ k\Omega$	1150		1550		1550		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 100\ pF$, $R_b = 2.7\ k\Omega$	1150		1550		1550		ns
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 2, $C_b = 100\ pF$, $R_b = 5.5\ k\Omega$	1550		1550		1550		ns
Hold time when SCLr = "H"	t_{HIGH}	$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$	245		610		610		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 50\ pF$, $R_b = 2.7\ k\Omega$	200		610		610		ns
		$4.0\ V \le EV_{DD0} \le 5.5\ V$, $2.7\ V \le V_b \le 4.0\ V$, $C_b = 100\ pF$, $R_b = 2.8\ k\Omega$	675		610		610		ns
		$2.7\ V \le EV_{DD0} < 4.0\ V$, $2.3\ V \le V_b \le 2.7\ V$, $C_b = 100\ pF$, $R_b = 2.7\ k\Omega$	600		610		610		ns
		$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$ Note 2, $C_b = 100\ pF$, $R_b = 5.5\ k\Omega$	610		610		610		ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)

($T_A = -40$ to +85°C, $1.8 V \le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5 V$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0 V$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	$4.0 V \le EV_{DD0} \le 5.5 V$, $2.7 V \le V_b \le 4.0 V$, $C_b = 50 pF$, $R_b = 2.7 k\Omega$	$1/f_{MCK}$ + 135 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		kHz
		$2.7 V \le EV_{DD0} < 4.0 V$, $2.3 V \le V_b \le 2.7 V$, $C_b = 50 pF$, $R_b = 2.7 k\Omega$	$1/f_{MCK}$ + 135 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		kHz
		$4.0 V \le EV_{DD0} \le 5.5 V$, $2.7 V \le V_b \le 4.0 V$, $C_b = 100 pF$, $R_b = 2.8 k\Omega$	$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		kHz
		$2.7 V \le EV_{DD0} < 4.0 V$, $2.3 V \le V_b \le 2.7 V$, $C_b = 100 pF$, $R_b = 2.7 k\Omega$	$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		kHz
		$1.8 V \le EV_{DD0} < 3.3 V$, $1.6 V \le V_b \le 2.0 V$ [Note 2], $C_b = 100 pF$, $R_b = 5.5 k\Omega$	$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		$1/f_{MCK}$ + 190 [Note 3]		kHz
Data hold time (transmission)	$t_{HD:DAT}$	$4.0 V \le EV_{DD0} \le 5.5 V$, $2.7 V \le V_b \le 4.0 V$, $C_b = 50 pF$, $R_b = 2.7 k\Omega$	0	305	0	305	0	305	ns
		$2.7 V \le EV_{DD0} < 4.0 V$, $2.3 V \le V_b \le 2.7 V$, $C_b = 50 pF$, $R_b = 2.7 k\Omega$	0	305	0	305	0	305	ns
		$4.0 V \le EV_{DD0} \le 5.5 V$, $2.7 V \le V_b \le 4.0 V$, $C_b = 100 pF$, $R_b = 2.8 k\Omega$	0	355	0	355	0	355	ns
		$2.7 V \le EV_{DD0} < 4.0 V$, $2.3 V \le V_b \le 2.7 V$, $C_b = 100 pF$, $R_b = 2.7 k\Omega$	0	355	0	355	0	355	ns
		$1.8 V \le EV_{DD0} < 3.3 V$, $1.6 V \le V_b \le 2.0 V$ [Note 2], $C_b = 100 pF$, $R_b = 5.5 k\Omega$	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

2. Use it with $EV_{DD0} \ge V_b$.

3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$@1 MHz to 32 MHz
$2.4 \text{ V} \leq V_{DD} \leq 5.5 \text{ V}$@1 MHz to 16 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

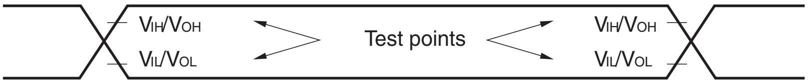
2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)
(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

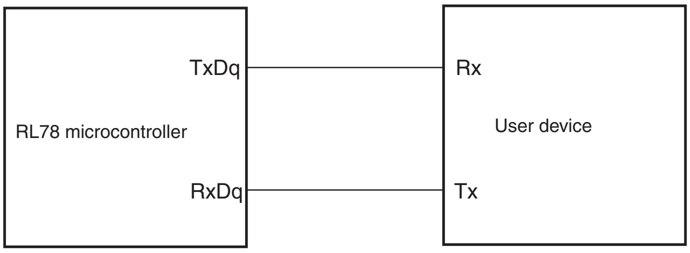
Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate Note 1					f_{MCK}/12 Note 2	bps
			Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

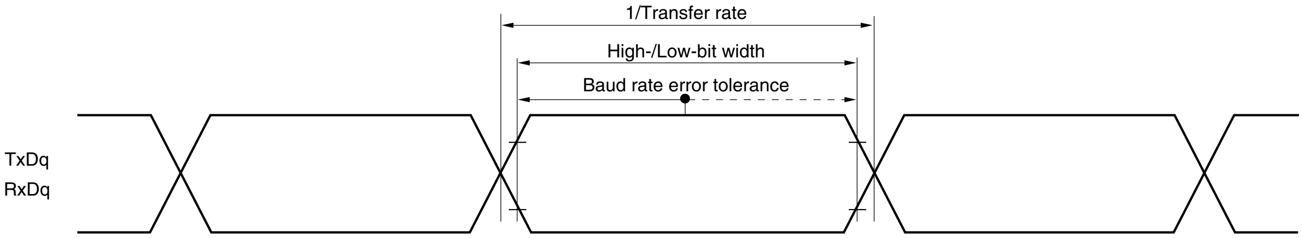
2. The following conditions are required for low voltage interface when E_{VDD0} < V_{DD}.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 20 MHz	12/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	16/f_{MCK}		ns
			f_{MCK} ≤ 16 MHz	12/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		16/f_{MCK}		ns
				12/f_{MCK} and 1000		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 − 14		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 − 16		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 − 36		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+40		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+60		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	2.4 V ≤ EV_{DD0} ≤ 5.5 V		1/f_{MCK}+62		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+66	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		2/f_{MCK}+113	ns

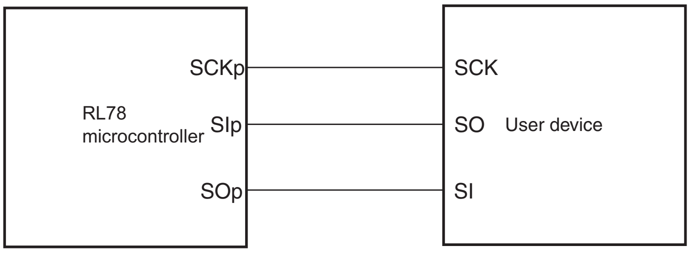
Notes
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SOp output lines.
5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
2. f_{MCK}: Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)



(4) During communication at same potential (simplified I^2C mode)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 [Note1]	kHz
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 [Note1]	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 220 [Note2]		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	$1/f_{MCK}$ + 580 [Note2]		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes **1.** The value must also be equal to or less than $f_{MCK}/4$.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution **Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin : ANI16 to ANI26	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution EV_{DD0} ≤ AV_{REFP} = V_{DD} [Notes 3, 4]	2.4 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI26		0		AV_{REFP} and EV_{DD0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR} [Note 3], Reference voltage (–) = AV_{REFM} [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error [Notes 1, 2]	E_{ZS}	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error [Note 1]	ILE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS}, the MAX. values are as follows.
Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV_{REFM}.
Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.
Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM}.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/°C
Operation stabilization wait time	t_{AMP}		5			μs

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.