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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100lhdfa-v0

Table 1-1. List of Ordering Part Numbers

(12/12)

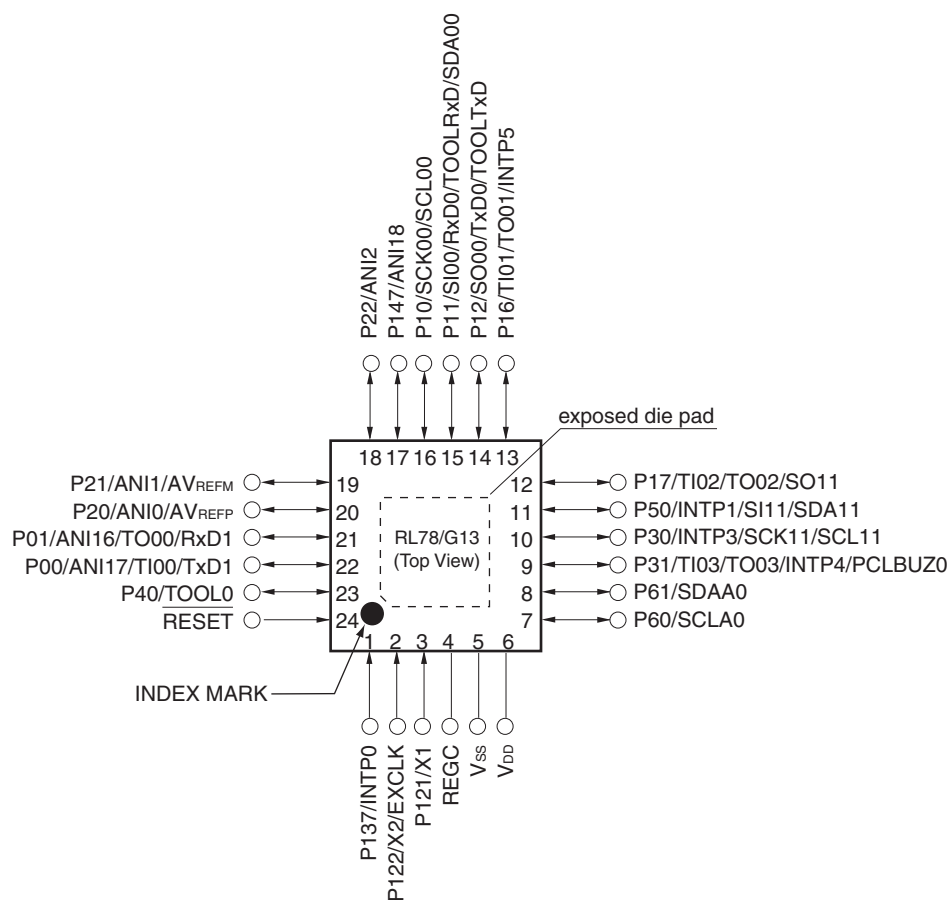
Pin count	Package	Data flash	Fields of Application ^{Note}	Ordering Part Number
128 pins	128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)	Mounted	A	R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0
			D	R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0
		Not mounted	A	R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0
			D	R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

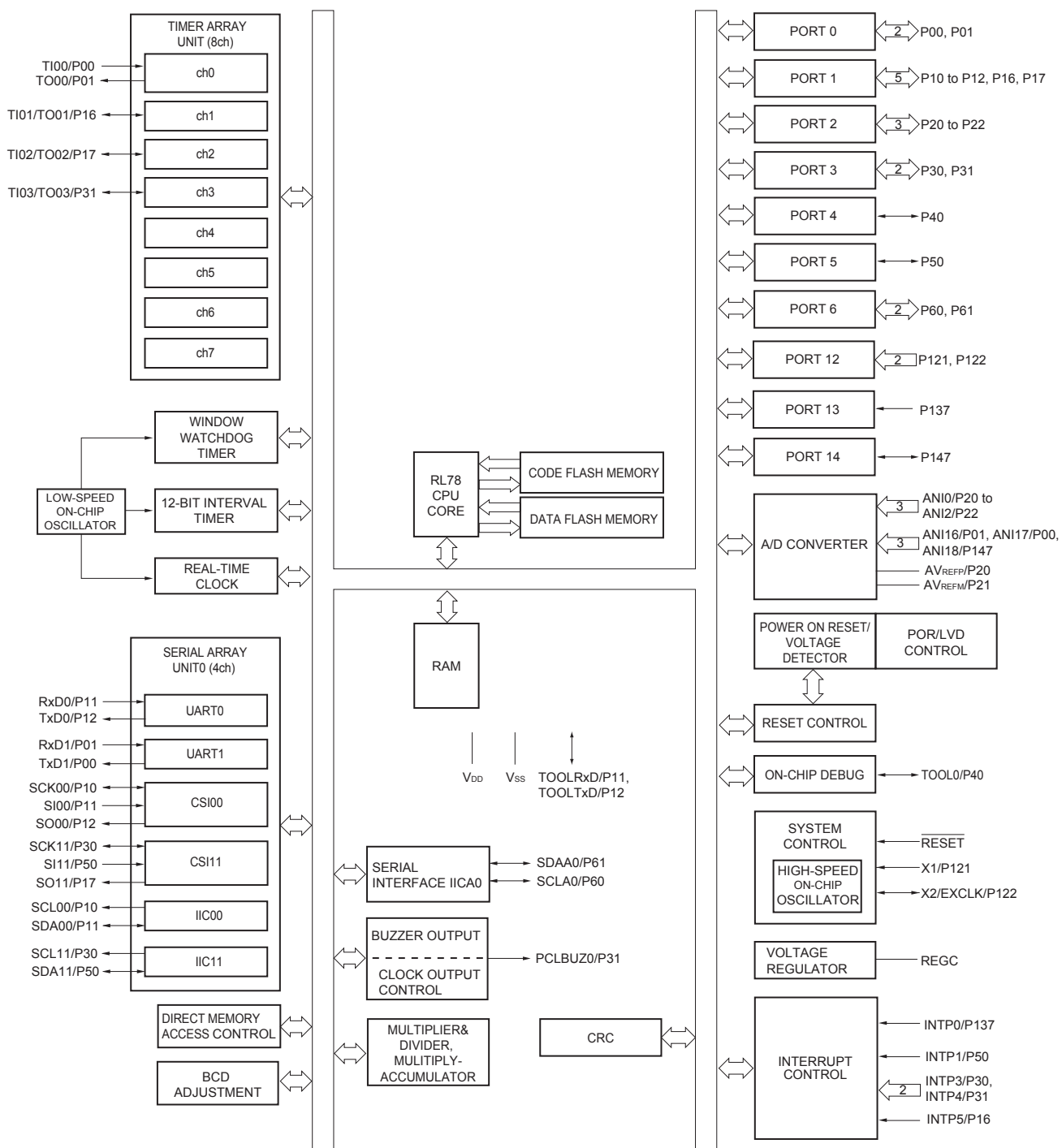


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

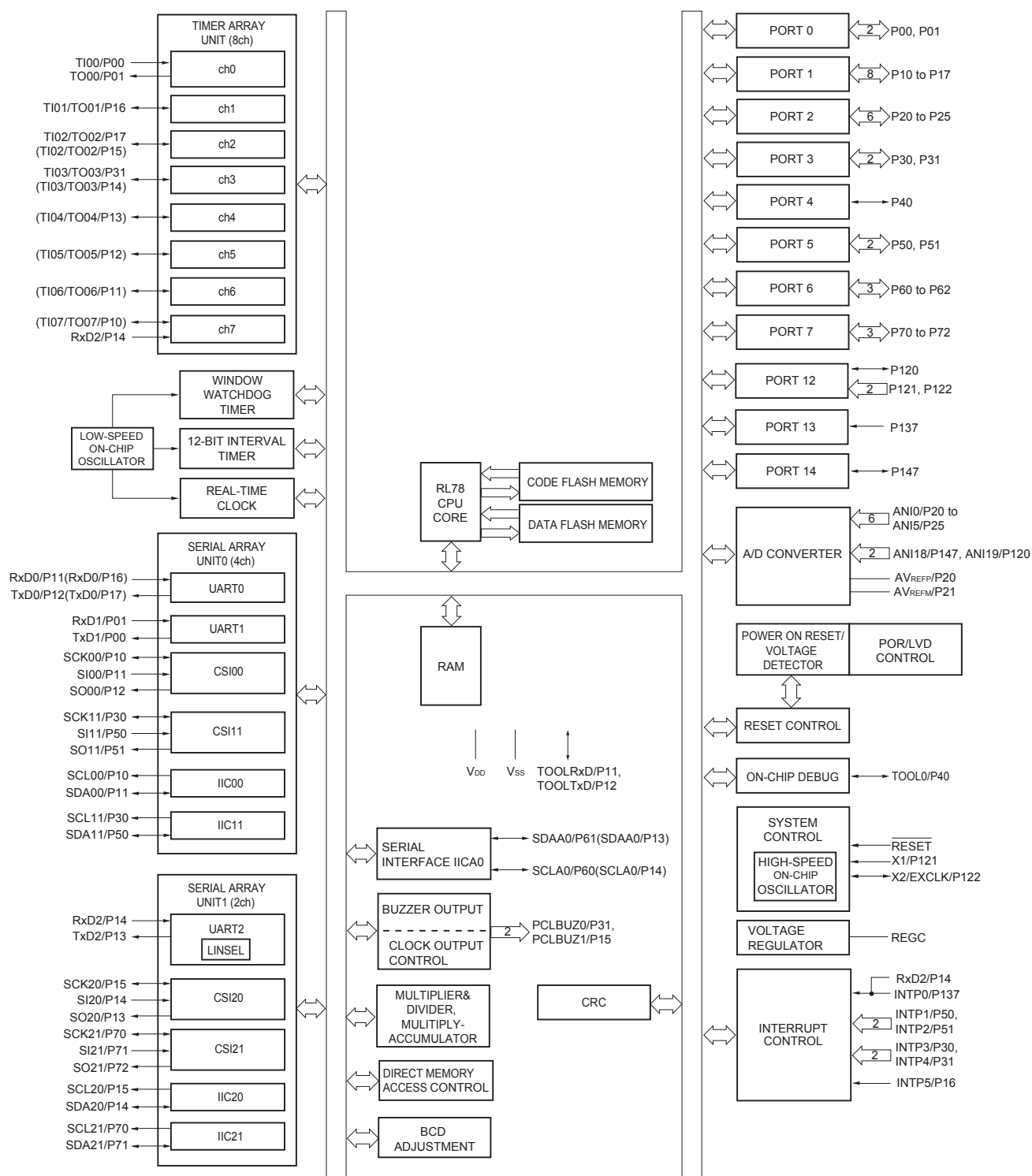
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. It is recommended to connect an exposed die pad to Vss.

1.5.2 24-pin products



1.5.6 36-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—
RAM (KB)		2 to 16 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation)									
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)									
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)									
Instruction set		<ul style="list-style-type: none">• Data transfer (8/16 bits)• Adder and subtractor/logical operation (8/16 bits)• Multiplication (8 bits × 8 bits)• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10)		31 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10)		34 (N-ch O.D. I/O [V _{DD} withstand voltage]: 11)		38 (N-ch O.D. I/O [V _{DD} withstand voltage]: 13)		48 (N-ch O.D. I/O [V _{DD} withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	—		—		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3 ^{Note2}), 8 channels (PWM outputs: 7 ^{Note2, Note3})		5 channels (PWM outputs: 4 ^{Note2}), 8 channels (PWM outputs: 7 ^{Note2}) ^{Note3}						8 channels (PWM outputs: 7 ^{Note2})	
	RTC output	1 channel • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)									

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H

R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
3. When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Lx	R5F101Lx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		<ul style="list-style-type: none">2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] <ul style="list-style-type: none">CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channelCSI: 1 channel/simplified I²C: 1 channel/UART: 1 channelCSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] <ul style="list-style-type: none">CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channelCSI: 1 channel/simplified I²C: 1 channel/UART: 1 channelCSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] <ul style="list-style-type: none">CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channelCSI: 2 channels/simplified I²C: 2 channels/UART: 1 channelCSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
		I ² C bus	1 channel		1 channel		1 channel		1 channel		1 channel
Multiplier and divider/multiply-accumulator		<ul style="list-style-type: none">16 bits × 16 bits = 32 bits (Unsigned or signed)32 bits ÷ 32 bits = 32 bits (Unsigned)16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		<ul style="list-style-type: none">Reset by RESET pinInternal reset by watchdog timerInternal reset by power-on-resetInternal reset by voltage detectorInternal reset by illegal instruction execution ^{Note}Internal reset by RAM parity errorInternal reset by illegal-memory access									
Power-on-reset circuit		<ul style="list-style-type: none">Power-on-reset: 1.51 V (TYP.)Power-down-reset: 1.50 V (TYP.)									
Voltage detector		<ul style="list-style-type: none">Rising edge : 1.67 V to 4.06 V (14 stages)Falling edge : 1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)									
Operating ambient temperature		T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)									

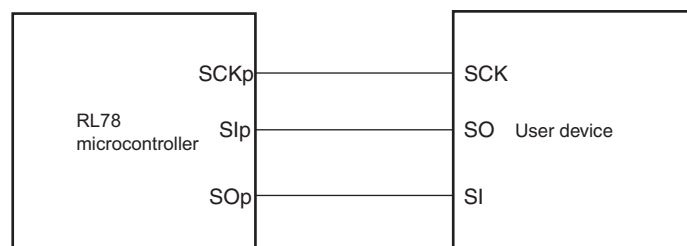
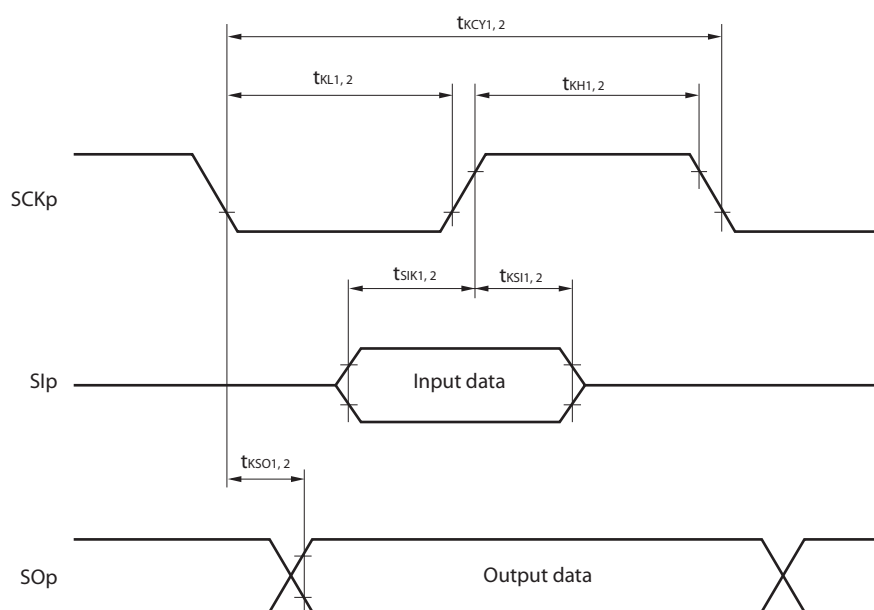
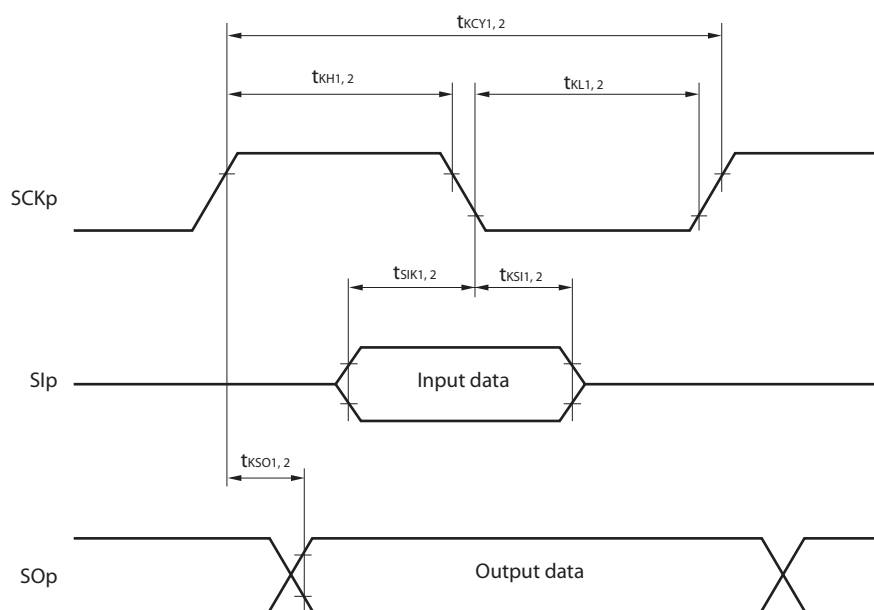
Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R>

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode**.

- Remarks**
1. f_{IL} : Low-speed on-chip oscillator clock frequency
 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 3. f_{CLK} : CPU/peripheral hardware clock frequency
 4. Temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)****CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

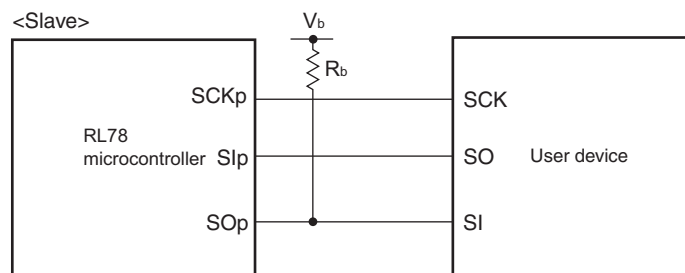
(5) During communication at same potential (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

($T_A = -40$ to $+105^{\circ}\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{DD0}		1	μA		
	I _{LH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}		1	μA		
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input	1	μA		
				In resonator connection	10	μA		
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0}		−1	μA		
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}		−1	μA		
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input	−1	μA		
				In resonator connection	−10	μA		
On-chip pll-up resistance	R _U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0} , In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}\text{C}$

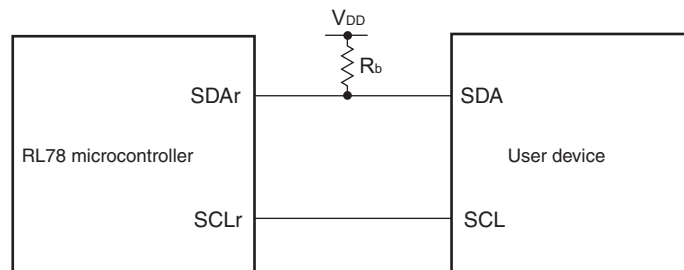
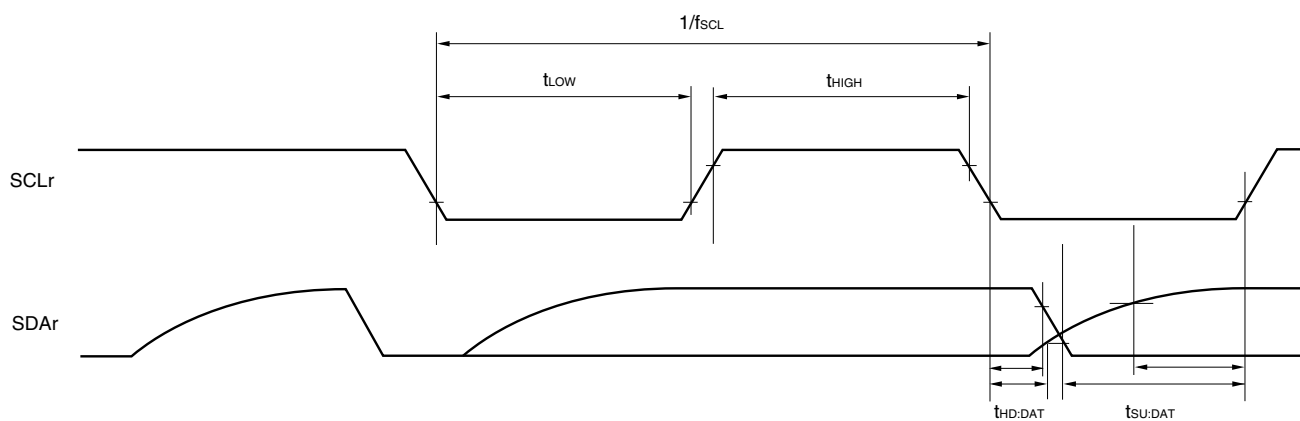
(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	250		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	500		ns
SCKp high-/low-level width	$t_{\text{KH1}}, t_{\text{KL1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 24$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 36$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 76$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI1}		38		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 4}		50	ns

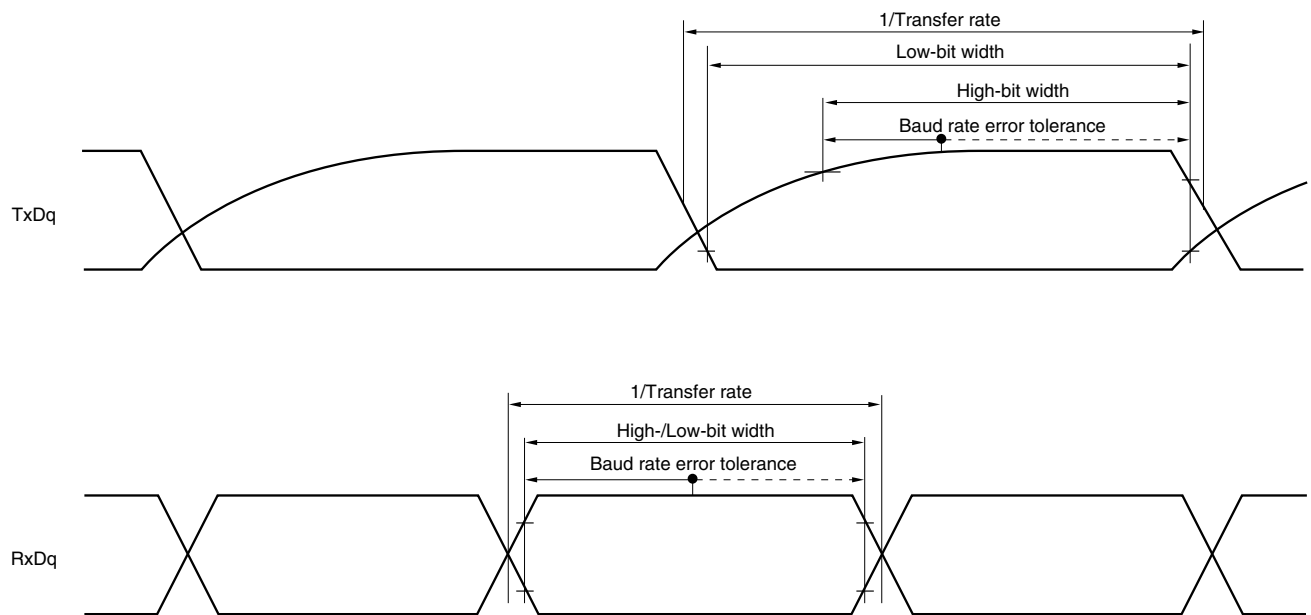
- Notes**
1. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 2. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 3. When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

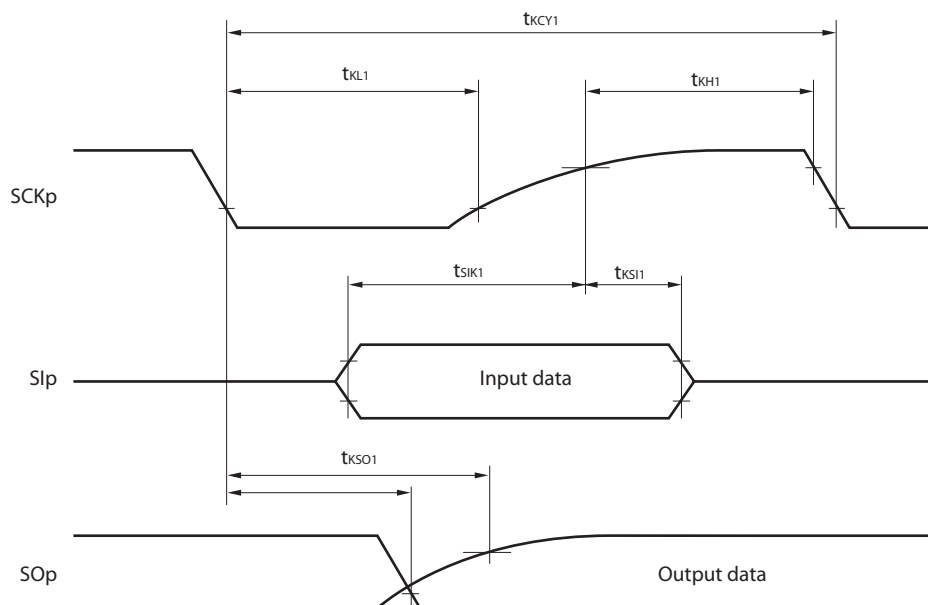
Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

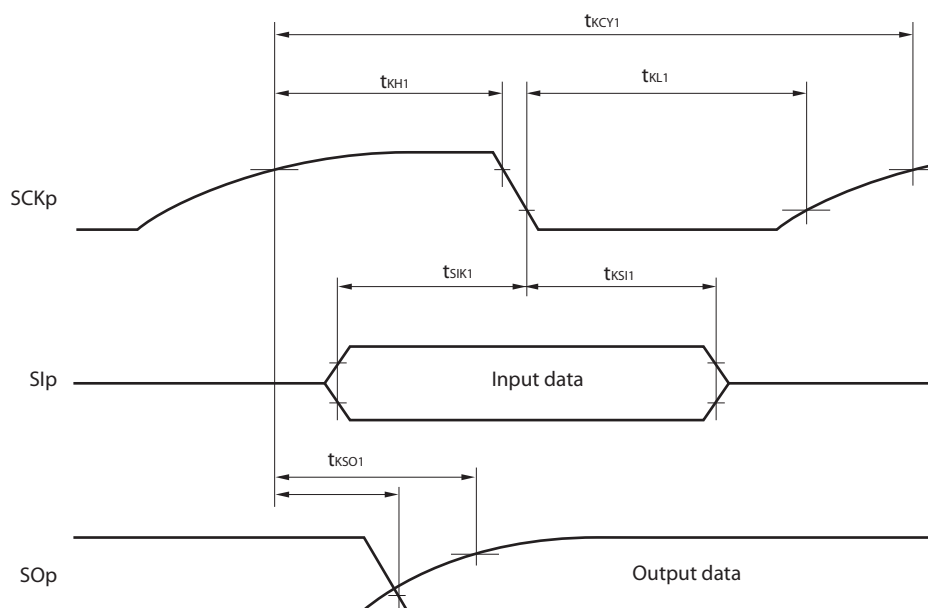
UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites <small>Notes 1,2,3</small>	C _{enwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	1,000			Times
Number of data flash rewrites <small>Notes 1,2,3</small>		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

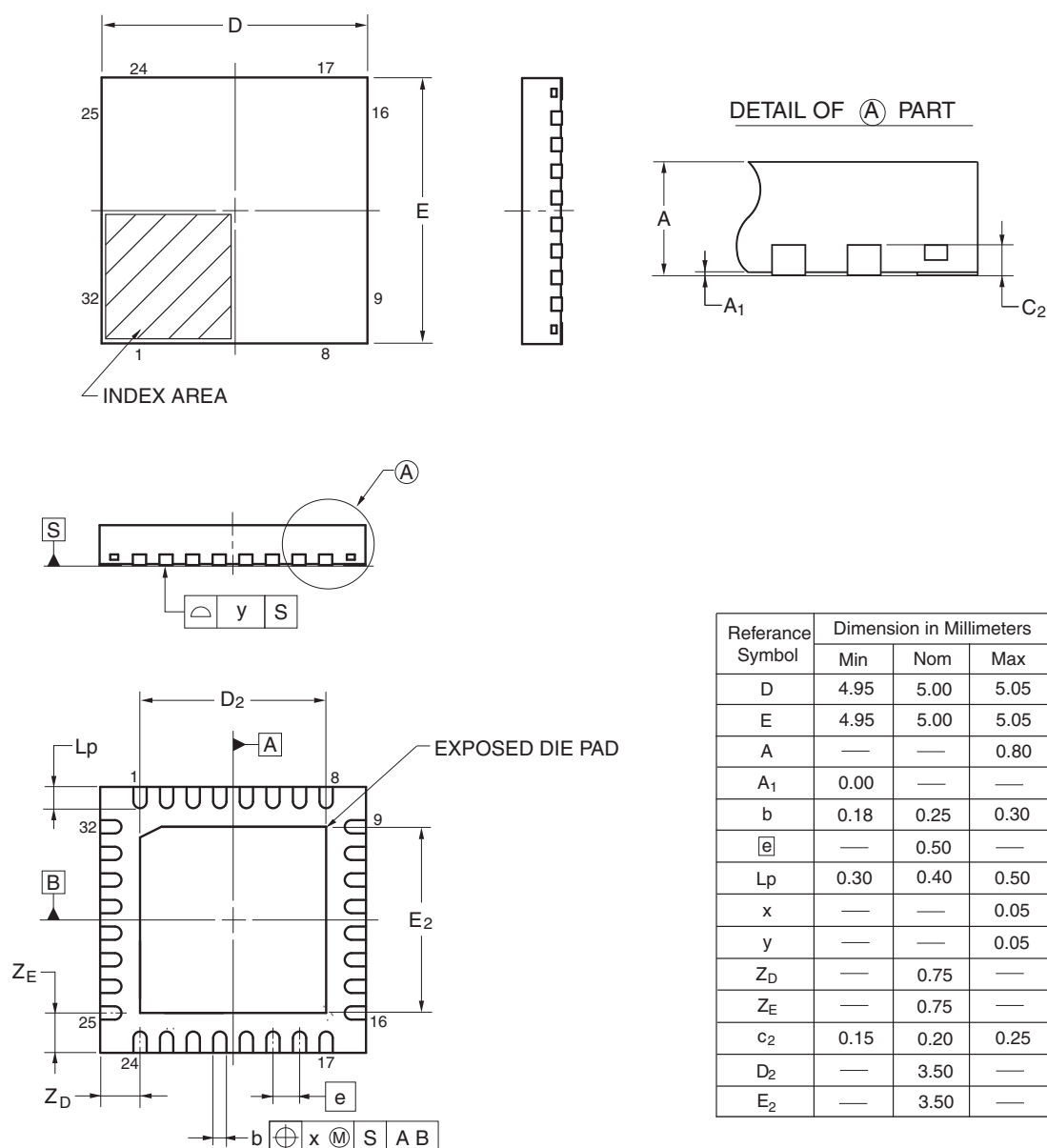
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} = V_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = V_{SS0} = V_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	118	Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		118	Modification of table and note in 2.6.3 POR circuit characteristics
		119	Modification of table in 2.6.4 LVD circuit characteristics
		120	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		120	Renamed to 2.6.5 Power supply voltage rising slope characteristics
		122	Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes
		123	Modification of caution 1 and description
		124	Modification of table and remark 3 in Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)
		126	Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics
		126	Modification of table in 3.2.2 On-chip oscillator characteristics
		127	Modification of note 3 in 3.3.1 Pin characteristics (1/5)
		128	Modification of note 3 in 3.3.1 Pin characteristics (2/5)
		133	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2)
		135	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2)
		137	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2)
		139	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2)
		140	Modification of (3) Peripheral Functions (Common to all products)
		142	Modification of table in 3.4 AC Characteristics
		143	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		143	Modification of figure of AC Timing Test Points
		143	Modification of figure of External System Clock Timing
		145	Modification of figure of AC Timing Test Points
		145	Modification of description, note 1, and caution in (1) During communication at same potential (UART mode)
		146	Modification of description in (2) During communication at same potential (CSI mode)
		147	Modification of description in (3) During communication at same potential (CSI mode)
		149	Modification of table, note 1, and caution in (4) During communication at same potential (simplified I ² C mode)
		151	Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		152 to 154	Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		155	Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		156	Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		157, 158	Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		160, 161	Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)