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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mfdfb-30">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mfdfb-30</a>

## 1.2 List of Part Numbers

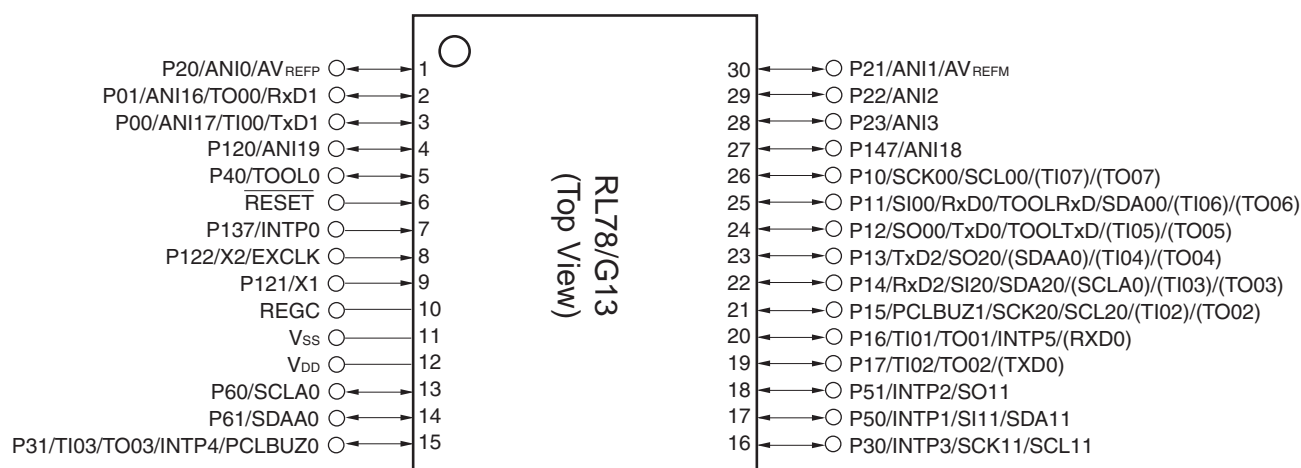
Figure 1-1. Part Number, Memory Size, and Package of RL78/G13



- Notes**
1. Products only for "A: Consumer applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )", and "G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ )"
  2. Products only for "A: Consumer applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )", and "D: Industrial applications ( $T_A = -40$  to  $+85^\circ\text{C}$ )"

## 1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

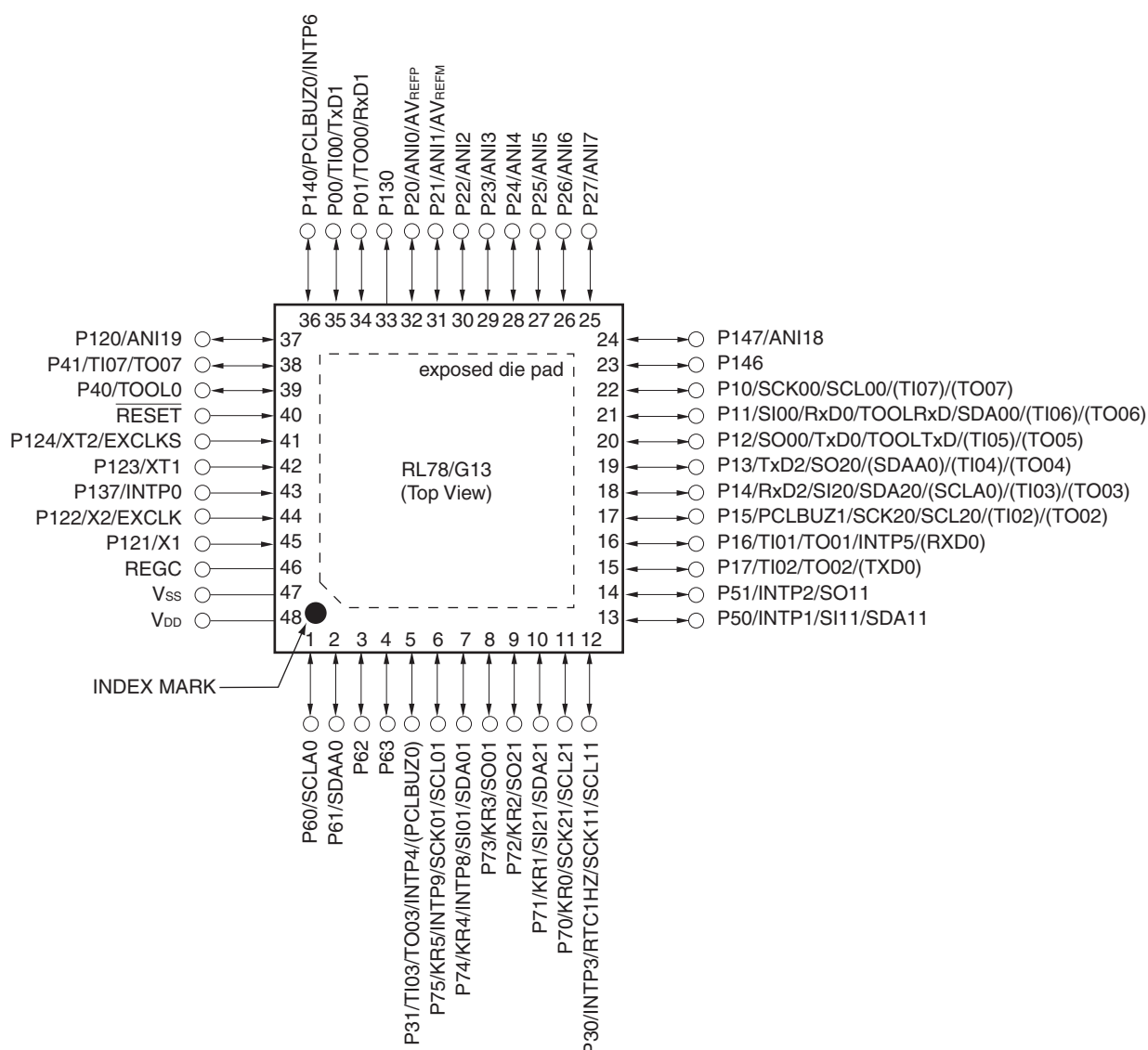


**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

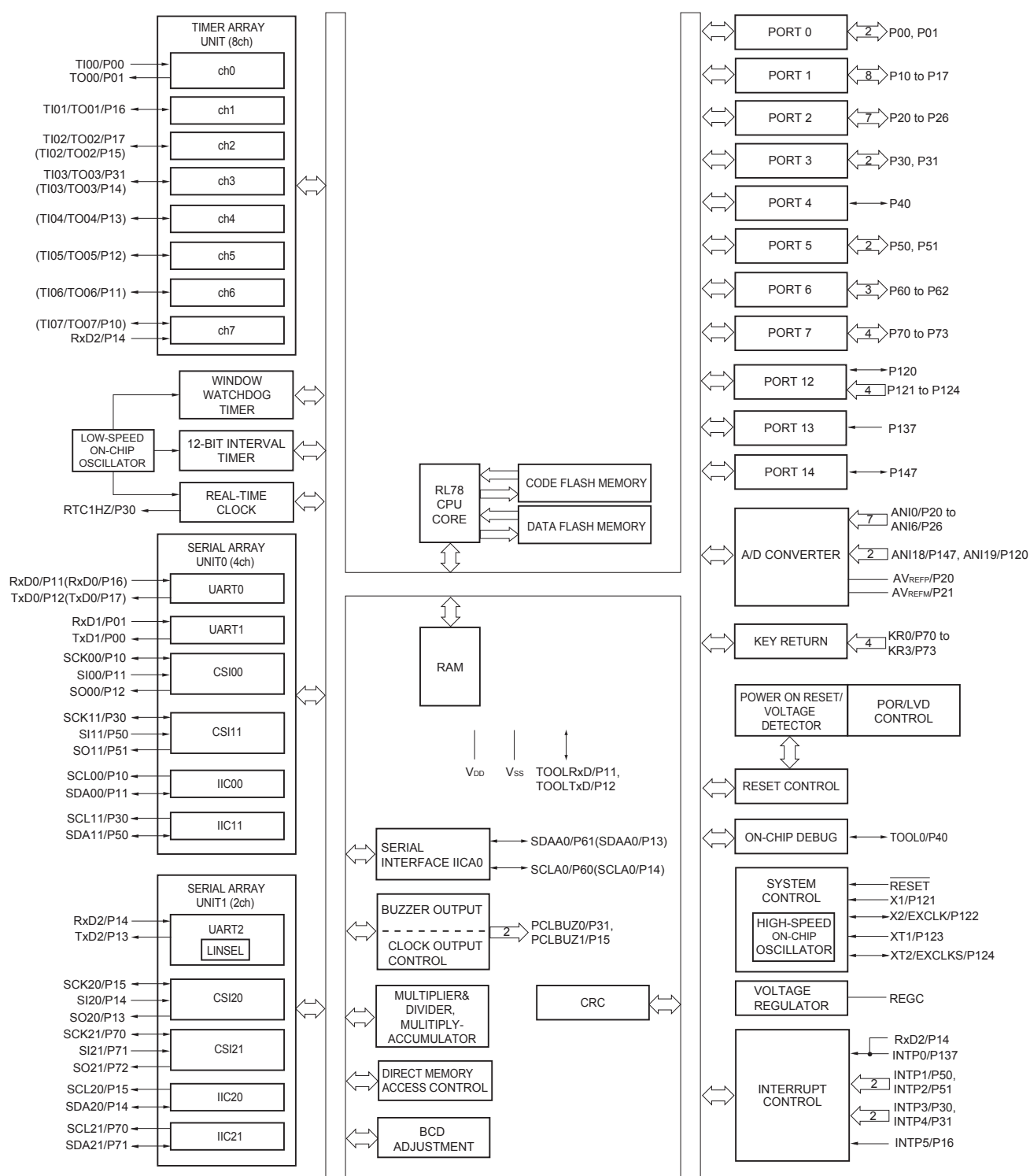


**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

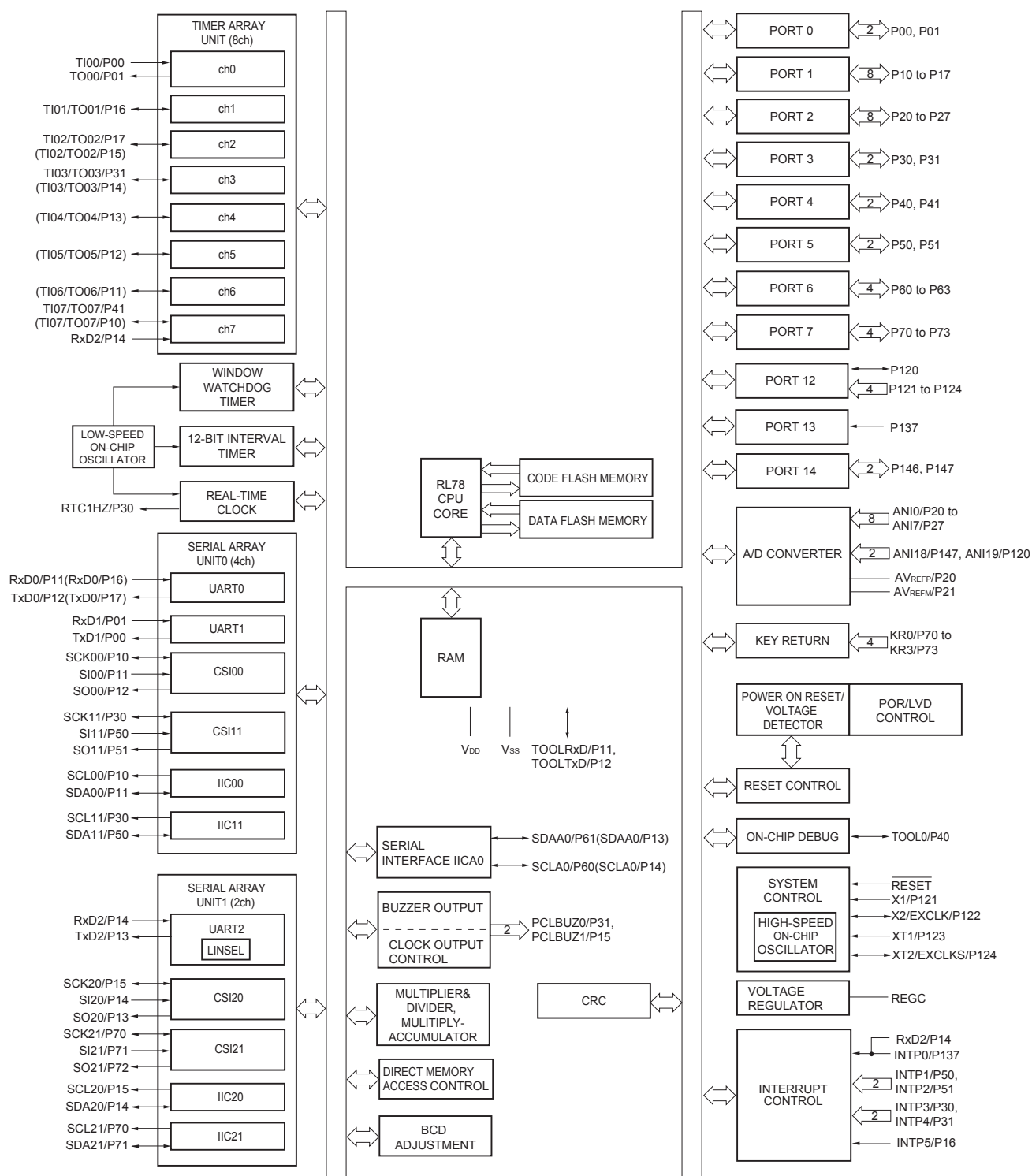
- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to Vss.

## 1.5.7 40-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.8 44-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +6.5	V
	EV <sub>DD0</sub> , EV <sub>DD1</sub>	EV <sub>DD0</sub> = EV <sub>DD1</sub>	-0.5 to +6.5	V
	EV <sub>SS0</sub> , EV <sub>SS1</sub>	EV <sub>SS0</sub> = EV <sub>SS1</sub>	-0.5 to +0.3	V
REGC pin input voltage	V <sub>IREGC</sub>	REGC	-0.3 to +2.8 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Input voltage	V <sub>I1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>I2</sub>	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V <sub>I3</sub>	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Output voltage	V <sub>O1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>O2</sub>	P20 to P27, P150 to P156	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Analog input voltage	V <sub>AI1</sub>	ANI16 to ANI26	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V
	V <sub>AI2</sub>	ANI0 to ANI14	-0.3 to V <sub>DD</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed AV<sub>REF</sub>(+) + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** AV<sub>REF</sub>(+) : + side reference voltage of the A/D converter.

**3.** V<sub>SS</sub> : Reference voltage

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I <sub>OH1</sub>	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I <sub>OH2</sub>	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
	Output current, low	I <sub>OL1</sub>	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
I <sub>OL2</sub>		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T <sub>A</sub>	In normal operation mode		−40 to +85
	In flash memory programming mode				
Storage temperature	T <sub>stg</sub>			−65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



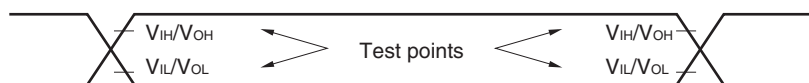
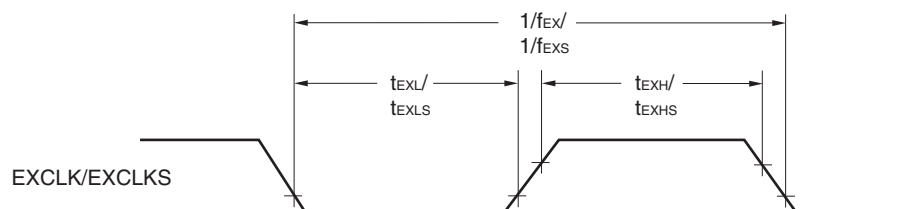
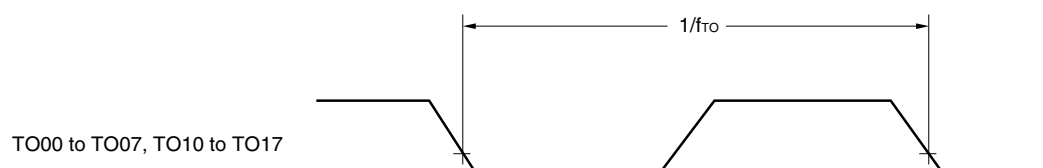
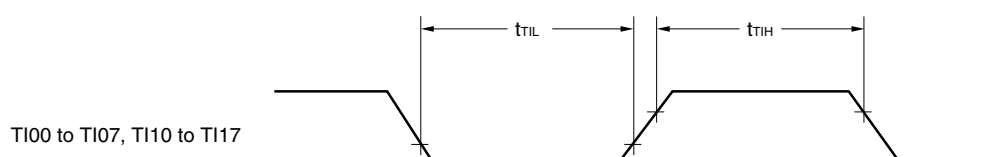
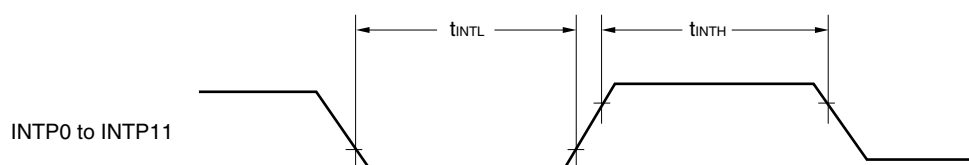
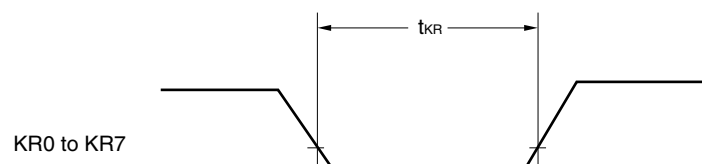
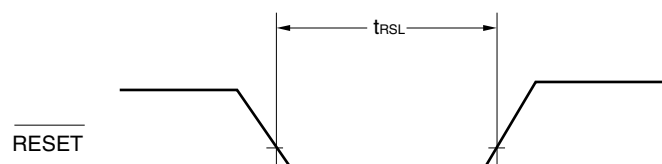
**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)**

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	f <sub>IH</sub> = 32 MHz Note 3	Basic operation	V <sub>DD</sub> = 5.0 V		2.3		mA
						V <sub>DD</sub> = 3.0 V		2.3		mA
					Normal operation	V <sub>DD</sub> = 5.0 V		5.2	8.5	mA
						V <sub>DD</sub> = 3.0 V		5.2	8.5	mA
				f <sub>IH</sub> = 24 MHz Note 3	Normal operation	V <sub>DD</sub> = 5.0 V		4.1	6.6	mA
						V <sub>DD</sub> = 3.0 V		4.1	6.6	mA
				f <sub>IH</sub> = 16 MHz Note 3	Normal operation	V <sub>DD</sub> = 5.0 V		3.0	4.7	mA
						V <sub>DD</sub> = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode Note 5	f <sub>IH</sub> = 8 MHz Note 3	Normal operation	V <sub>DD</sub> = 3.0 V		1.3	2.1	mA
						V <sub>DD</sub> = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode Note 5	f <sub>IH</sub> = 4 MHz Note 3	Normal operation	V <sub>DD</sub> = 3.0 V		1.3	1.8	mA
						V <sub>DD</sub> = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode Note 5	f <sub>MX</sub> = 20 MHz Note 2, V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f <sub>MX</sub> = 20 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f <sub>MX</sub> = 10 MHz Note 2, V <sub>DD</sub> = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f <sub>MX</sub> = 10 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode Note 5	f <sub>MX</sub> = 8 MHz Note 2, V <sub>DD</sub> = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f <sub>MX</sub> = 8 MHz Note 2, V <sub>DD</sub> = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = -40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f <sub>SUB</sub> = 32.768 kHz Note 4 T <sub>A</sub> = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.**  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- 2.**  $f_{IH}$ : High-speed on-chip oscillator clock frequency
- 3.**  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
- 4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**AC Timing Test Points****External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

## (3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t <sub>KH1</sub> , t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 38		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		t <sub>KCY1</sub> /2 – 100		t <sub>KCY1</sub> /2 – 100		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t <sub>KSI1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t <sub>KSO1</sub>	1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			25		25		25	ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V C = 30 pF <small>Note 4</small>			—		25		25	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	t <sub>KCY2</sub> /2 - 12		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	t <sub>KCY2</sub> /2 - 18		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 3</sup>	t <sub>SIK2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
Slp hold time (from SCKp↑) <sup>Note 4</sup>	t <sub>KS12</sub>		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		ns
Delay time from SCKp↓ to SOp output <sup>Note 5</sup>	t <sub>KSO2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ		2/f <sub>MCK</sub> + 120		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ		2/f <sub>MCK</sub> + 214		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns

**Notes** 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t <sub>SU:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
Data hold time (transmission)	t <sub>HD:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	ns

**Notes** 1. The value must also be equal to or less than f<sub>MCK</sub>/4.2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.3. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

## 2.8 Flash Memory Programming Characteristics

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	$f_{CLK}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	$C_{erwr}$	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

**Notes** 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9 Dedicated Flash Memory Programmer Communication (UART)

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (4/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	$\text{V}_{\text{OH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	$\text{V}_{\text{OH2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	$\text{V}_{\text{OL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	$\text{V}_{\text{OL2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	$\text{V}_{\text{OL3}}$	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

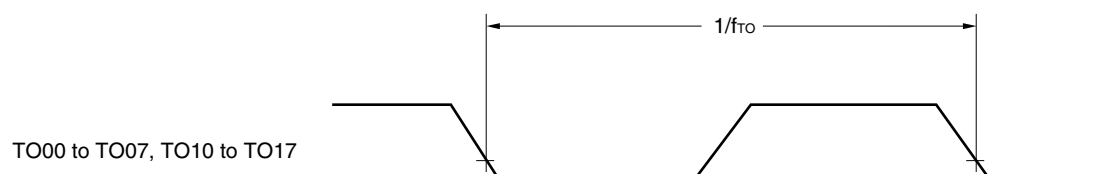
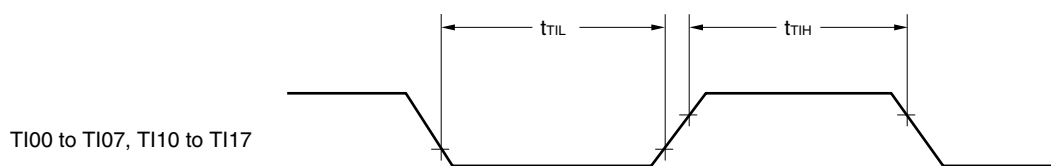
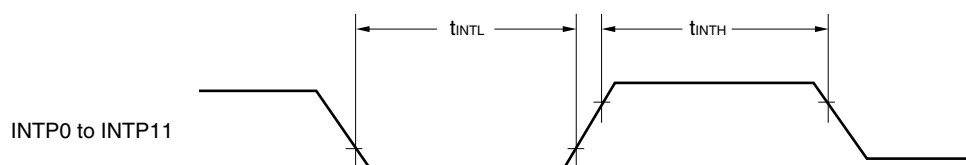
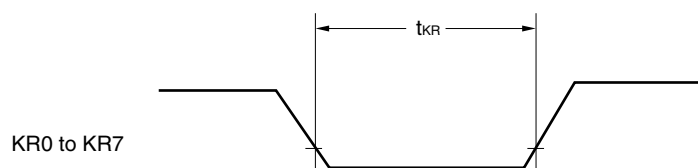
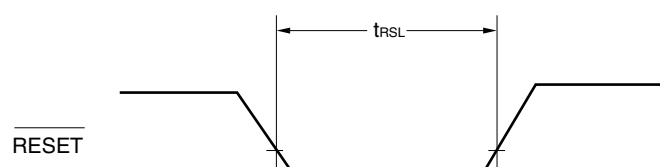


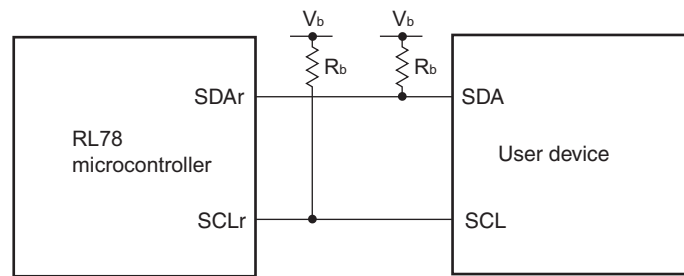
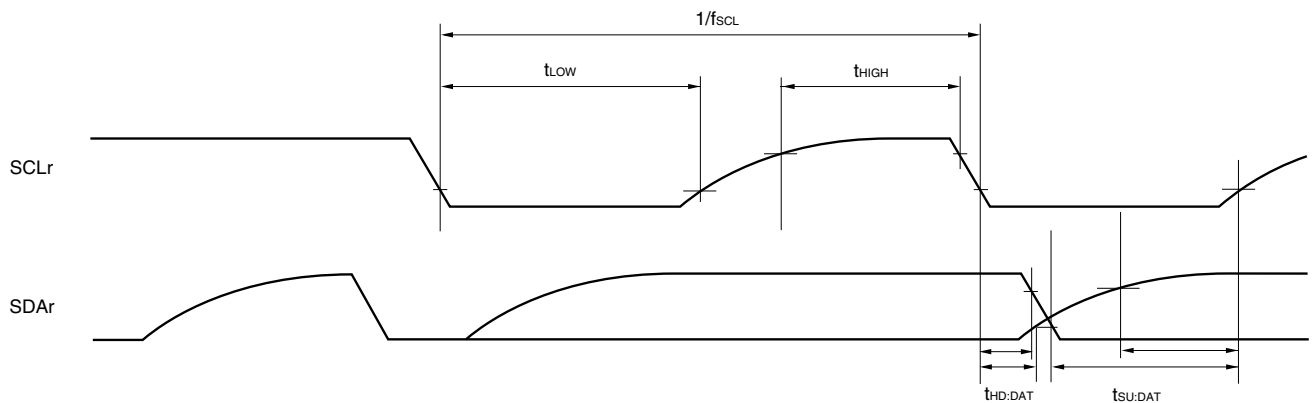
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

**Simplified I<sup>2</sup>C mode connection diagram (during communication at different potential)****Simplified I<sup>2</sup>C mode serial transfer timing (during communication at different potential)**

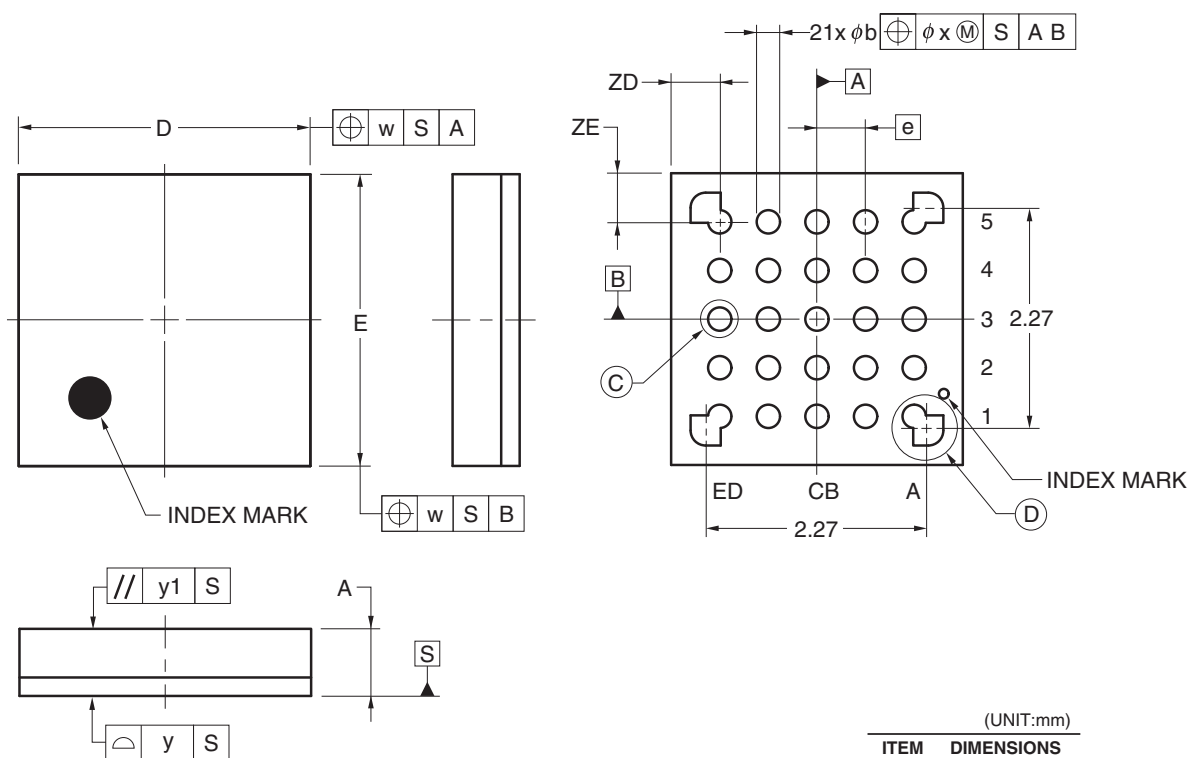
**Caution** Select the TTL input buffer and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage
  2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

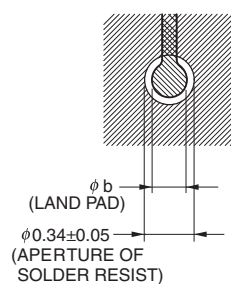
## 4.3 25-pin Products

R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA  
 R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA  
 R5F1008AGLA, R5F1008CGLA, R5F1008DGLA, R5F1008EGLA

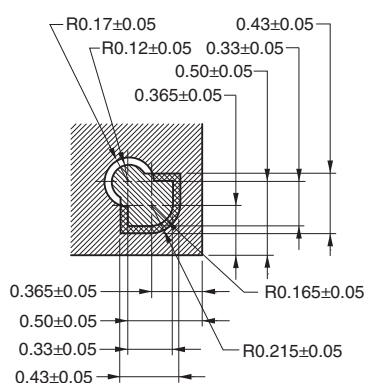
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01



DETAIL OF © PART



DETAIL OF © PART

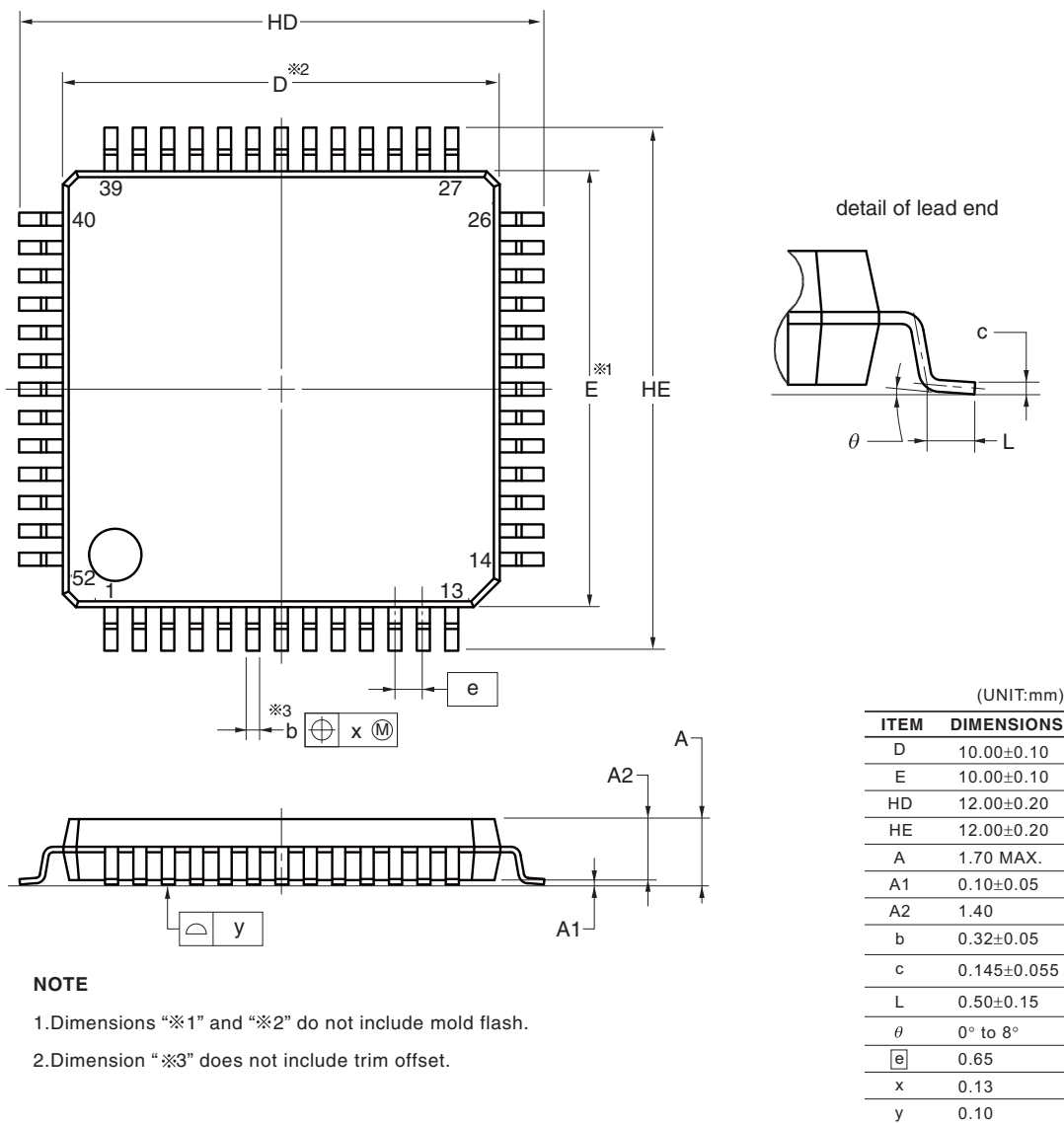


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## 4.10 52-pin Products

R5F100JCAFA, R5F100JDFA, R5F100JEFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFA, R5F100JKFA, R5F100JLAFA  
 R5F101JCAFA, R5F101JDFA, R5F101JEFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFA, R5F101JKFA, R5F101JLAFA  
 R5F100JCDA, R5F100JDDA, R5F100JEDA, R5F100JFDA, R5F100JGDA, R5F100JHDA, R5F100JJDA, R5F100JKDA, R5F100JLDA  
 R5F101JCDA, R5F101JDDA, R5F101JEDA, R5F101JFDA, R5F101JGDA, R5F101JHDA, R5F101JJDA, R5F101JKDA, R5F101JLDA  
 R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



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