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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mfdfb-50">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mfdfb-50</a>

Table 1-1. List of Ordering Part Numbers

(8/12)

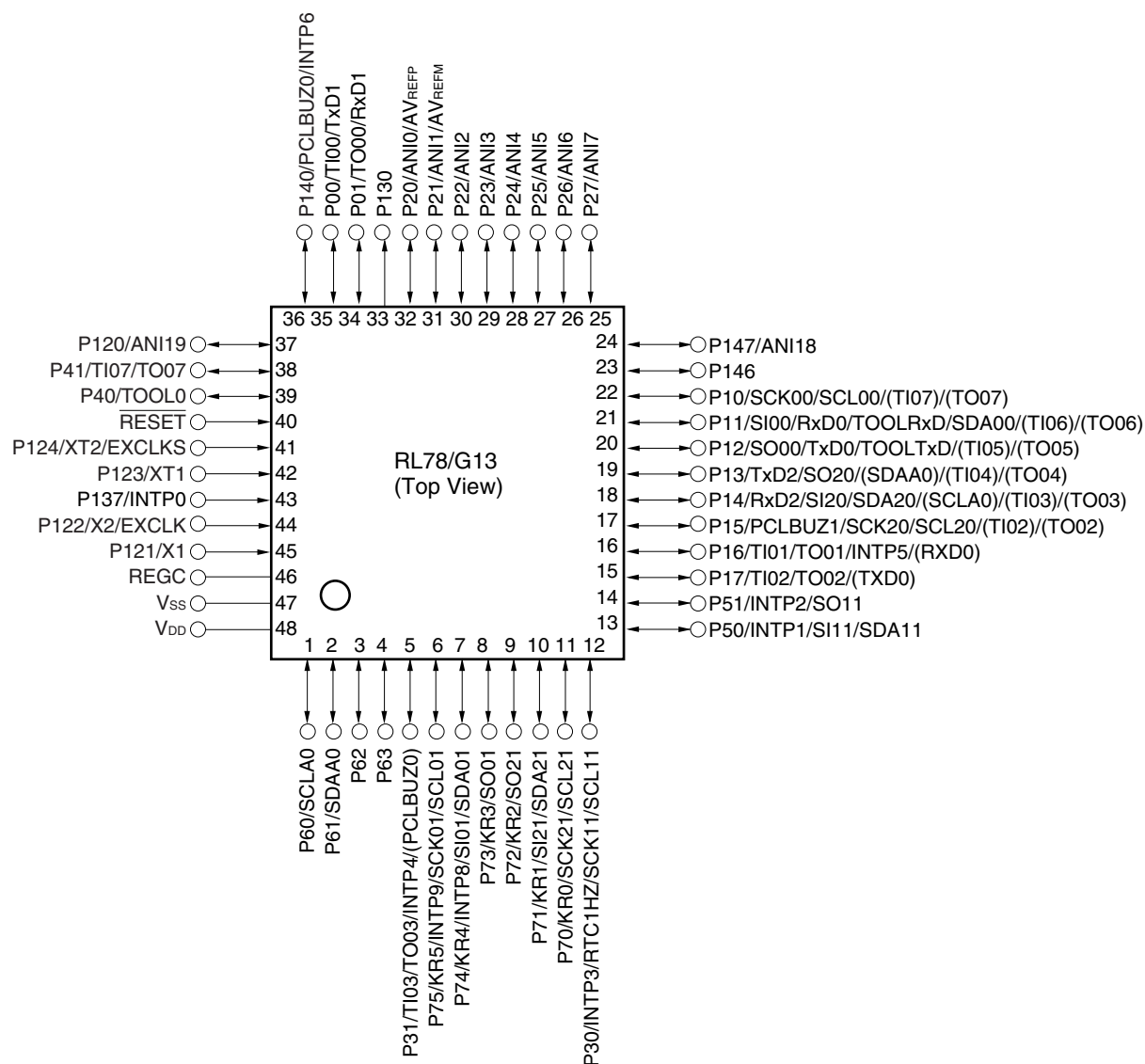
Pin count	Package	Data flash	Fields of Application <sup>Note</sup>	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJFAFA#V0, R5F100LKFAFA#V0, R5F100LLAFA#V0 R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0, R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJFAFA#X0, R5F100LKFAFA#X0, R5F100LLAFA#X0 R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDAFA#V0, R5F100LHDAFA#V0, R5F100LJDAFA#V0, R5F100LKDAFA#V0, R5F100LLDAFA#V0 R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDAFA#X0, R5F100LHDAFA#X0, R5F100LJDAFA#X0, R5F100LKDAFA#X0, R5F100LLDAFA#X0 R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0 R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0 R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0 R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJFAFA#V0, R5F101LKFAFA#V0, R5F101LLAFA#V0 R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0, R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJFAFA#X0, R5F101LKFAFA#X0, R5F101LLAFA#X0 R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDAFA#V0, R5F101LHDAFA#V0, R5F101LJDAFA#V0, R5F101LKDAFA#V0, R5F101LLDAFA#V0 R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDAFA#X0, R5F101LHDAFA#X0, R5F101LJDAFA#X0, R5F101LKDAFA#X0, R5F101LLDAFA#X0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.3.9 48-pin products

- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)

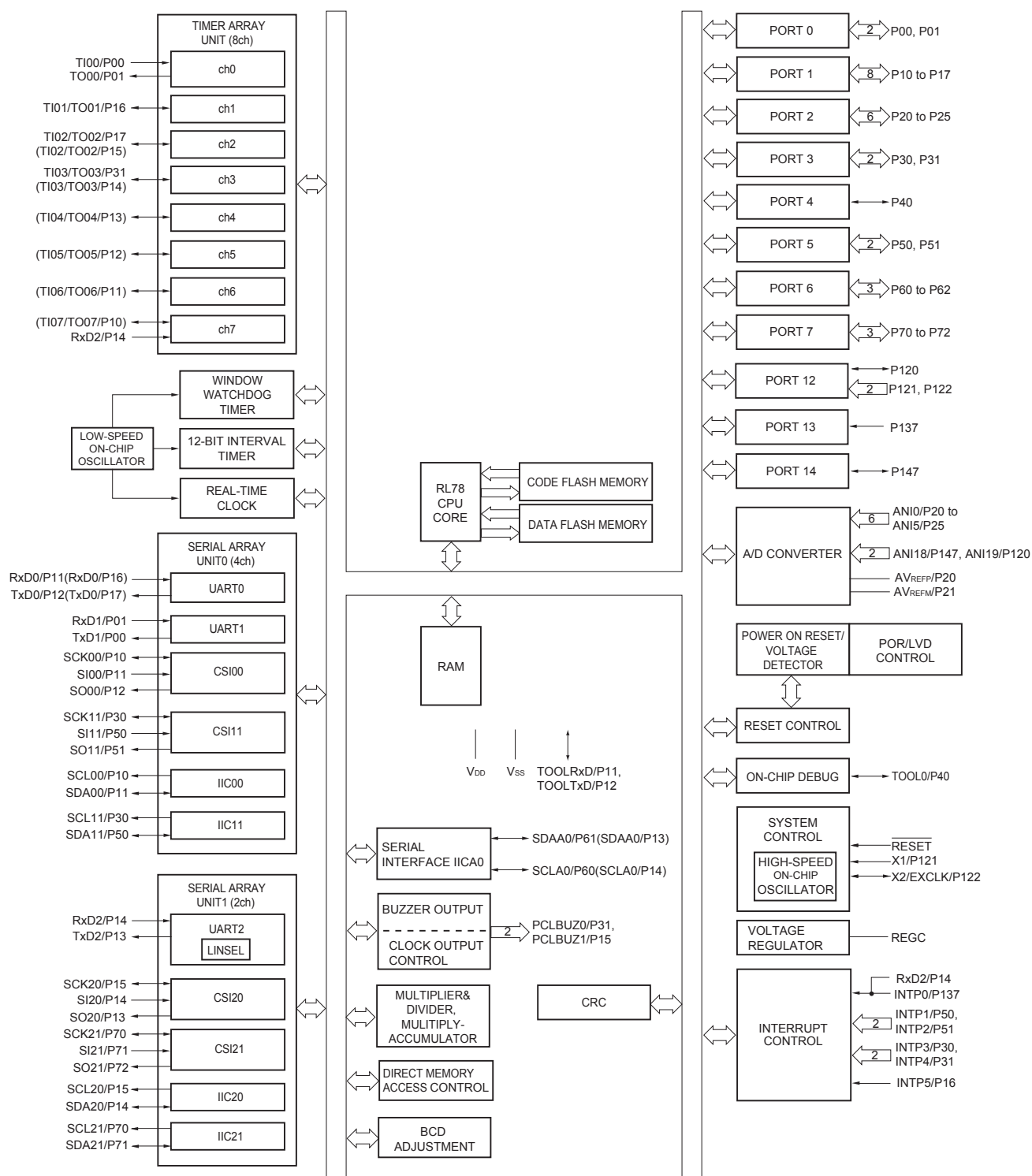


**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.6 36-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxAxx, R5F101xxAxx

D: Industrial applications  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxDxx, R5F101xxDxx

G: Industrial applications when  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $EV_{DD0}$ ,  $EV_{DD1}$ ,  $EV_{SS0}$ , or  $EV_{SS1}$  pin, replace  $EV_{DD0}$  and  $EV_{DD1}$  with  $V_{DD}$ , or replace  $EV_{SS0}$  and  $EV_{SS1}$  with  $V_{SS}$ .
  3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.

## 2.3 DC Characteristics

## 2.3.1 Pin characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-10.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-55.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-10.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		-5.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-80.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-19.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		-10.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		-5.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-135.0 <sup>Note 4</sup>	mA
	I <sub>OH2</sub>	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		-1.5	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>DD</sub> pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is -100 mA.

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I <sub>OL</sub> <sup>Note 1</sup>	I <sub>OL1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			20.0 <sup>Note 2</sup>	mA
		Per pin for P60 to P63			15.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		70.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		15.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		9.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		80.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		35.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		20.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )			150.0	mA
	I <sub>OL2</sub>	Per pin for P20 to P27, P150 to P156			0.4 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		5.0	mA

- Notes**
1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV<sub>SS0</sub>, EV<sub>SS1</sub> and V<sub>SS</sub> pin.
  2. However, do not exceed the total current value.
  3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OL</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OL</sub> = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \cong 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV <sub>DD0</sub>	EV <sub>DD0</sub>	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	2.2	EV <sub>DD0</sub>	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	2.0	EV <sub>DD0</sub>	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	1.5	EV <sub>DD0</sub>	V
	V <sub>IH3</sub>	P20 to P27, P150 to P156	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH4</sub>	P60 to P63	0.7EV <sub>DD0</sub>		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	0.2EV <sub>DD0</sub>	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	0	0.32	V
	V <sub>IL3</sub>	P20 to P27, P150 to P156	0		0.3V <sub>DD</sub>	V
	V <sub>IL4</sub>	P60 to P63	0		0.3EV <sub>DD0</sub>	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V <sub>DD</sub>	V

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV<sub>DD0</sub>, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



**(4) Peripheral Functions (Common to all products)****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I <sub>FIL</sub> <sup>Note 1</sup>				0.20		μA
RTC operating current	I <sub>RTC</sub> <sup>Notes 1, 2, 3</sup>				0.02		μA
12-bit interval timer operating current	I <sub>IT</sub> <sup>Notes 1, 2, 4</sup>				0.02		μA
Watchdog timer operating current	I <sub>WDT</sub> <sup>Notes 1, 2, 5</sup>	f <sub>IL</sub> = 15 kHz			0.22		μA
A/D converter operating current	I <sub>ADC</sub> <sup>Notes 1, 6</sup>	When conversion at maximum speed	Normal mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I <sub>ADREF</sub> <sup>Note 1</sup>				75.0		μA
Temperature sensor operating current	I <sub>TMPS</sub> <sup>Note 1</sup>				75.0		μA
LVD operating current	I <sub>LVI</sub> <sup>Notes 1, 7</sup>				0.08		μA
Self-programming operating current	I <sub>FSP</sub> <sup>Notes 1, 9</sup>				2.50	12.20	mA
BGO operating current	I <sub>BGO</sub> <sup>Notes 1, 8</sup>				2.50	12.20	mA
SNOOZE operating current	I <sub>SNOZ</sub> <sup>Note 1</sup>	ADC operation	The mode is performed <sup>Note 10</sup>		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV <sub>REFP</sub> = V <sub>DD</sub> = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

**Notes** 1. Current flowing to V<sub>DD</sub>.

- When high speed on-chip oscillator and high-speed system clock are stopped.
- Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I<sub>DD1</sub> or I<sub>DD2</sub>, and I<sub>RTC</sub>, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I<sub>FIL</sub> should be added. I<sub>DD2</sub> subsystem clock operation includes the operational current of the real-time clock.
- Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I<sub>DD1</sub> or I<sub>DD2</sub>, and I<sub>IT</sub>, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I<sub>FIL</sub> should be added.
- Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I<sub>DD1</sub>, I<sub>DD2</sub> or I<sub>DD3</sub> and I<sub>WDT</sub> when the watchdog timer is in operation.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**  
**(3/3)**

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) <sup>Note 1</sup>	t <sub>KSH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output <sup>Note 1</sup>	t <sub>KSO1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ		25		25		25	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**Remark** The electrical characteristics of the products G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ ) are different from those of the products “A: Consumer applications, and D: Industrial applications”. For details, refer to 3.1 to 3.10.

### 3.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ ) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	$V_{DD}$		$-0.5$ to $+6.5$	V
	$EV_{DD0}$ , $EV_{DD1}$	$EV_{DD0} = EV_{DD1}$	$-0.5$ to $+6.5$	V
	$EV_{SS0}$ , $EV_{SS1}$	$EV_{SS0} = EV_{SS1}$	$-0.5$ to $+0.3$	V
REGC pin input voltage	$V_{IREGC}$	REGC	$-0.3$ to $+2.8$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 1</sup>	V
Input voltage	$V_{I1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
	$V_{I2}$	P60 to P63 (N-ch open-drain)	$-0.3$ to $+6.5$	V
	$V_{I3}$	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	$-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
Output voltage	$V_{O1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
	$V_{O2}$	P20 to P27, P150 to P156	$-0.3$ to $V_{DD} + 0.3$ <sup>Note 2</sup>	V
Analog input voltage	$V_{AI1}$	ANI16 to ANI26	$-0.3$ to $EV_{DD0} + 0.3$ and $-0.3$ to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 3</sup>	V
	$V_{AI2}$	ANI0 to ANI14	$-0.3$ to $V_{DD} + 0.3$ and $-0.3$ to $AV_{REF(+)} + 0.3$ <sup>Notes 2, 3</sup>	V

- Notes 1.** Connect the REGC pin to  $V_{SS}$  via a capacitor (0.47 to 1  $\mu\text{F}$ ). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
- 2.** Must be 6.5 V or lower.
- 3.** Do not exceed  $AV_{REF(+)} + 0.3$  V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
- 2.**  $AV_{REF(+)}$  : + side reference voltage of the A/D converter.
- 3.**  $V_{SS}$  : Reference voltage

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (2/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, $\text{I}_{\text{OL}}$ <sup>Note 1</sup>	$\text{I}_{\text{OL1}}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			8.5 <sup>Note 2</sup>	mA
		Per pin for P60 to P63			15.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$		15.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$		40.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$		35.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$		20.0	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )			80.0	mA
	$\text{I}_{\text{OL2}}$	Per pin for P20 to P27, P150 to P156			0.4 <sup>Note 2</sup>	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		5.0	mA

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the  $\text{EV}_{\text{SS0}}$ ,  $\text{EV}_{\text{SS1}}$  and  $\text{V}_{\text{SS}}$  pin.
  - Do not exceed the total current value.
  - Specification under conditions where the duty factor  $\leq 70\%$ .  
The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
    - Total output current of pins =  $(\text{I}_{\text{OL}} \times 0.7) / (n \times 0.01)$   
 $\text{<Example>}$  Where  $n = 80\%$  and  $\text{I}_{\text{OL}} = 10.0\text{ mA}$   
 Total output current of pins =  $(10.0 \times 0.7) / (80 \times 0.01) \cong 8.7\text{ mA}$   
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor.  
 A current higher than the absolute maximum rating must not flow into one pin.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### 3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD0} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = 0\text{ V}$ ) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	$f_{IH} = 32\text{ MHz}$ Note 3	Basic operation	$V_{DD} = 5.0\text{ V}$		2.1		mA
						$V_{DD} = 3.0\text{ V}$		2.1		mA
					Normal operation	$V_{DD} = 5.0\text{ V}$		4.6	7.5	mA
						$V_{DD} = 3.0\text{ V}$		4.6	7.5	mA
				$f_{IH} = 24\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		3.7	5.8	mA
						$V_{DD} = 3.0\text{ V}$		3.7	5.8	mA
				$f_{IH} = 16\text{ MHz}$ Note 3	Normal operation	$V_{DD} = 5.0\text{ V}$		2.7	4.2	mA
						$V_{DD} = 3.0\text{ V}$		2.7	4.2	mA
			HS (high-speed main) mode Note 5	$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 20\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 5.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				$f_{MX} = 10\text{ MHz}$ Note 2, $V_{DD} = 3.0\text{ V}$	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
		Subsystem clock operation		$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	$\mu\text{A}$
						Resonator connection		4.2	5.0	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.1	4.9	$\mu\text{A}$
						Resonator connection		4.2	5.0	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		4.2	5.5	$\mu\text{A}$
						Resonator connection		4.3	5.6	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		4.3	6.3	$\mu\text{A}$
						Resonator connection		4.4	6.4	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		4.6	7.7	$\mu\text{A}$
						Resonator connection		4.7	7.8	$\mu\text{A}$
				$f_{SUB} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		6.9	19.7	$\mu\text{A}$
						Resonator connection		7.0	19.8	$\mu\text{A}$

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note</sup>	$t_{SIK1}$	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) <sup>Note</sup>	$t_{KSI1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output <sup>Note</sup>	$t_{KSO1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$ , $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ , $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$		50	ns

**Note** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $V_{DD}$  tolerance (for the 20- to 52-pin products)/ $EV_{DD}$  tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



(2) When reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (–) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), target pin : ANI16 to ANI26

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$ , Reference voltage (+) =  $AV_{REFP}$ , Reference voltage (–) =  $AV_{REFM} = 0\text{ V}$ )

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error <sup>Note 1</sup>	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	$\pm 5.0$	LSB
Conversion time	$t_{CONV}$	10-bit resolution Target pin : ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	$\mu\text{s}$
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	$\mu\text{s}$
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	$\mu\text{s}$
Zero-scale error <sup>Notes 1, 2</sup>	E <sub>ZS</sub>	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 0.35$	%FSR
Full-scale error <sup>Notes 1, 2</sup>	E <sub>FS</sub>	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 0.35$	%FSR
Integral linearity error <sup>Note 1</sup>	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 3.5$	LSB
Differential linearity error <sup>Note 1</sup>	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		$\pm 2.0$	LSB
Analog input voltage	V <sub>AIN</sub>	ANI16 to ANI26	0		$AV_{REFP}$ and $EV_{DD0}$	V

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When  $AV_{REFP} < V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 1.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Zero-scale error/Full-scale error: Add  $\pm 0.05\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Integral linearity error/ Differential linearity error: Add  $\pm 0.5$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

4. When  $AV_{REFP} < EV_{DD0} \leq V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 4.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Zero-scale error/Full-scale error: Add  $\pm 0.20\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .

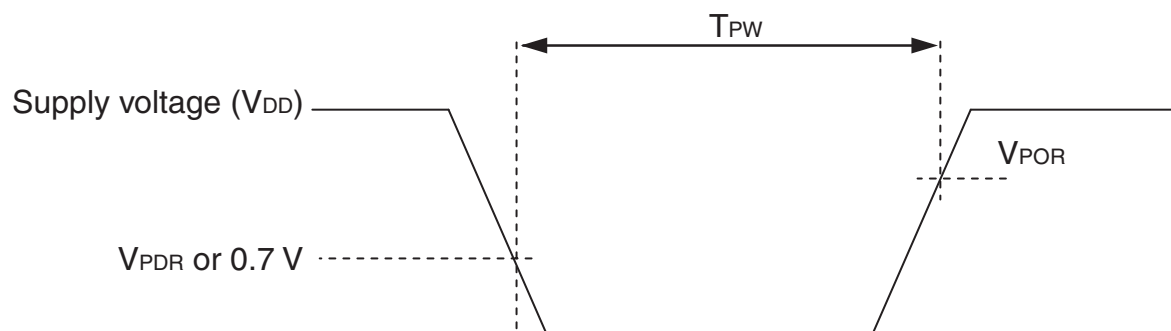
Integral linearity error/ Differential linearity error: Add  $\pm 2.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

## 3.6.3 POR circuit characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	$T_{PW}$		300			$\mu\text{s}$

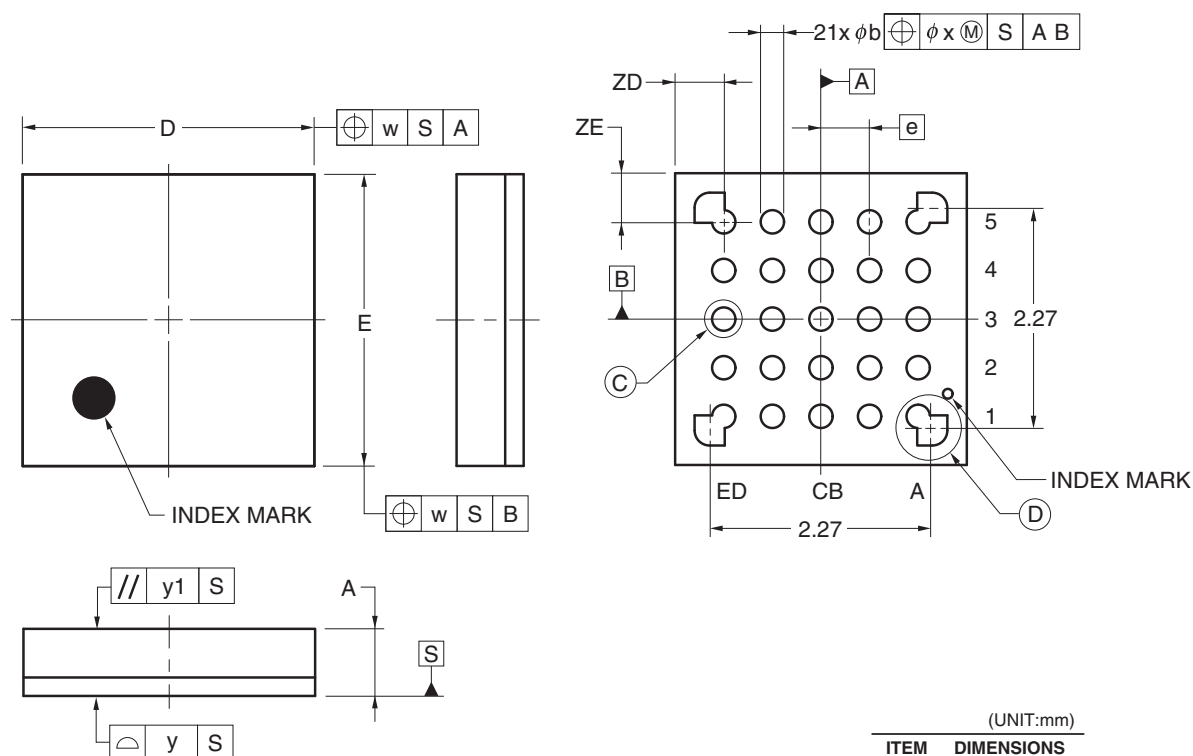
**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



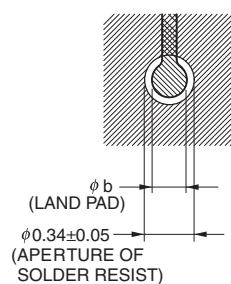
### 4.3 25-pin Products

R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA  
R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA  
R5F1008AGLA, R5F1008CGLA, R5F1008DGLA, R5F1008EGLA

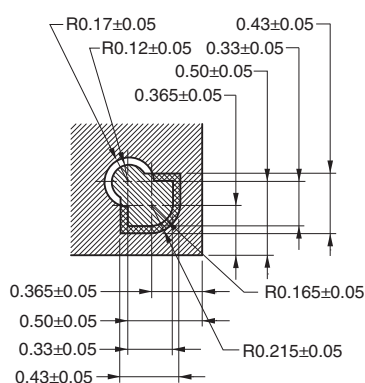
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWL0025KA-A	P25FC-50-2N2-2	0.01



### DETAIL OF © PART



DETAIL OF (D) PART



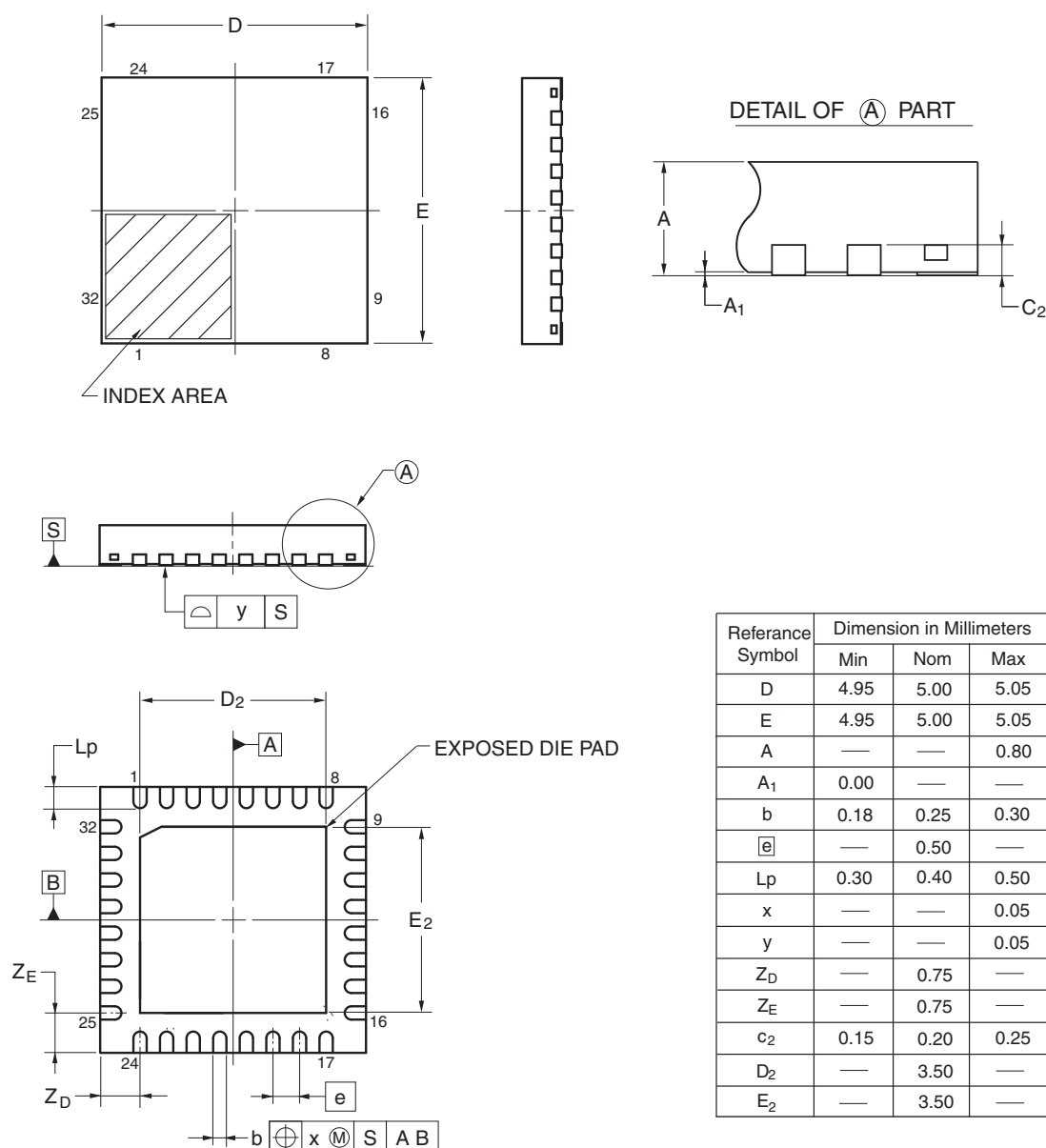
(UNIT:mm)	
ITEM	DIMENSIONS
D	3.00 ±0.10
E	3.00 ±0.10
w	0.20
e	0.50
A	0.69 ±0.07
b	0.24 ±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

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## 4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA  
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA  
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA  
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA  
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

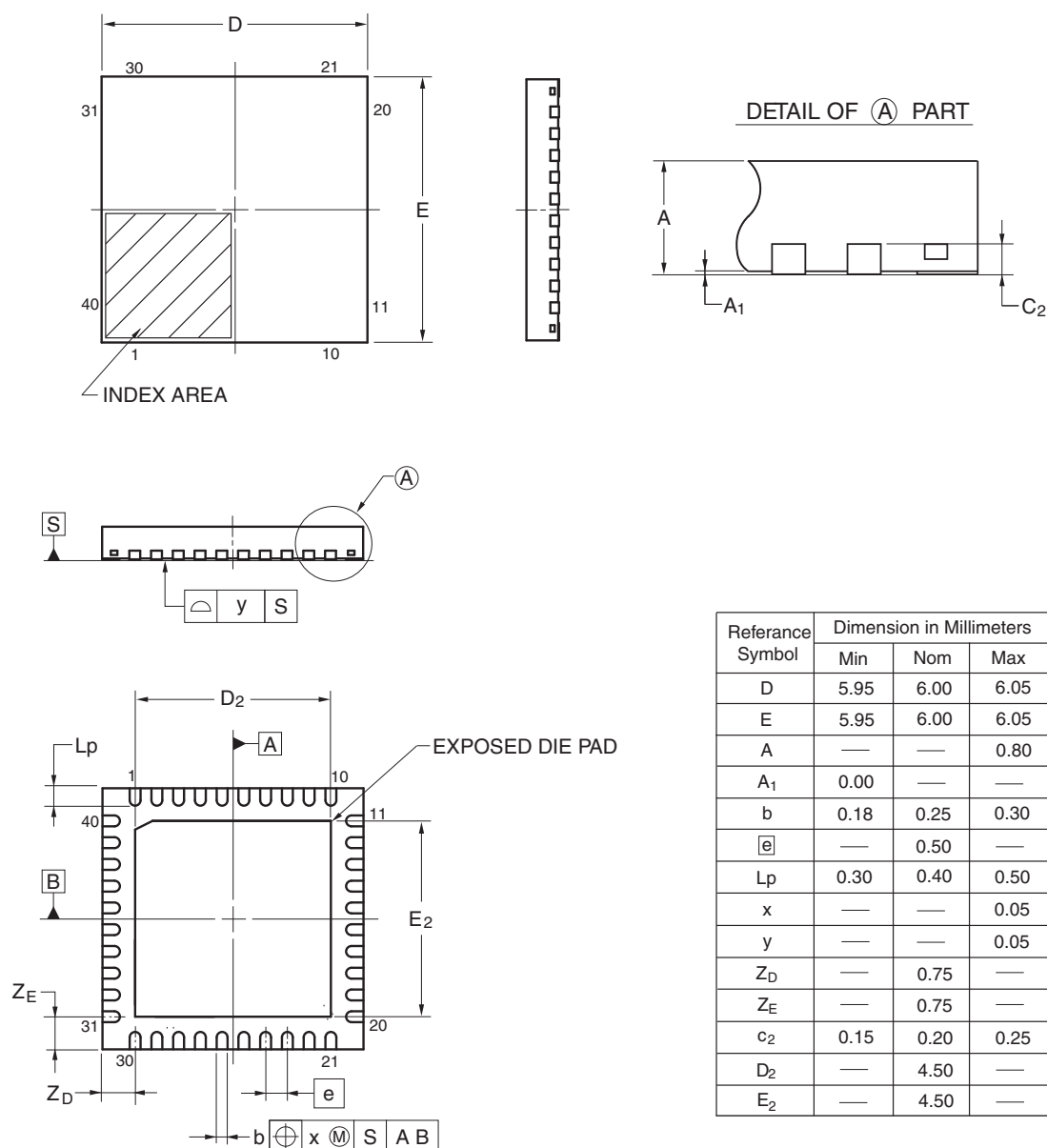


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## 4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA  
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA  
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,  
 R5F100EHDNA  
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,  
 R5F101EHDNA  
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,  
 R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09



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