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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

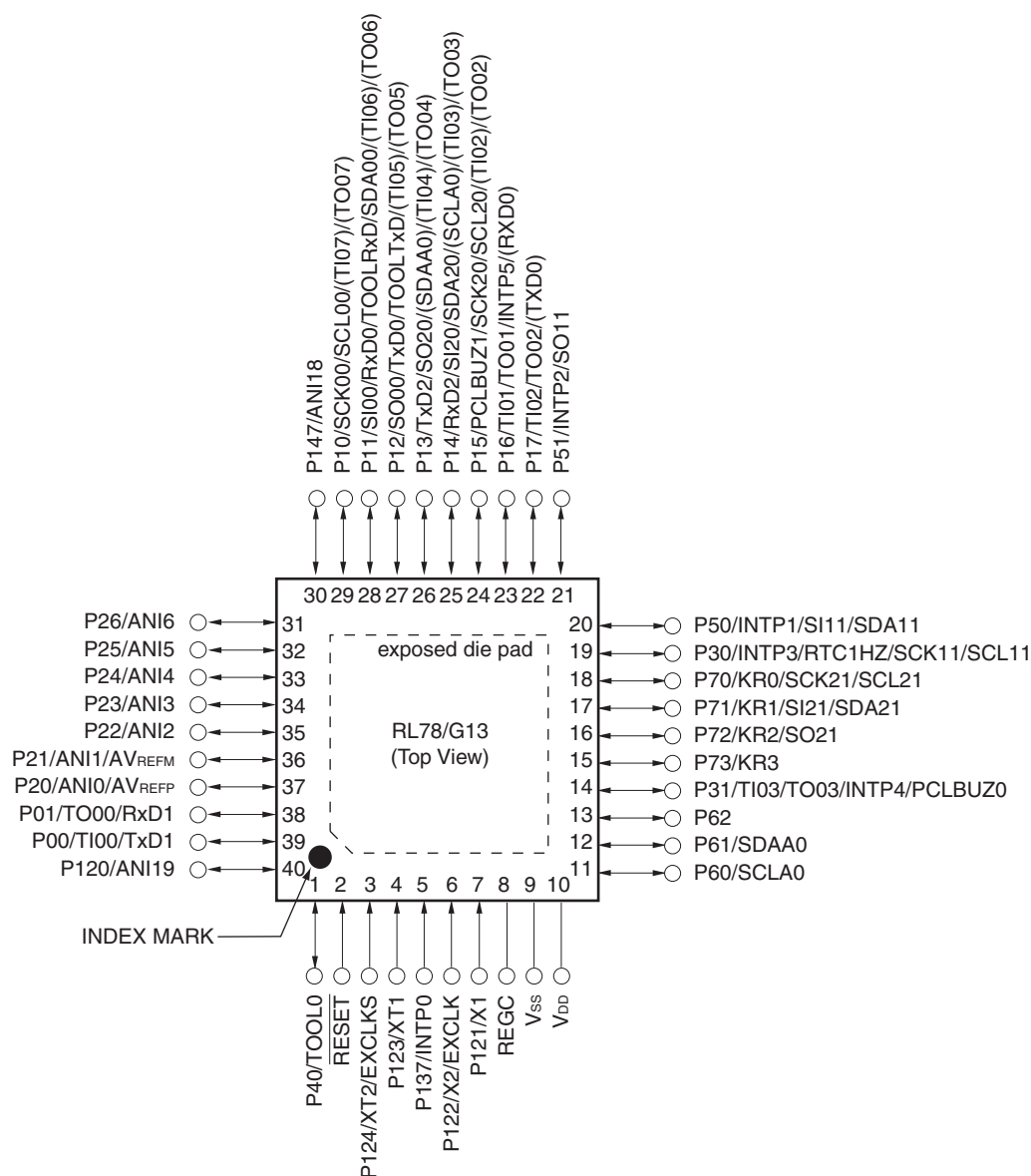
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mfgfb-x0

1.3.7 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



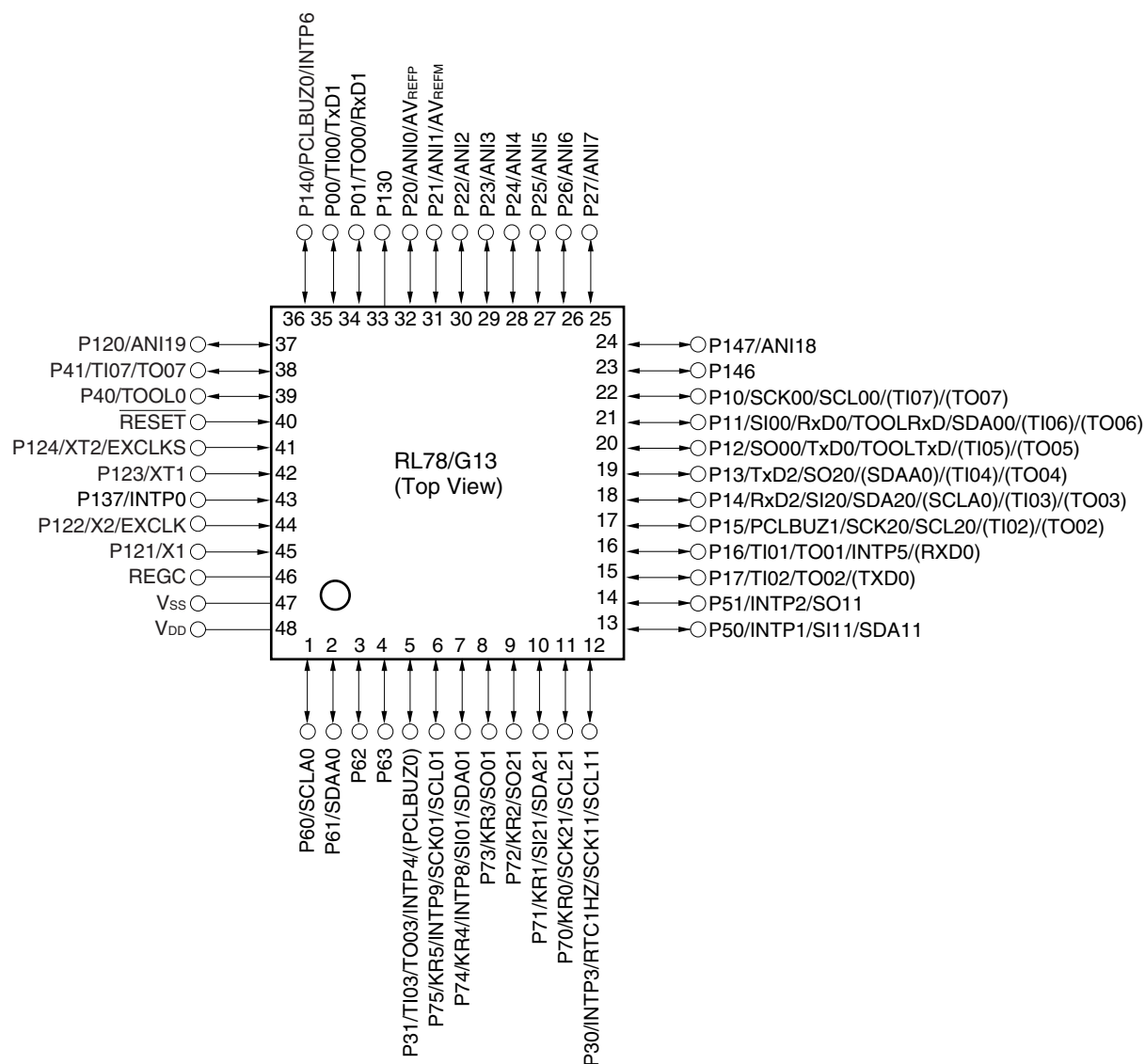
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
- It is recommended to connect an exposed die pad to Vss.

1.3.9 48-pin products

- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



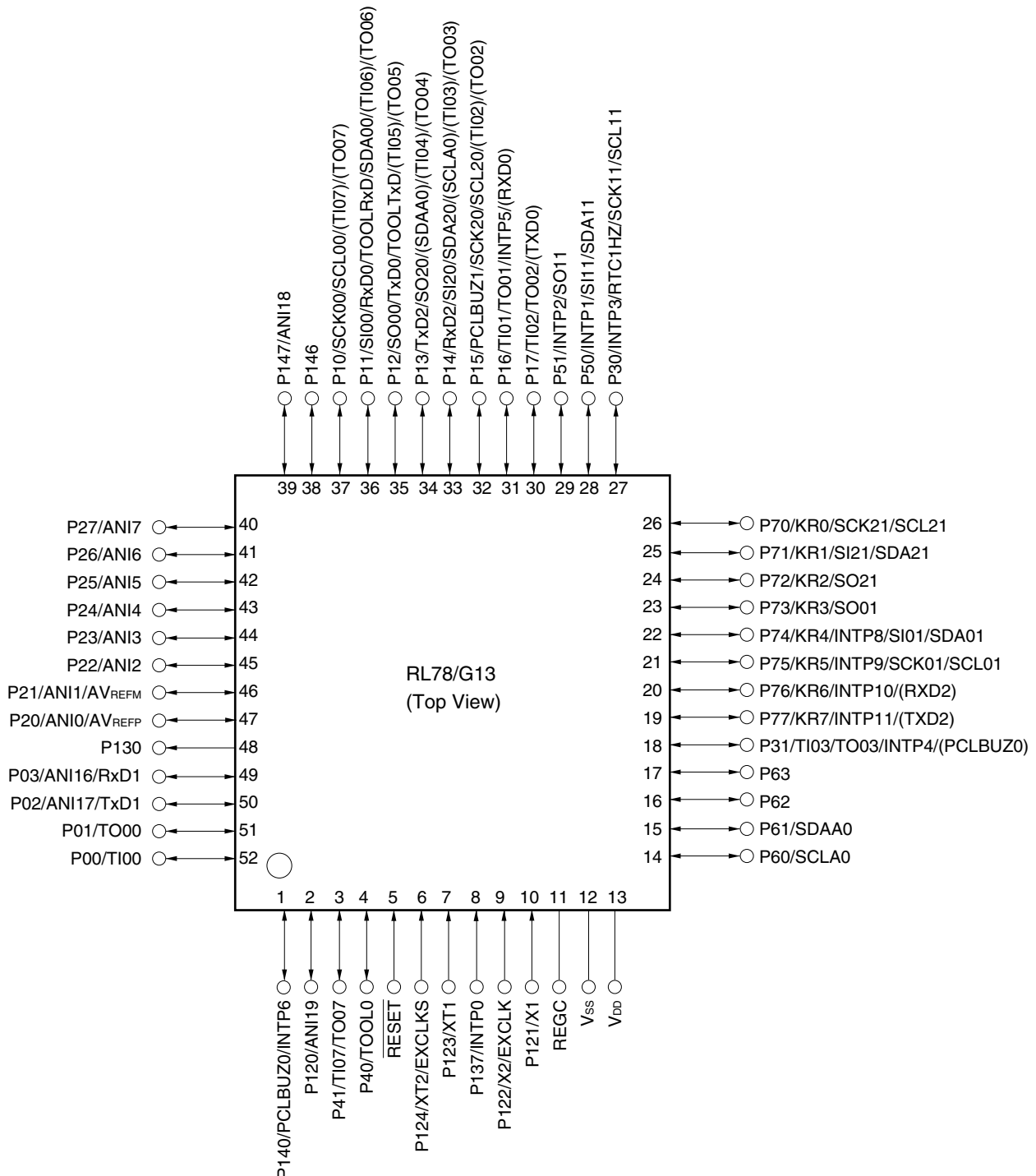
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



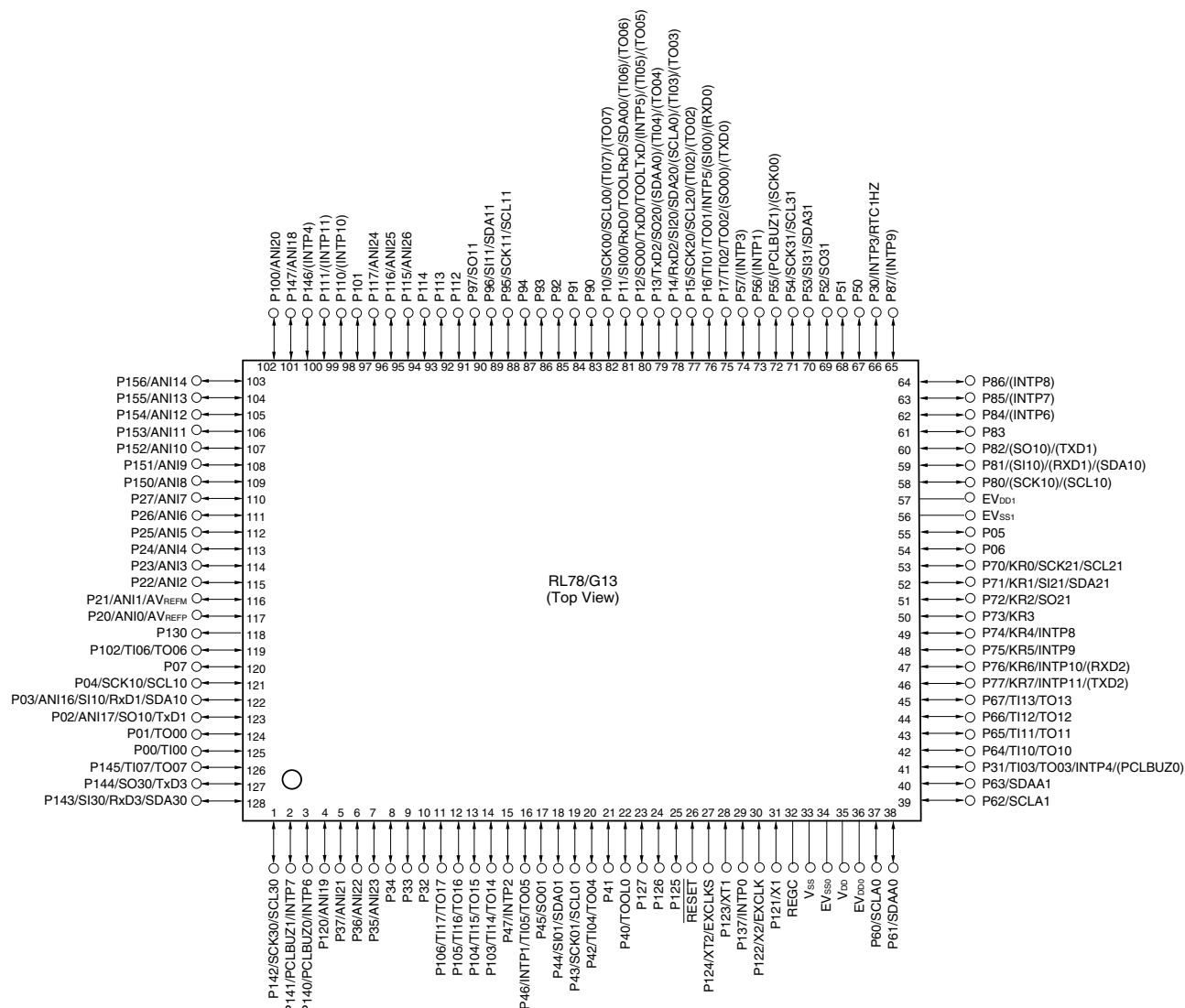
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.14 128-pin products

- 128-pin plastic LQFP (14 × 20 mm, 0.5 mm pitch)



Cautions 1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).

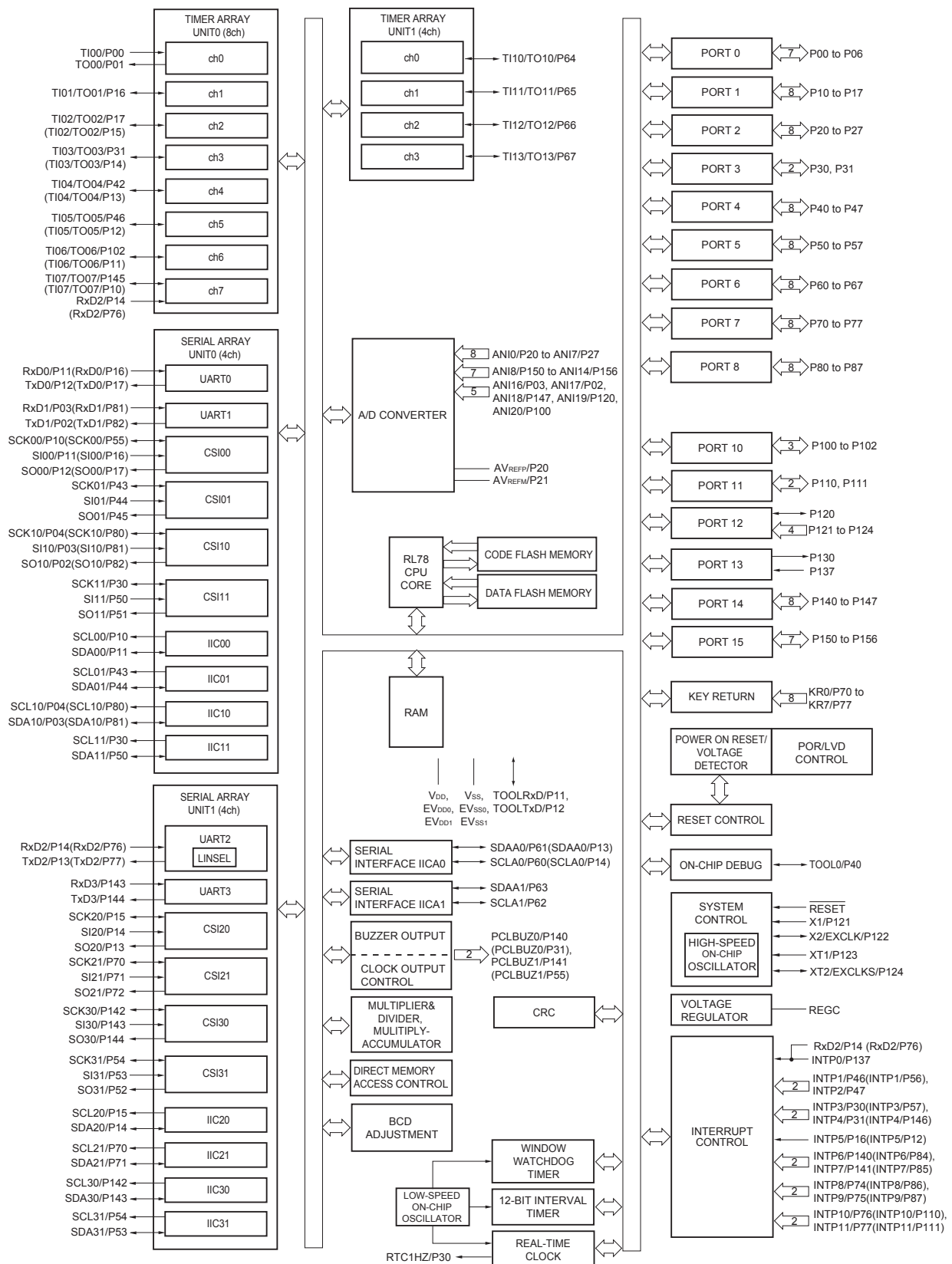
3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.13 100-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
- When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Lx	R5F101Lx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel - CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
		I ² C bus	1 channel		1 channel		1 channel		1 channel		1 channel
Multiplier and divider/multiply-accumulator		16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		- Reset by RESET pin - Internal reset by watchdog timer - Internal reset by power-on-reset - Internal reset by voltage detector - Internal reset by illegal instruction execution ^{Note} - Internal reset by RAM parity error - Internal reset by illegal-memory access									
Power-on-reset circuit		- Power-on-reset: 1.51 V (TYP.) - Power-down-reset: 1.50 V (TYP.)									
Voltage detector		- Rising edge : 1.67 V to 4.06 V (14 stages) - Falling edge : 1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)									
Operating ambient temperature		T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)									

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

<R>

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

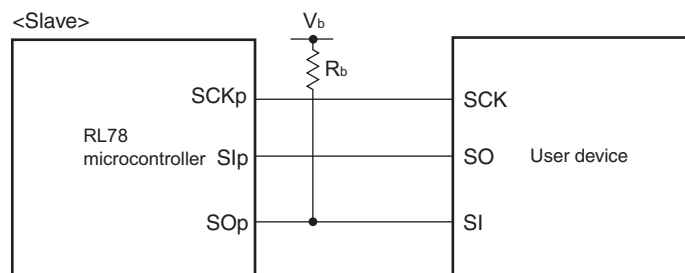
(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +20		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +30		1/f _{MCK} +30		1/f _{MCK} +30		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +40		1/f _{MCK} +40		1/f _{MCK} +40		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +40		1/f _{MCK} +40		ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{KSI2}	1.8 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +31		1/f _{MCK} +31		1/f _{MCK} +31		ns
		1.7 V ≤ EV _{DD0} ≤ 5.5 V		1/f _{MCK} +250		1/f _{MCK} +250		1/f _{MCK} +250		ns
		1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		1/f _{MCK} +250		1/f _{MCK} +250		ns
Delay time from SCKp↓ to SOp output ^{Note 3}	t _{KSO2}	C = 30 pF ^{Note 4}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +44		2/f _{MCK} +110		2/f _{MCK} +110	ns
			2.4 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +75		2/f _{MCK} +110		2/f _{MCK} +110	ns
			1.8 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +110		2/f _{MCK} +110		2/f _{MCK} +110	ns
			1.7 V ≤ EV _{DD0} ≤ 5.5 V		2/f _{MCK} +220		2/f _{MCK} +220		2/f _{MCK} +220	ns
			1.6 V ≤ EV _{DD0} ≤ 5.5 V		—		2/f _{MCK} +220		2/f _{MCK} +220	ns

- Notes**
1. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp setup time becomes “to SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 2. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The Slp hold time becomes “from SCKp↓” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 3. When DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1. The delay time to SOp output becomes “from SCKp↑” when DAP_{mn} = 0 and CKP_{mn} = 1, or DAP_{mn} = 1 and CKP_{mn} = 0.
 4. C is the load capacitance of the SOp output lines.
 5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		300 Note 1		300 ote 1	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		ns

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI14	Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI26	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T_A = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V	1.2	±3.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}	1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57	95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±2.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution AV _{REFP} = V _{DD} ^{Note 3}	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±1.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V ^{Note 4}		±2.0	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI14	0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 5}			V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 5}			V

(Notes are listed on the next page.)

2.6.5 Power supply voltage rising slope characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

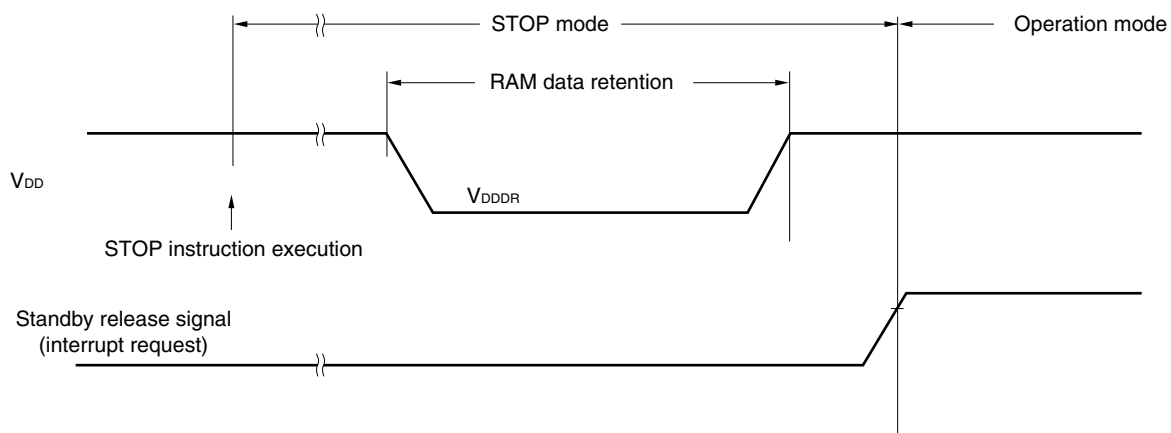
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C	100,000			
		Retained for 20 years T _A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

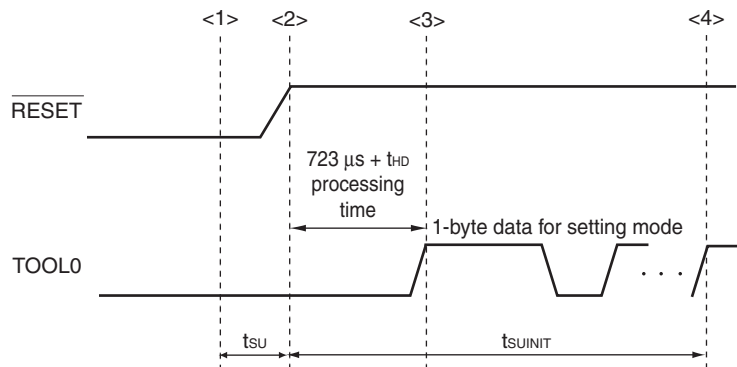
(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t _{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t _{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t _{HD}	POR and LVD reset must be released before the external reset is released.	1			ms

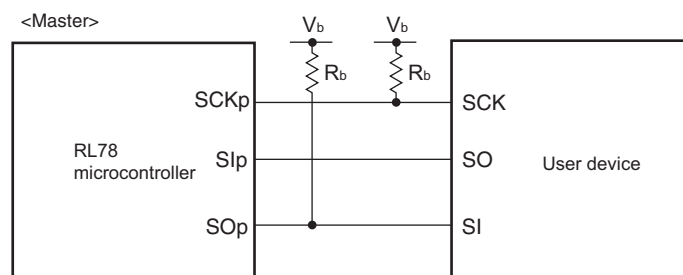


- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

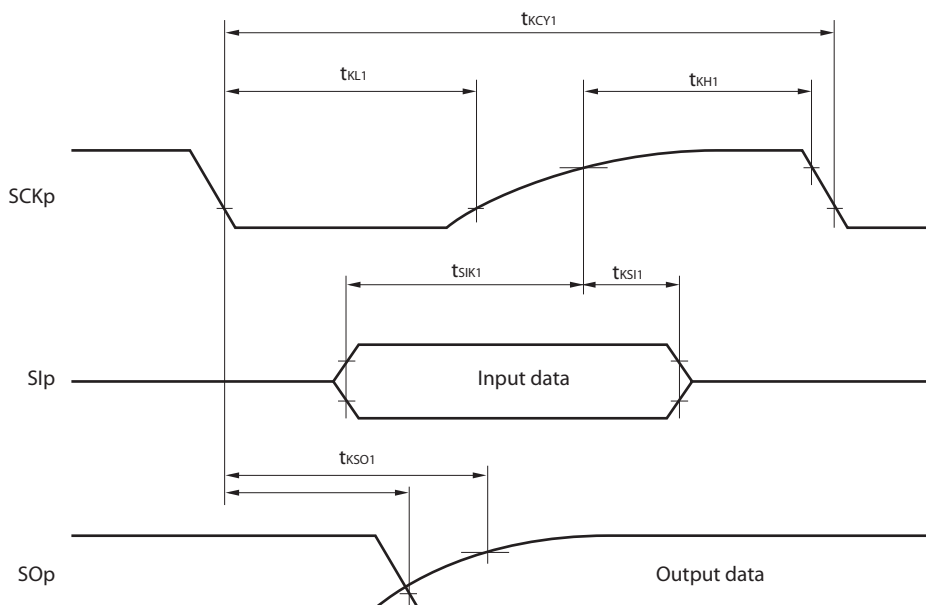
t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

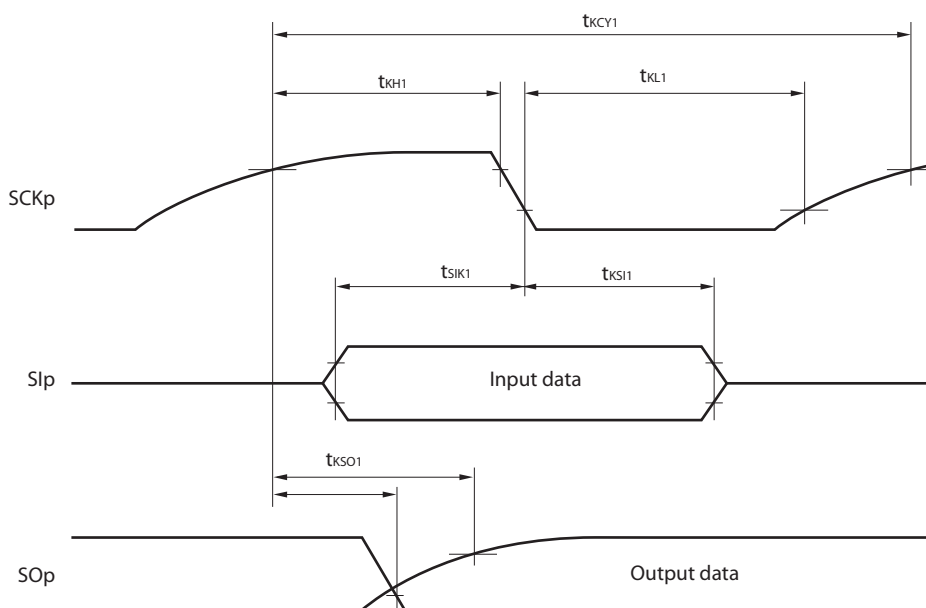
CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$28/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$20/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$40/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$28/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$96/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$72/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$64/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$52/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$20/f_{\text{MCK}}$		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		t _{KCY2} /2 – 24		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		t _{KCY2} /2 – 36		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ ^{Note 2}		t _{KCY2} /2 – 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}			$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 240$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			$2/f_{\text{MCK}} + 428$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			$2/f_{\text{MCK}} + 1146$	ns

(Notes, Caution and Remarks are listed on the next page.)

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}/ANI1$ (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} ^{Note 3}, Reference voltage (–) = AV_{REFM} ^{Note 4} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Analog input voltage	V_{AIN}			0		V_{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (–) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (–) = AV_{REFM} .

3.6.2 Temperature sensor/internal reference voltage characteristics

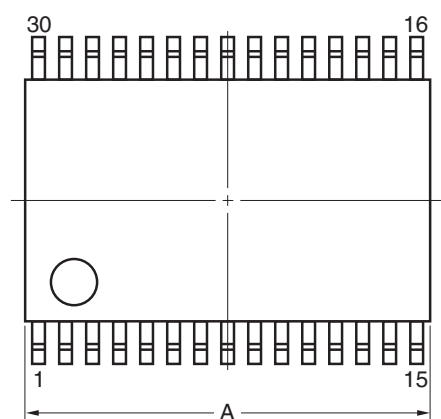
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	V_{BGR}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	t_{AMP}		5			μs

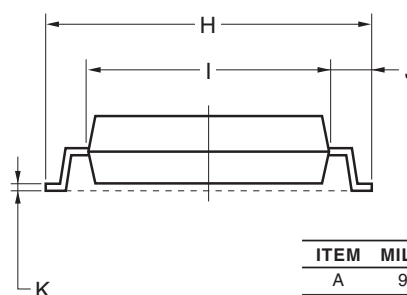
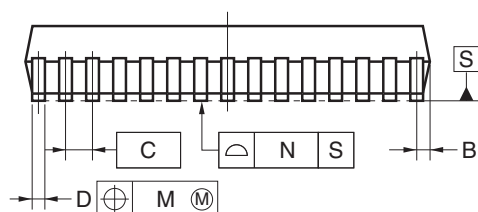
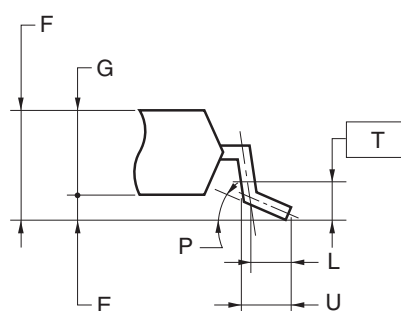
4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end

**NOTE**

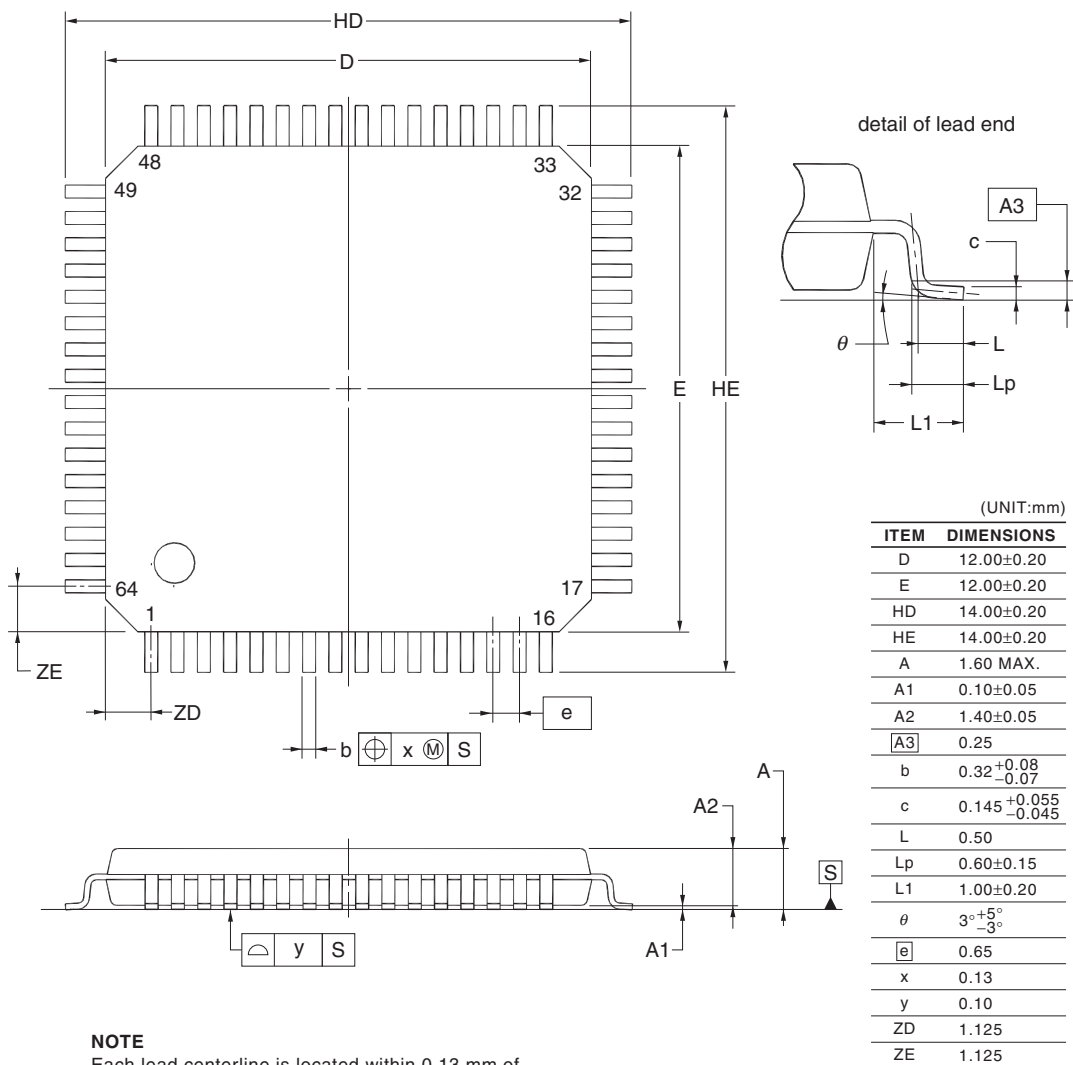
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

4.11 64-pin Products

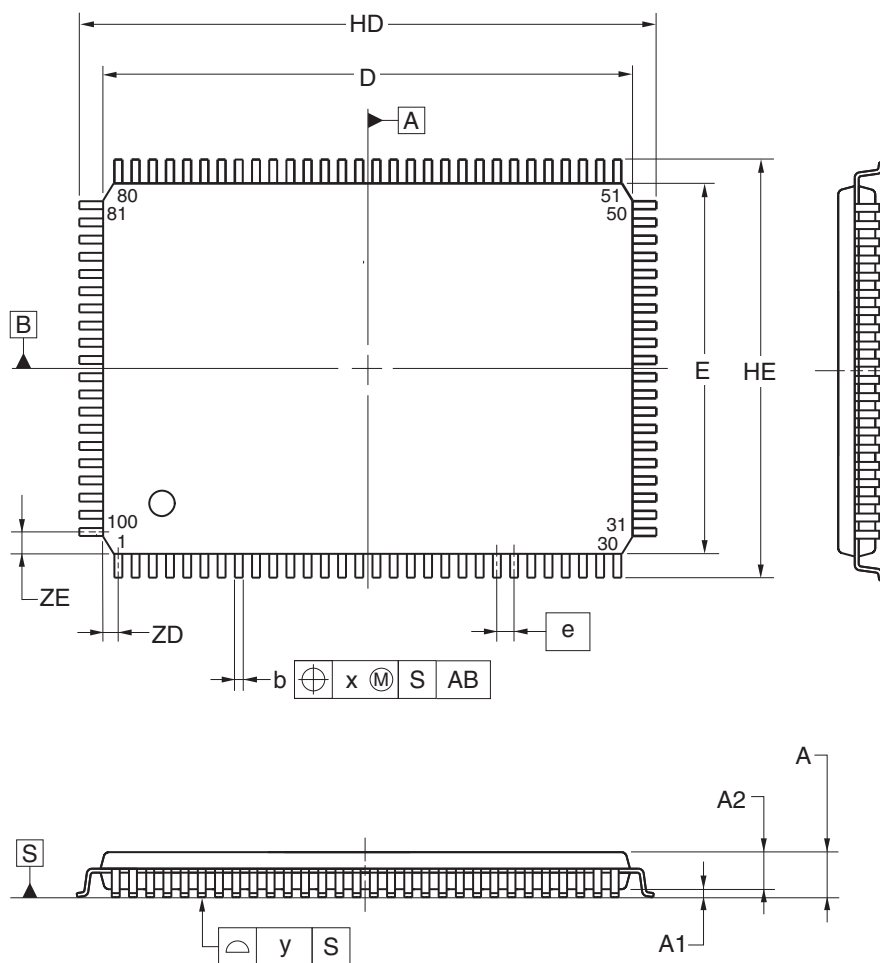
R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAF, A,
 R5F100LKAFA, R5F100LLAFA
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAF, A,
 R5F101LKAFA, R5F101LLAFA
 R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LHDFA, R5F100LJDFA,
 R5F100LK DFA, R5F100LLDFA
 R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LHDFA, R5F101LJDFA,
 R5F101LK DFA, R5F101LLDFA
 R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,
 R5F100LJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

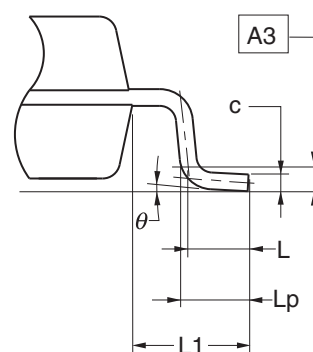


R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJFAFA, R5F100PKAFA, R5F100PLAFA
 R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJFAFA, R5F101PKAFA, R5F101PLAFA
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA
 R5F100PFGFA, R5F100PGGFA, R5F100PHGFA, R5F100PJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.32 ^{+0.08} _{-0.07}
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825