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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	64
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LFQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mhdfb-30">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100mhdfb-30</a>

Table 1-1. List of Ordering Part Numbers

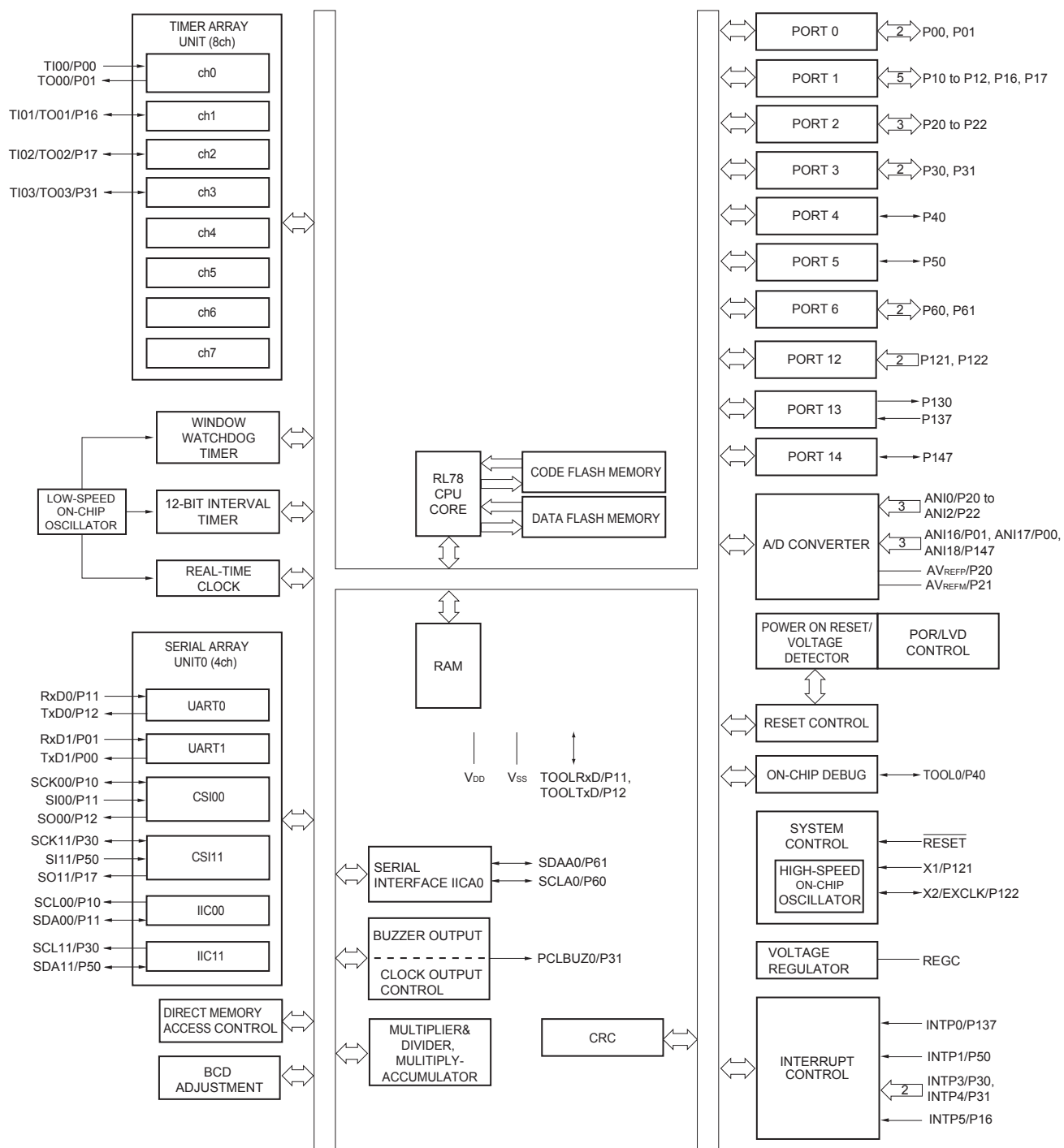
(10/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGFAFA#V0, R5F100MHAFA#V0, R5F100MJFAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGFAFA#X0, R5F100MHAFA#X0, R5F100MJFAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0
			D	R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0
			G	R5F100MFGFA#V0, R5F100MGGFA#V0, R5F100MHGFA#V0, R5F100MJGFA#V0 R5F100MFGFA#X0, R5F100MGGFA#X0, R5F100MHGFA#X0, R5F100MJGFA#X0
		Not mounted	A	R5F101MFAFA#V0, R5F101MGFAFA#V0, R5F101MHAFA#V0, R5F101MJFAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGFAFA#X0, R5F101MHAFA#X0, R5F101MJFAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0
			D	R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0
			G	R5F101MFGFA#V0, R5F101MGGFA#V0, R5F101MHGFA#V0, R5F101MJGFA#V0 R5F101MFGFA#X0, R5F101MGGFA#X0, R5F101MHGFA#X0, R5F101MJGFA#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0
			D	R5F100MFDDB#V0, R5F100MGDFB#V0, R5F100MHDDB#V0, R5F100MJDFB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDDB#X0, R5F100MGDFB#X0, R5F100MHDDB#X0, R5F100MJDFB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0
			G	R5F100MFGFB#V0, R5F100MGGFB#V0, R5F100MHGFB#V0, R5F100MJGFB#V0 R5F100MFGFB#X0, R5F100MGGFB#X0, R5F100MHGFB#X0, R5F100MJGFB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0
			D	R5F101MFDDB#V0, R5F101MGDFB#V0, R5F101MHDDB#V0, R5F101MJDFB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDDB#X0, R5F101MGDFB#X0, R5F101MHDDB#X0, R5F101MJDFB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0
			G	R5F101MFGFB#V0, R5F101MGGFB#V0, R5F101MHGFB#V0, R5F101MJGFB#V0 R5F101MFGFB#X0, R5F101MGGFB#X0, R5F101MHGFB#X0, R5F101MJGFB#X0

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution** The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

## 1.5.3 25-pin products



## 2. ELECTRICAL SPECIFICATIONS ( $T_A = -40$ to $+85^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products A: Consumer applications  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxAxx, R5F101xxAxx

D: Industrial applications  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxDxx, R5F101xxDxx

G: Industrial applications when  $T_A = -40$  to  $+105^\circ\text{C}$  products is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$

R5F100xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $EV_{DD0}$ ,  $EV_{DD1}$ ,  $EV_{SS0}$ , or  $EV_{SS1}$  pin, replace  $EV_{DD0}$  and  $EV_{DD1}$  with  $V_{DD}$ , or replace  $EV_{SS0}$  and  $EV_{SS1}$  with  $V_{SS}$ .
  3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.

- Notes**
1. Total current flowing into  $V_{DD}$  and  $EV_{DD0}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$  or  $V_{SS}$ ,  $EV_{SS0}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

- Notes**
1. Total current flowing into V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, including the input leakage current flowing when the level of the input pin is fixed to V<sub>DD</sub>, EV<sub>DD0</sub>, and EV<sub>DD1</sub>, or V<sub>SS</sub>, EV<sub>SS0</sub>, and EV<sub>SS1</sub>. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz
    - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz

- Remarks**
1. f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
  3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**Note** The following conditions are required for low voltage interface when  $E_{VDD0} < V_{DD}$

$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$  : MIN. 125 ns

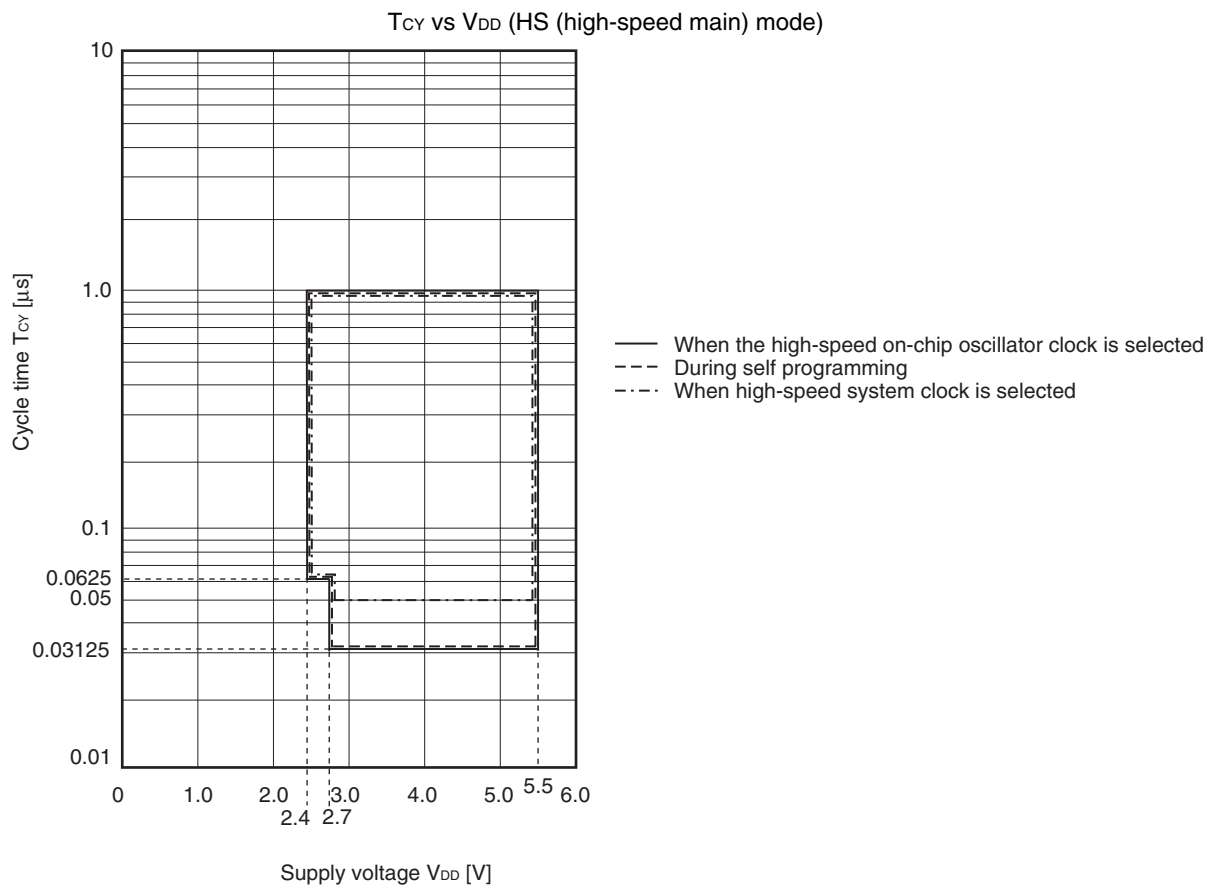
$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$  : MIN. 250 ns

**Remark**  $f_{MCK}$ : Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number ( $m = 0, 1$ ), n: Channel number ( $n = 0$  to  $7$ ))

#### Minimum Instruction Execution Time during Main System Clock Operation





## (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T<sub>A</sub> = -40 to +85°C, 2.7 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	200		1150		1150		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t <sub>KH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 120		t <sub>KCY1</sub> /2 – 120		t <sub>KCY1</sub> /2 – 120		ns
SCKp low-level width	t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 7		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 10		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	121		479		479		ns
Slp hold time (from SCKp↑) <sup>Note 1</sup>	t <sub>SH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOp output <sup>Note 1</sup>	t <sub>KSO1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 20 pF, R <sub>b</sub> = 2.7 kΩ		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**  
**(3/3)**

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) <sup>Note 1</sup>	t <sub>SIK1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) <sup>Note 1</sup>	t <sub>KSH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output <sup>Note 1</sup>	t <sub>KSO1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ		25		25		25	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

## (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time <sup>Note 1</sup>	t <sub>KCY2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	24 MHz < f <sub>MCK</sub>	14/ f <sub>MCK</sub>		—		—		ns
			20 MHz < f <sub>MCK</sub> ≤ 24 MHz	12/ f <sub>MCK</sub>		—		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 20 MHz	10/ f <sub>MCK</sub>		—		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	8/f <sub>MCK</sub>		16/ f <sub>MCK</sub>		—		ns
			f <sub>MCK</sub> ≤ 4 MHz	6/f <sub>MCK</sub>		10/ f <sub>MCK</sub>		10/ f <sub>MCK</sub>		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	24 MHz < f <sub>MCK</sub>	20/ f <sub>MCK</sub>		—		—		ns
			20 MHz < f <sub>MCK</sub> ≤ 24 MHz	16/ f <sub>MCK</sub>		—		—		ns
			16 MHz < f <sub>MCK</sub> ≤ 20 MHz	14/ f <sub>MCK</sub>		—		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 16 MHz	12/ f <sub>MCK</sub>		—		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	8/f <sub>MCK</sub>		16/ f <sub>MCK</sub>		—		ns
			f <sub>MCK</sub> ≤ 4 MHz	6/f <sub>MCK</sub>		10/ f <sub>MCK</sub>		10/ f <sub>MCK</sub>		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	24 MHz < f <sub>MCK</sub>	48/ f <sub>MCK</sub>		—		—		ns
			20 MHz < f <sub>MCK</sub> ≤ 24 MHz	36/ f <sub>MCK</sub>		—		—		ns
			16 MHz < f <sub>MCK</sub> ≤ 20 MHz	32/ f <sub>MCK</sub>		—		—		ns
			8 MHz < f <sub>MCK</sub> ≤ 16 MHz	26/ f <sub>MCK</sub>		—		—		ns
			4 MHz < f <sub>MCK</sub> ≤ 8 MHz	16/ f <sub>MCK</sub>		16/ f <sub>MCK</sub>		—		ns
			f <sub>MCK</sub> ≤ 4 MHz	10/ f <sub>MCK</sub>		10/ f <sub>MCK</sub>		10/ f <sub>MCK</sub>		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

**(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	t <sub>KCY2</sub> /2 - 12		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	t <sub>KCY2</sub> /2 - 18		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		t <sub>KCY2</sub> /2 - 50		ns
Slp setup time (to SCKp↑) <sup>Note 3</sup>	t <sub>SIK2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V	1/f <sub>MCK</sub> + 20		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup>	1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		1/f <sub>MCK</sub> + 30		ns
Slp hold time (from SCKp↑) <sup>Note 4</sup>	t <sub>KS12</sub>		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		1/f <sub>MCK</sub> + 31		ns
Delay time from SCKp↓ to SOp output <sup>Note 5</sup>	t <sub>KSO2</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ		2/f <sub>MCK</sub> + 120		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ		2/f <sub>MCK</sub> + 214		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573		2/f <sub>MCK</sub> + 573	ns

**Notes** 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t <sub>SU:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
Data hold time (transmission)	t <sub>HD:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	ns

**Notes** 1. The value must also be equal to or less than f<sub>MCK</sub>/4.2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.3. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

### 3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$ )

This chapter describes the following electrical specifications.

Target products G: Industrial applications  $T_A = -40$  to  $+105^\circ\text{C}$   
R5F100xxGxx

- Cautions**
1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
  2. With products not provided with an  $\text{EV}_{\text{DD0}}$ ,  $\text{EV}_{\text{DD1}}$ ,  $\text{EV}_{\text{SS0}}$ , or  $\text{EV}_{\text{SS1}}$  pin, replace  $\text{EV}_{\text{DD0}}$  and  $\text{EV}_{\text{DD1}}$  with  $\text{V}_{\text{DD}}$ , or replace  $\text{EV}_{\text{SS0}}$  and  $\text{EV}_{\text{SS1}}$  with  $\text{V}_{\text{SS}}$ .
  3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.
  4. Please contact Renesas Electronics sales office for derating of operation under  $T_A = +85^\circ\text{C}$  to  $+105^\circ\text{C}$ . Derating is the systematic reduction of load for the sake of improved reliability.

**Remark** When RL78/G13 is used in the range of  $T_A = -40$  to  $+85^\circ\text{C}$ , see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ( $T_A = -40$  to  $+85^\circ\text{C}$ )**.

There are following differences between the products "G: Industrial applications ( $T_A = -40$  to  $+105^\circ\text{C}$ )" and the products "A: Consumer applications, and D: Industrial applications".

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$	$T_A = -40$ to $+105^\circ\text{C}$
Operating mode Operating voltage range	HS (high-speed main) mode: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$ LS (low-speed main) mode: $1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }8\text{ MHz}$ LV (low-voltage main) mode: $1.6\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }4\text{ MHz}$	HS (high-speed main) mode only: $2.7\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$ $2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
High-speed on-chip oscillator clock accuracy	$1.8\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to $-20^\circ\text{C}$ $1.6\text{ V} \leq V_{\text{DD}} < 1.8\text{ V}$ $\pm 5.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 5.5\% @ T_A = -40$ to $-20^\circ\text{C}$	$2.4\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ $\pm 2.0\% @ T_A = +85$ to $+105^\circ\text{C}$ $\pm 1.0\% @ T_A = -20$ to $+85^\circ\text{C}$ $\pm 1.5\% @ T_A = -40$ to $-20^\circ\text{C}$
Serial array unit	UART CSI: $f_{\text{CLK}}/2$ (supporting 16 Mbps), $f_{\text{CLK}}/4$ Simplified I <sup>2</sup> C communication	UART CSI: $f_{\text{CLK}}/4$ Simplified I <sup>2</sup> C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(Remark is listed on the next page.)

## 3.3 DC Characteristics

## 3.3.1 Pin characteristics

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ ) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-3.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-10.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty $\leq 70\%$ <sup>Note 3</sup> )	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-30.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$		-19.0	mA
			$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$		-10.0	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )	$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$		-60.0	mA
	I <sub>OH2</sub>	Per pin for P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty $\leq 70\%$ <sup>Note 3</sup> )	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$		-1.5	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>DD</sub> pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor  $\leq 70\%$ .

The output current value that has changed to the duty factor  $> 70\%$  the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins =  $(I_{\text{OH}} \times 0.7)/(n \times 0.01)$

<Example> Where  $n = 80\%$  and  $I_{\text{OH}} = -10.0\text{ mA}$

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7\text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**( $T_A = -40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (5/5)**

Items	Symbol	Conditions	MIN.		TYP.	MAX.	Unit	
Input leakage current, high	I <sub>LH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>DD0</sub>			1	μA	
	I <sub>LH2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>DD</sub>			1	μA	
	I <sub>LH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub>			−1	μA	
	I <sub>LIL2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>SS</sub>			−1	μA	
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>	In input port or external clock input		−1	μA	
				In resonator connection		−10	μA	
On-chip pll-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub> , In input port		10	20	100	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



**(4) During communication at same potential (simplified I<sup>2</sup>C mode)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	$f_{\text{SCL}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$		400 <sup>Note1</sup>	kHz
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$		100 <sup>Note1</sup>	
Hold time when SCLr = "L"	$t_{\text{LOW}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		ns
Hold time when SCLr = "H"	$t_{\text{HIGH}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	1200		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	4600		ns
Data setup time (reception)	$t_{\text{SU:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 220$ <sup>Note2</sup>		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	$1/f_{\text{MCK}} + 580$ <sup>Note2</sup>		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 50\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$ , $C_b = 100\text{ pF}$ , $R_b = 3\text{ k}\Omega$	0	1420	ns

**Notes** 1. The value must also be equal to or less than  $f_{\text{MCK}}/4$ .2. Set the  $f_{\text{MCK}}$  value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the normal input buffer and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

## (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T<sub>A</sub> = -40 to +105°C, 2.4 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V		
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 1.4 kΩ, V <sub>b</sub> = 2.7 V		
				<b>Note 1</b>	bps
				2.6 <sup>Note 2</sup>	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ, V <sub>b</sub> = 2.3 V		
					<b>Note 3</b>
					1.2 <sup>Note 4</sup>
					Mbps
			2.4 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V		
			Theoretical value of the maximum transfer rate C <sub>b</sub> = 50 pF, R <sub>b</sub> = 5.5 kΩ, V <sub>b</sub> = 1.6 V		
					<b>Note 5</b>
					0.43 <sup>Note 6</sup>
					Mbps

**Notes 1.** The smaller maximum transfer rate derived by using f<sub>MCK</sub>/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV<sub>DD0</sub> ≤ 5.5 V and 2.7 V ≤ V<sub>b</sub> ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using f<sub>MCK</sub>/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> < 4.0 V and 2.4 V ≤ V<sub>b</sub> ≤ 2.7 V

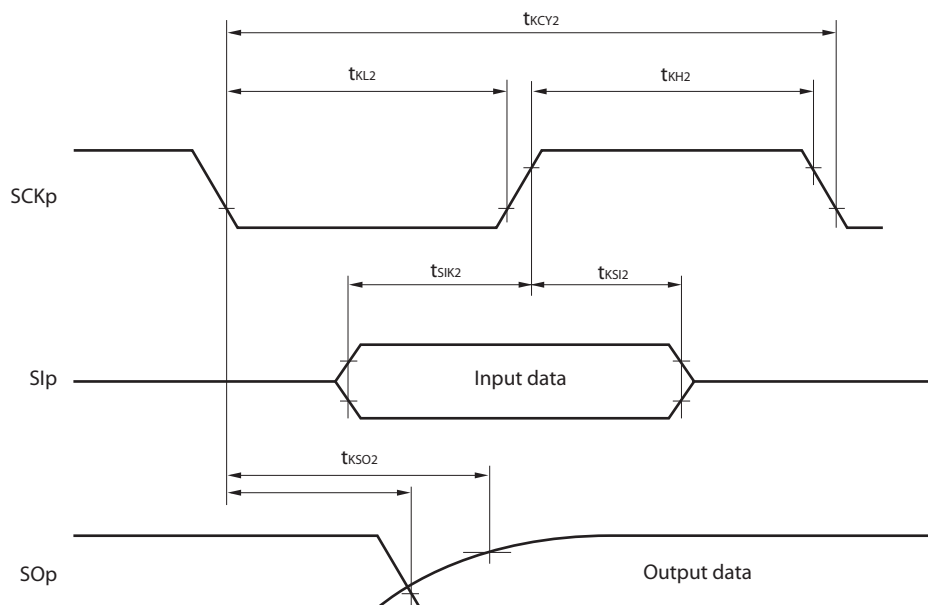
$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

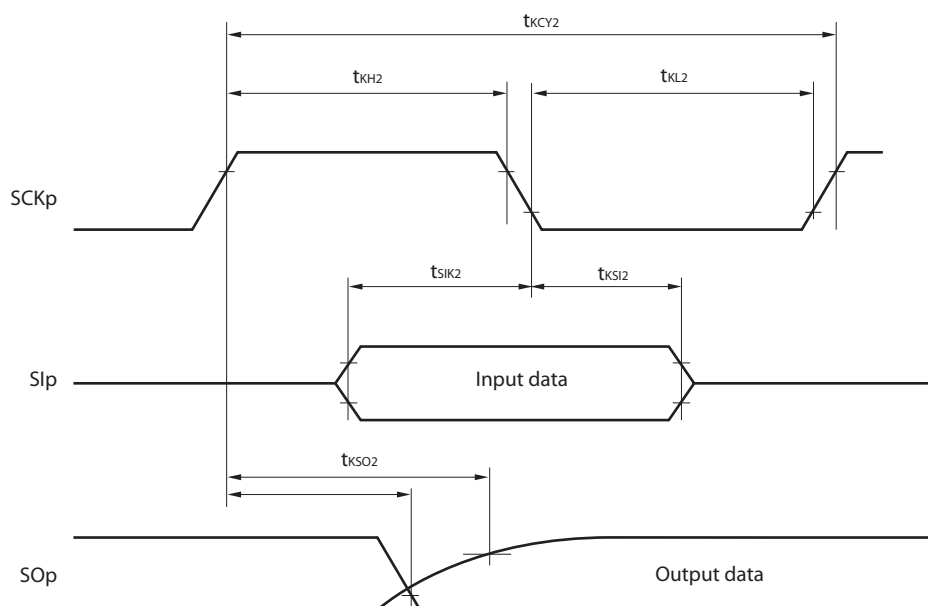
\* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)**  
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

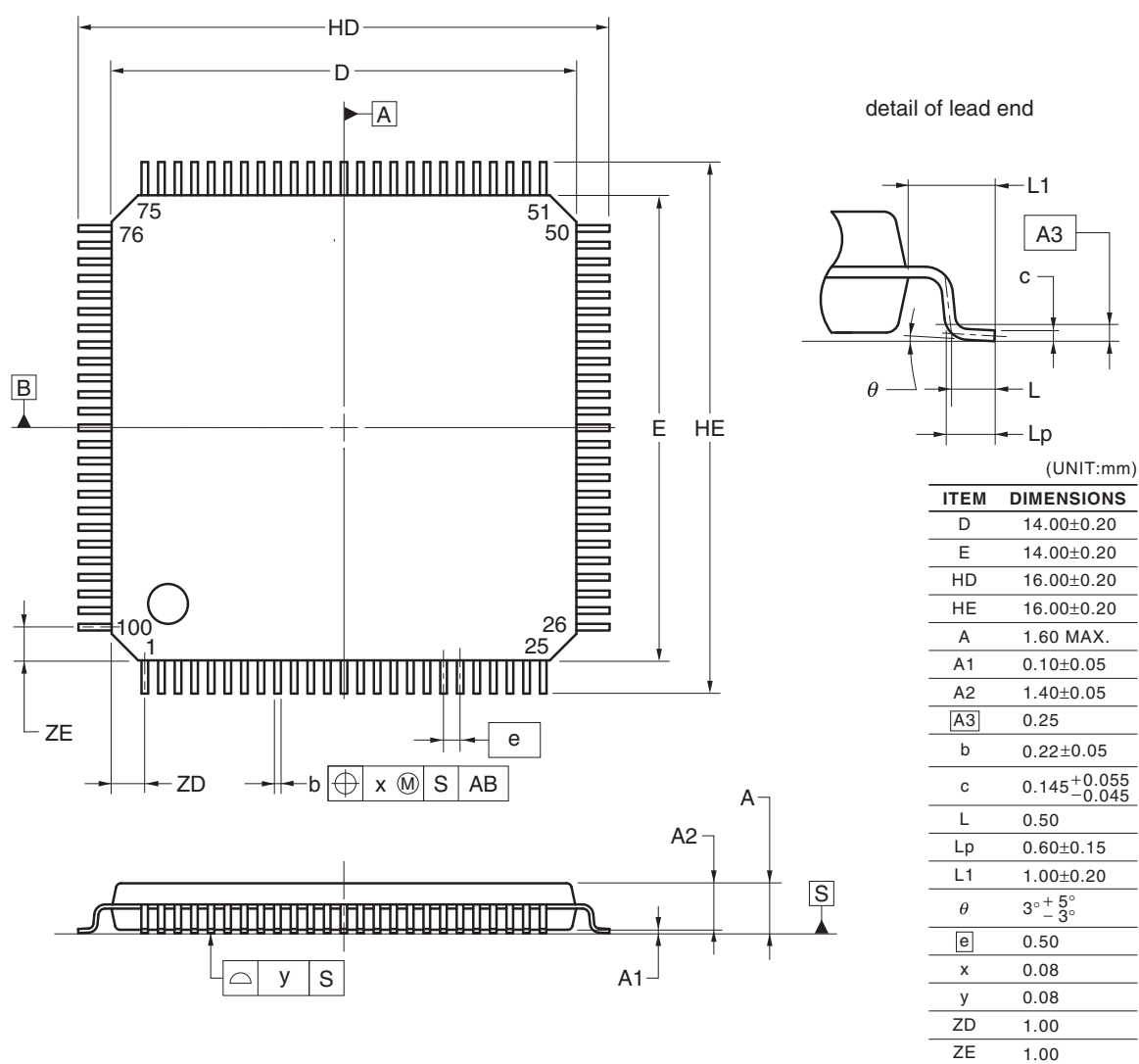


- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,  
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
 Use other CSI for communication at different potential.

## 4.13 100-pin Products

R5F100PFAFB, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB  
 R5F101PFAFB, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB  
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA  
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA  
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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