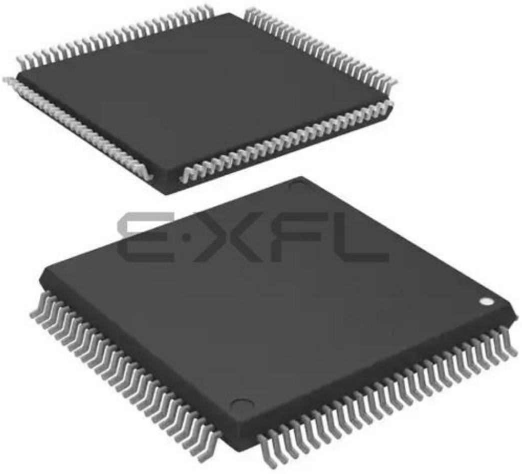


Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100pfdfb-50

Table 1-1. List of Ordering Part Numbers

(1/12)

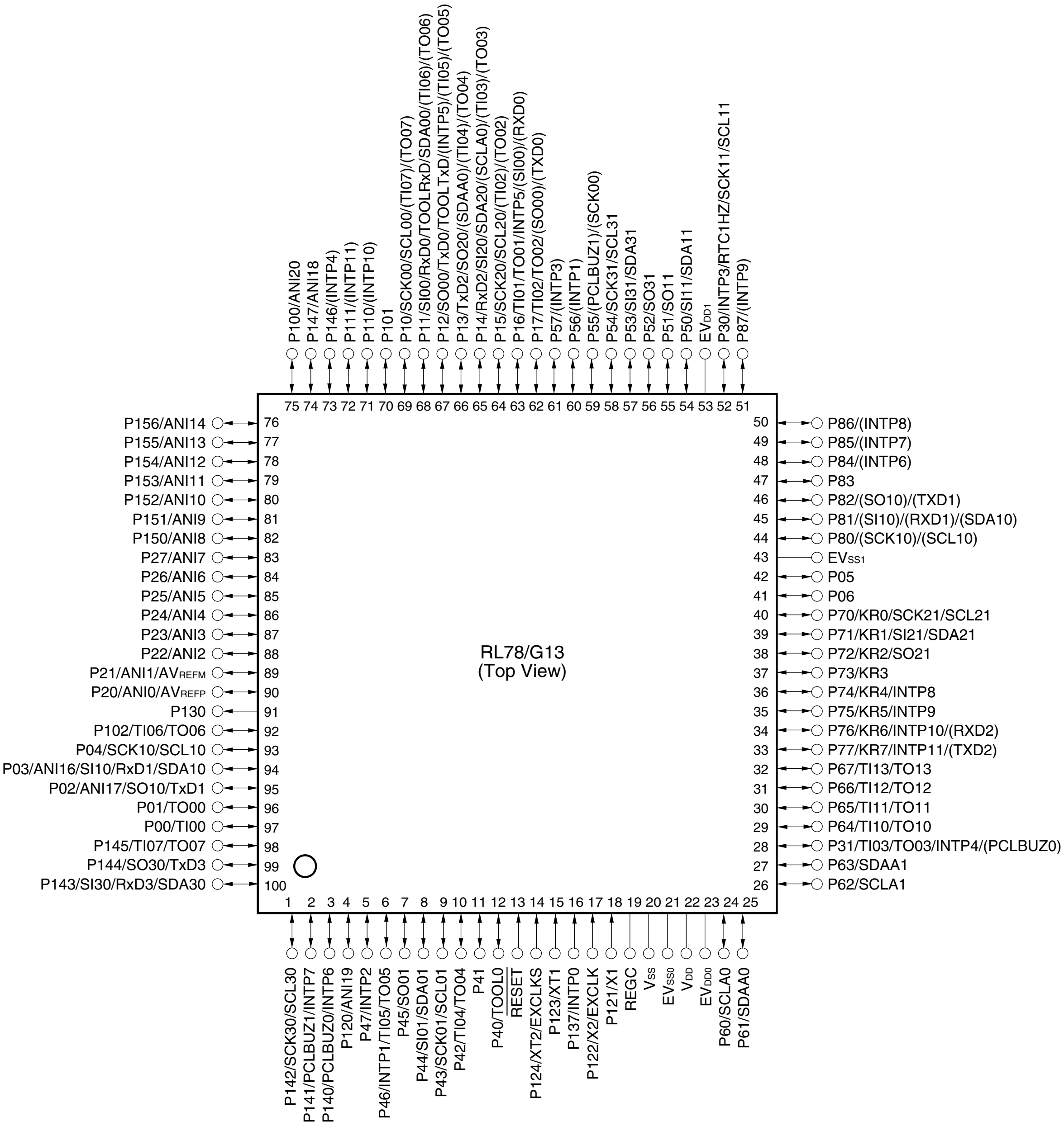
Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0 R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0 R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0 R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0
		Not mounted	A	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0 R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0 R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0
24 pins	24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch)	Mounted	A	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0 R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0 R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0 R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0
		Not mounted	A	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0 R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0 R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.13 100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)



Cautions 1. Make EV$_{SS0}$, EV$_{SS1}$ pins the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$, EV$_{DD1}$ pins (EV$_{DD0}$ = EV$_{DD1}$).

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$, EV$_{DD0}$ and EV$_{DD1}$ pins and connect the V$_{SS}$, EV$_{SS0}$ and EV$_{SS1}$ pins to separate ground lines.

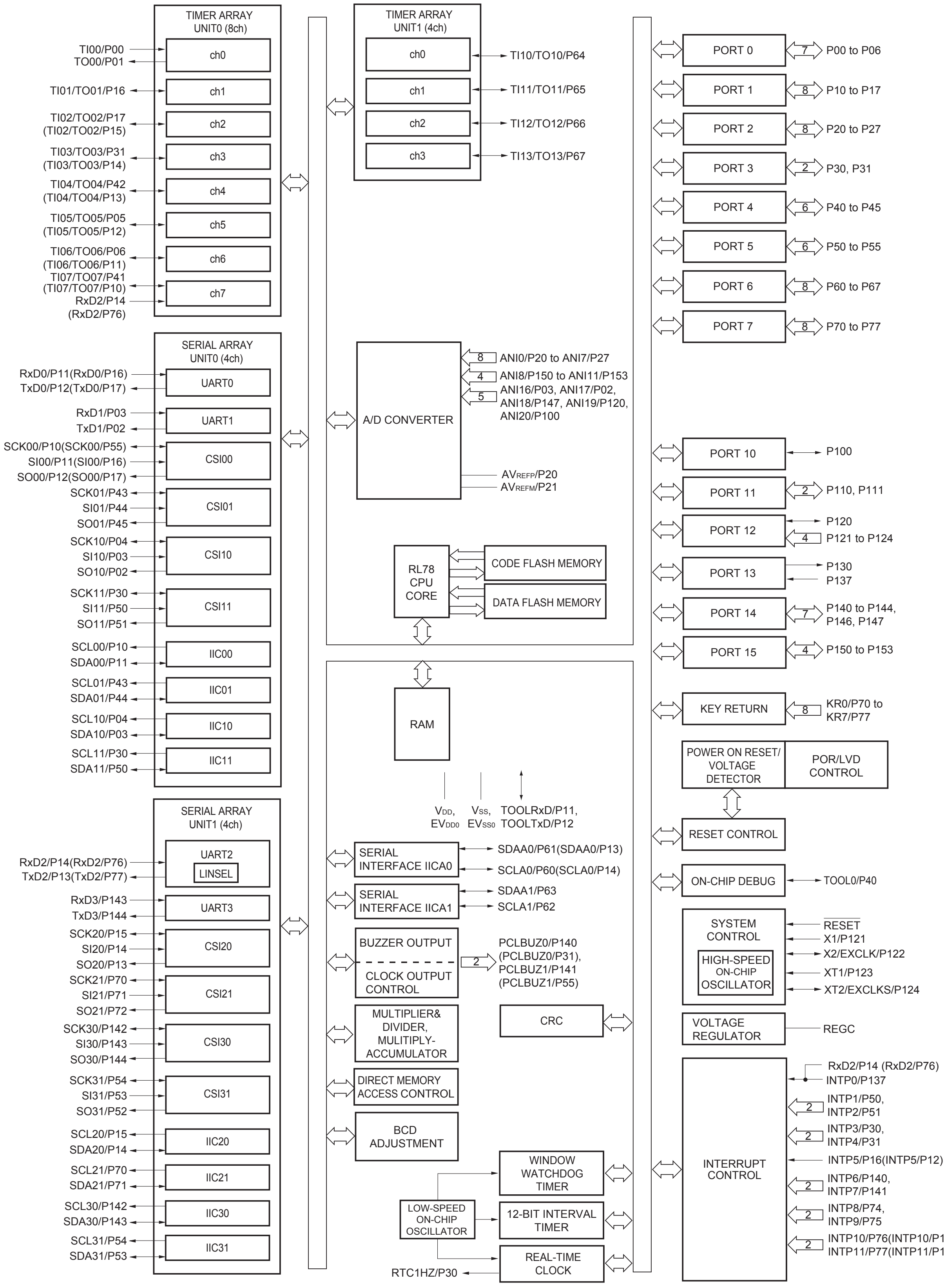
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.4 Pin Identification

ANI0 to ANI14, ANI16 to ANI26:	Analog input
AVREFM:	A/D converter reference potential (– side) input
AVREFP:	A/D converter reference potential (+ side) input
EVDD0, EVDD1:	Power supply for port
EVSS0, EVSS1:	Ground for port
EXCLK:	External clock input (Main system clock)
EXCLKS:	External clock input (Subsystem clock)
INTP0 to INTP11:	Interrupt request from peripheral
KR0 to KR7:	Key return
P00 to P07:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30 to P37:	Port 3
P40 to P47:	Port 4
P50 to P57:	Port 5
P60 to P67:	Port 6
P70 to P77:	Port 7
P80 to P87:	Port 8
P90 to P97:	Port 9
P100 to P106:	Port 10
P110 to P117:	Port 11
P120 to P127:	Port 12
P130, P137:	Port 13
P140 to P147:	Port 14
P150 to P156:	Port 15
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output

REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time clock correction clock (1 Hz) output
RxD0 to RxD3:	Receive data
SCK00, SCK01, SCK10, SCK11, SCK20, SCK21, SCLA0, SCLA1:	Serial clock input/output
SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11, SCL20,SCL21, SCL30, SCL31:	Serial clock output
SDAA0, SDAA1, SDA00, SDA01,SDA10, SDA11, SDA20,SDA21, SDA30, SDA31:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31:	Serial data output
TI00 to TI07, TI10 to TI17:	Timer input
TO00 to TO07, TO10 to TO17:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0 to TxD3:	Transmit data
VDD:	Power supply
VSS:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

1.5.12 80-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 32 MHz
	2.4 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		$1/f_{MCK}+20$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		$1/f_{MCK}+30$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		$1/f_{MCK}+40$		$1/f_{MCK}+40$		$1/f_{MCK}+40$		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		$1/f_{MCK}+40$		$1/f_{MCK}+40$		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI2}	1.8 V ≤ EV_{DD0} ≤ 5.5 V		$1/f_{MCK}+31$		$1/f_{MCK}+31$		$1/f_{MCK}+31$		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		$1/f_{MCK}+250$		$1/f_{MCK}+250$		$1/f_{MCK}+250$		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		$1/f_{MCK}+250$		$1/f_{MCK}+250$		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} ≤ 5.5 V		$2/f_{MCK}+44$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V		$2/f_{MCK}+75$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			1.8 V ≤ EV_{DD0} ≤ 5.5 V		$2/f_{MCK}+110$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			1.7 V ≤ EV_{DD0} ≤ 5.5 V		$2/f_{MCK}+220$		$2/f_{MCK}+220$		$2/f_{MCK}+220$	ns
			1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		$2/f_{MCK}+220$		$2/f_{MCK}+220$	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = −40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**		**Note 1**		**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**		**Note 3**		**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

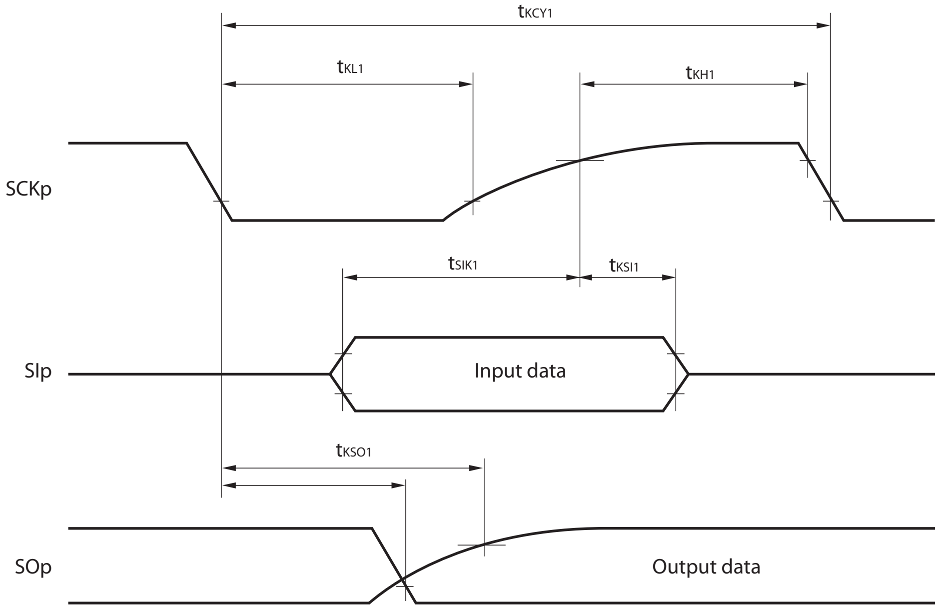
Notes **1.** When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. Use it with EV_{DD0} ≥ V_b.

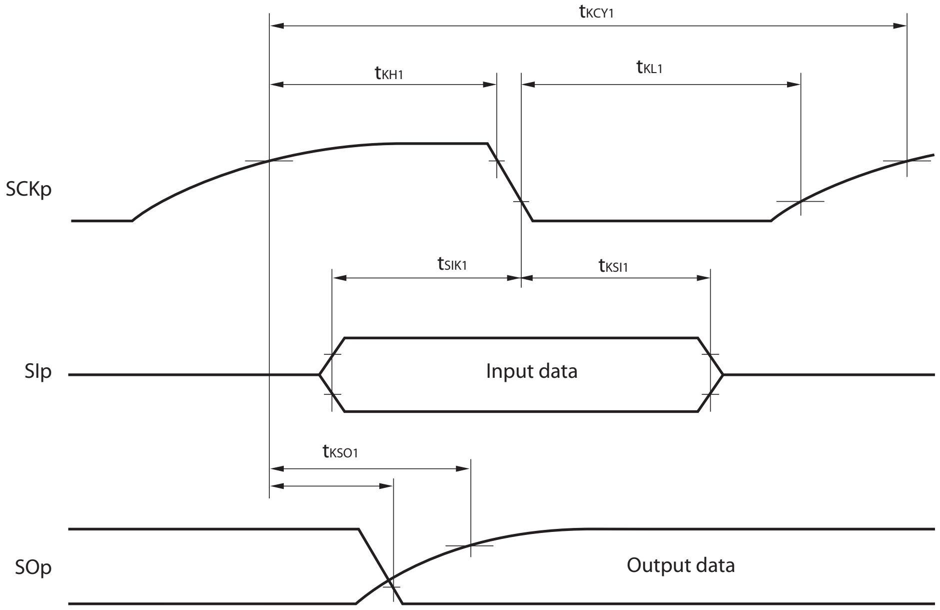
Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = −40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T_A = 25°C		1,000,000		
		Retained for 5 years T_A = 85°C	100,000			
		Retained for 20 years T_A = 85°C	10,000			

Notes **1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_X)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V_{DD} ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f_X)[Note]	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

(T_A = –40 to +105°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency[Notes 1, 2]	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		–20 to +85 °C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.0		+1.0	%
		–40 to –20 °C	2.4 V ≤ V_{DD} ≤ 5.5 V	–1.5		+1.5	%
		+85 to +105 °C	2.4 V ≤ V_{DD} ≤ 5.5 V	–2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				–15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

($T_A = -40$ to $+105°C$, $2.4\ V \le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5\ V$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\ V$) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$2.4\ V \le EV_{DD0} \le 5.5\ V$			-3.0 [Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% [Note 3])	$4.0\ V \le EV_{DD0} \le 5.5\ V$			-30.0	mA
			$2.7\ V \le EV_{DD0} < 4.0\ V$			−10.0	mA
			$2.4\ V \le EV_{DD0} < 2.7\ V$			−5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% [Note 3])	$4.0\ V \le EV_{DD0} \le 5.5\ V$			-30.0	mA
			$2.7\ V \le EV_{DD0} < 4.0\ V$			−19.0	mA
			$2.4\ V \le EV_{DD0} < 2.7\ V$			−10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	$2.4\ V \le EV_{DD0} \le 5.5\ V$			-60.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P156	$2,4\ V \le V_{DD} \le 5.5\ V$			−0.1[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	$2.4\ V \le V_{DD} \le 5.5\ V$			−1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, EV_{DD1}, V_{DD} pins to an output pin.

2. Do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

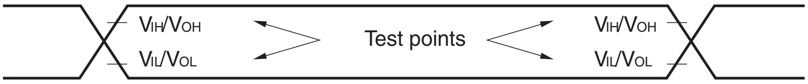
However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)
(T_A = –40 to +105°C, 2.4 V ≤ $EV_{DD0} = EV_{DD1} \leq V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V)

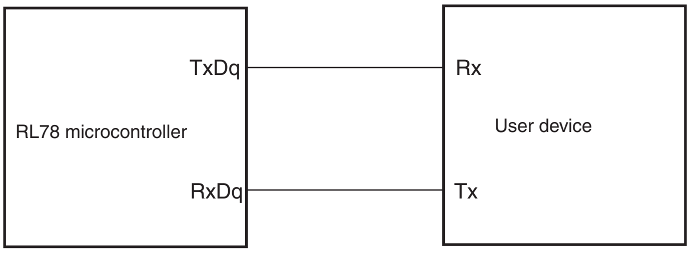
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate [Note 1]				$f_{MCK}/12$ [Note 2]	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, $f_{MCK} = f_{CLK}$		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

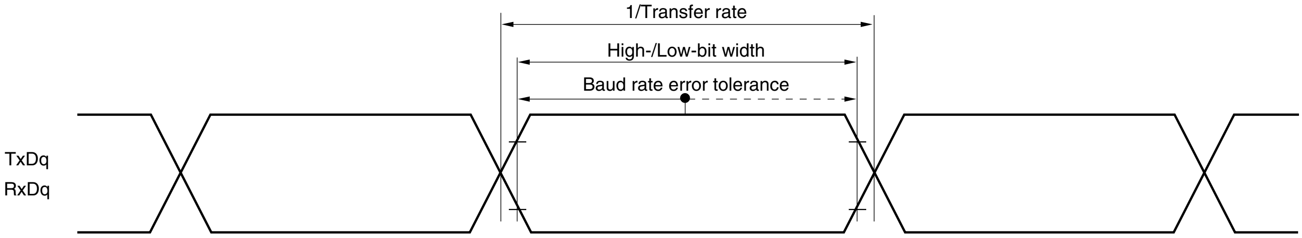
2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.
2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 340 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 340 Note 2		ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	$1/f_{MCK}$ + 760 Note 2		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 760 Note 2		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 570 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 100 pF, R_b = 5.5 kΩ	0	1215	ns

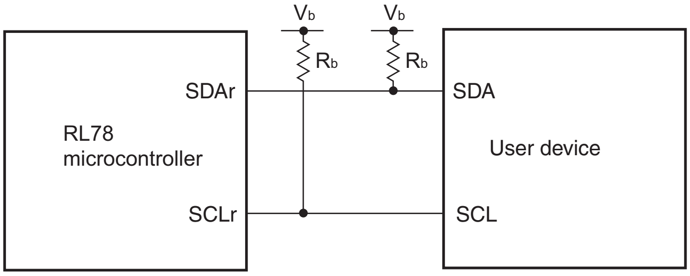
Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

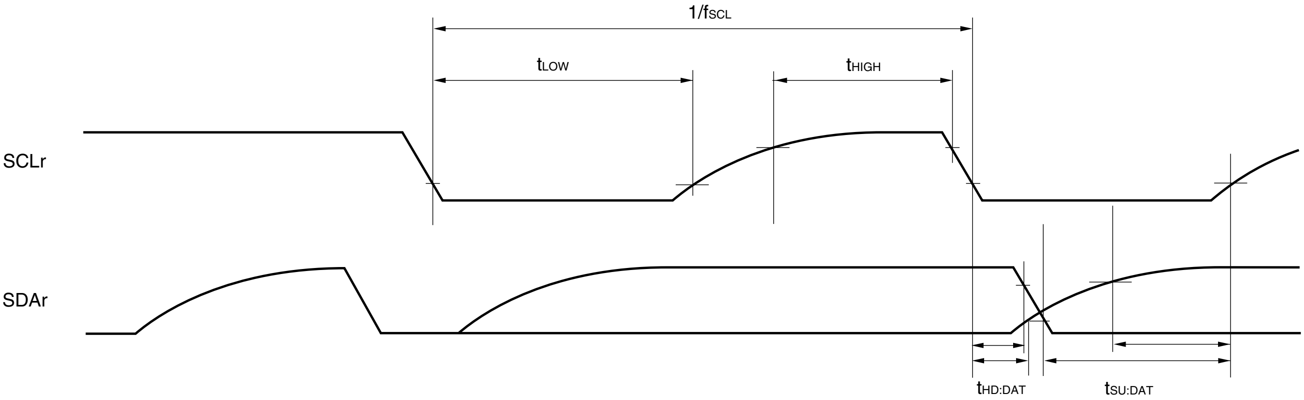
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V_{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.4 V ≤ V_{DD} ≤ 5.5 V			±2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
		Internal reference voltage output (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{BGR}[Note 3]			V
		Temperature sensor output voltage (2.4 V ≤ V_{DD} ≤ 5.5 V, HS (high-speed main) mode)		V_{TMPS25}[Note 3]			V

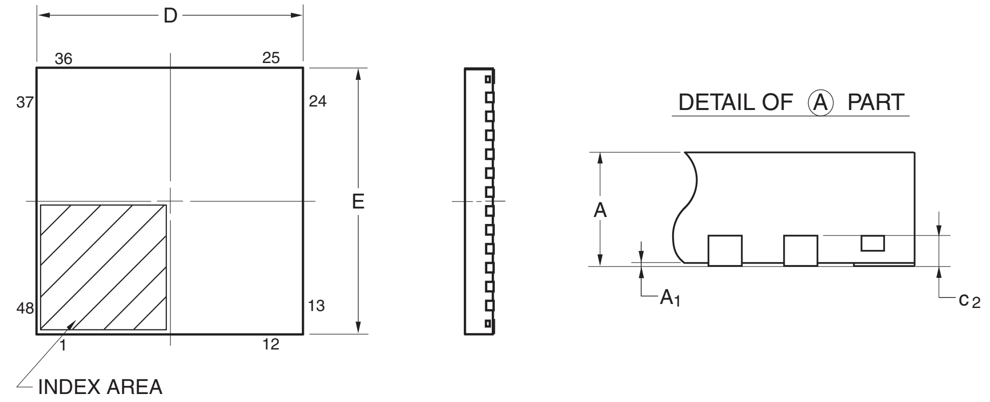
Notes **1.** Excludes quantization error (±1/2 LSB).

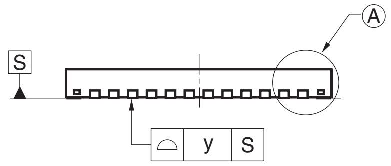
2. This value is indicated as a ratio (%FSR) to the full-scale value.

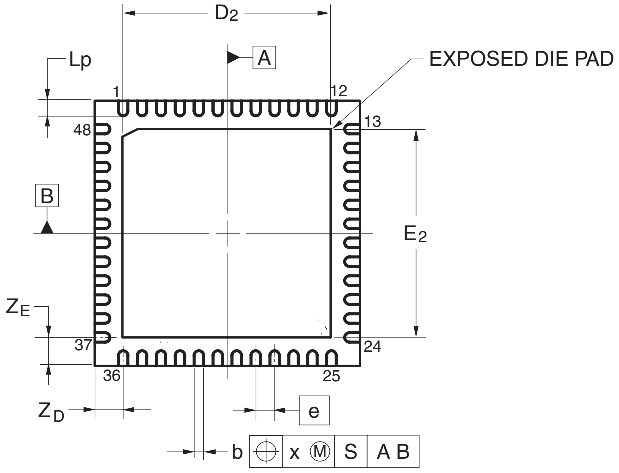
3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA, R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA, R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA, R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA, R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA, R5F100GHGNA, R5F100GJGNA

JEITA Package code	**RENESAS code**	**Previous code**	**MASS(TYP.)[g]**
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13







Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB

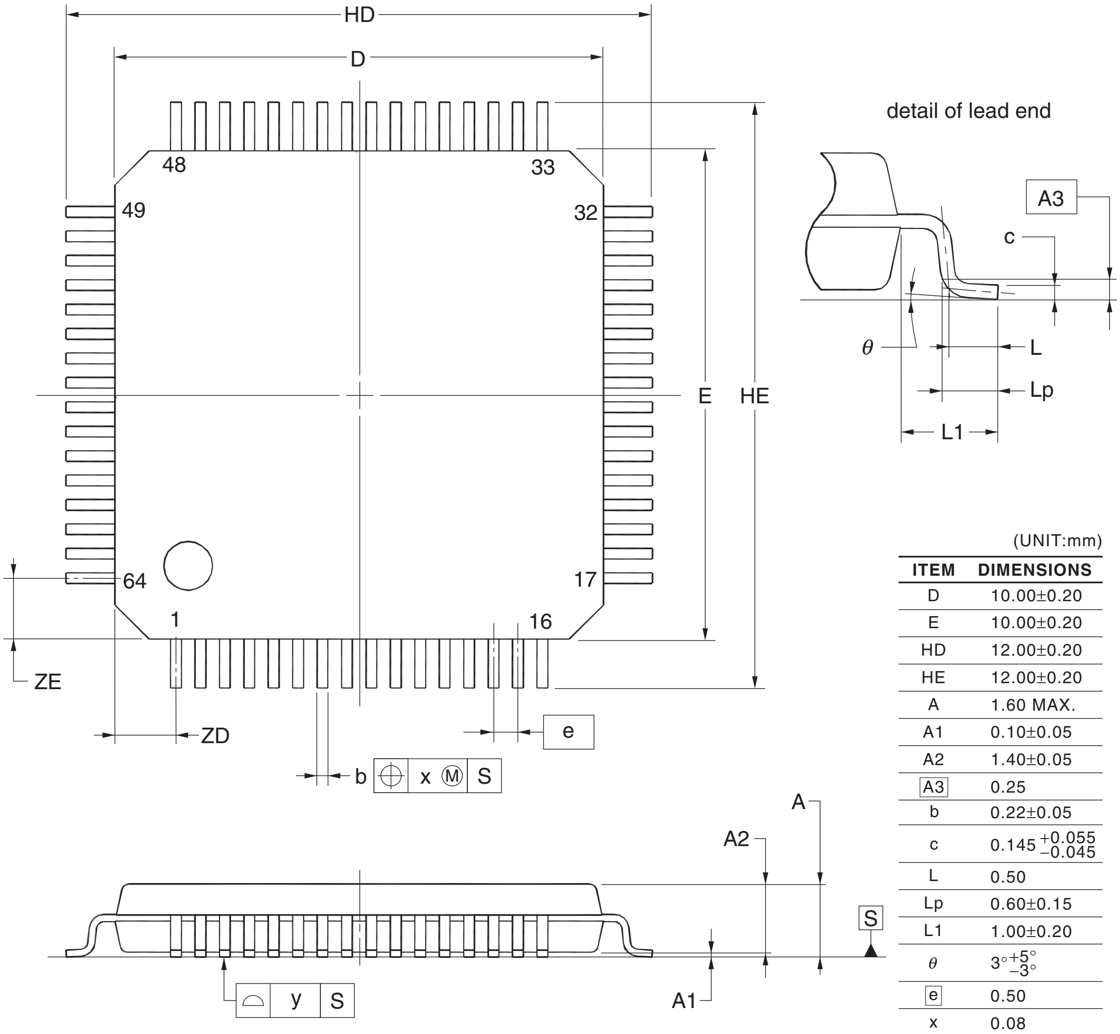
R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB

R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB, R5F100LKDFB, R5F100LLDFB

R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB, R5F101LKDFB, R5F101LLDFB

R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB, R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.