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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

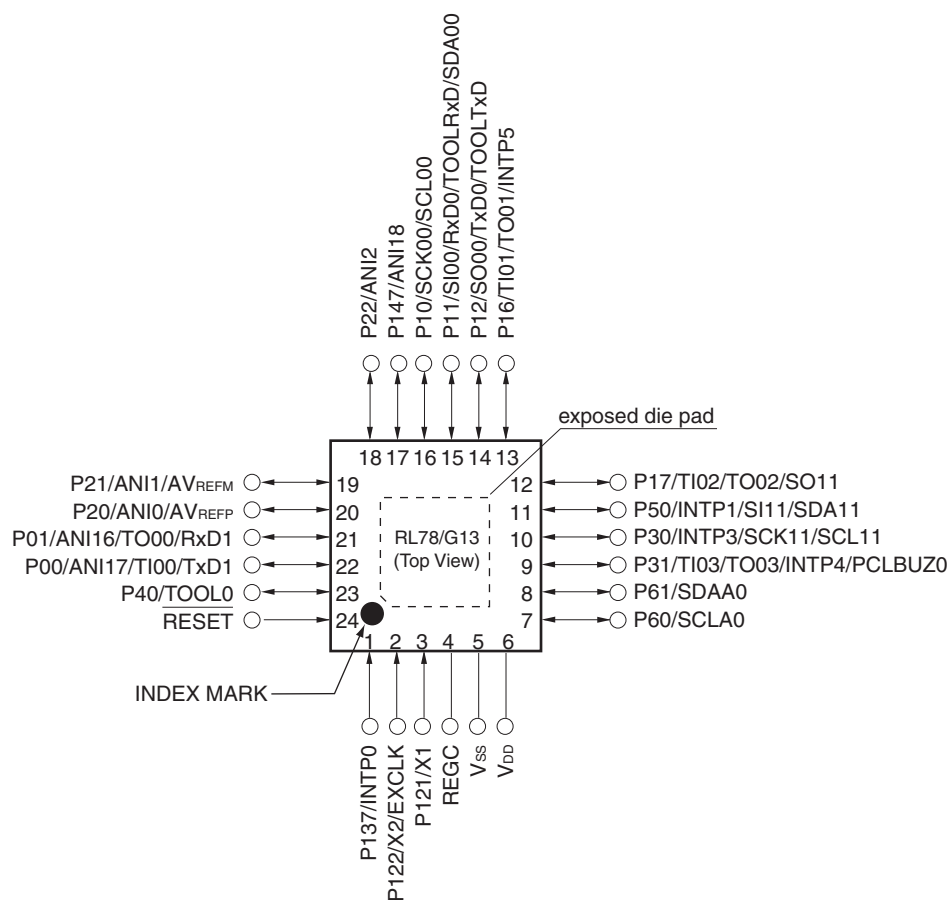| Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100pgafb-v0

Table 1-1. List of Ordering Part Numbers

(3/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	Mounted	A	R5F100CAALA#U0, R5F100CCALA#U0, R5F100CDALA#U0, R5F100CEALA#U0, R5F100CFALA#U0, R5F100CGALA#U0 R5F100CAALA#W0, R5F100CCALA#W0, R5F100CDALA#W0, R5F100CEALA#W0, R5F100CFALA#W0, R5F100CGALA#W0
			G	R5F100CAGLA#U0, R5F100CCGLA#U0, R5F100CDGLA#U0, R5F100CEGLA#U0, R5F100CFGLA#U0, R5F100CGGLA#U0 R5F100CAGLA#W0, R5F100CCGLA#W0, R5F100CDGLA#W0, R5F100CEGLA#W0, R5F100CFGLA#W0, R5F100CGGLA#W0
		Not mounted	A	R5F101CAALA#U0, R5F101CCALA#U0, R5F101CDALA#U0, R5F101CEALA#U0, R5F101CFALA#U0, R5F101CGALA#U0 R5F101CAALA#W0, R5F101CCALA#W0, R5F101CDALA#W0, R5F101CEALA#W0, R5F101CFALA#W0, R5F101CGALA#W0
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	Mounted	A	R5F100EAANA#U0, R5F100ECANA#U0, R5F100EDANA#U0, R5F100EEANA#U0, R5F100EFANA#U0, R5F100EGANA#U0, R5F100EHANA#U0 R5F100EAANA#W0, R5F100ECANA#W0, R5F100EDANA#W0, R5F100EEANA#W0, R5F100EFANA#W0, R5F100EGANA#W0, R5F100EHANA#W0
			D	R5F100EADNA#U0, R5F100ECDNA#U0, R5F100EDDNA#U0, R5F100EEDNA#U0, R5F100EFDNA#U0, R5F100EGDNA#U0, R5F100EHDNA#U0 R5F100EADNA#W0, R5F100ECDNA#W0, R5F100EDDNA#W0, R5F100EEDNA#W0, R5F100EFDNA#W0, R5F100EGDNA#W0, R5F100EHDNA#W0
			G	R5F100EAGNA#U0, R5F100ECGNA#U0, R5F100EDGNA#U0, R5F100EEGNA#U0, R5F100EFGNA#U0, R5F100EGGNA#U0, R5F100EHGNA#U0 R5F100EAGNA#W0, R5F100ECGNA#W0, R5F100EDGNA#W0, R5F100EEGNA#W0, R5F100EFGNA#W0, R5F100EGGNA#W0, R5F100EHGNA#W0
		Not mounted	A	R5F101EAANA#U0, R5F101ECANA#U0, R5F101EDANA#U0, R5F101EEANA#U0, R5F101EFANA#U0, R5F101EGANA#U0, R5F101EHANA#U0 R5F101EAANA#W0, R5F101ECANA#W0, R5F101EDANA#W0, R5F101EEANA#W0, R5F101EFANA#W0, R5F101EGANA#W0, R5F101EHANA#W0
			D	R5F101EADNA#U0, R5F101ECDNA#U0, R5F101EDDNA#U0, R5F101EEDNA#U0, R5F101EFDNA#U0, R5F101EGDNA#U0, R5F101EHDNA#U0 R5F101EADNA#W0, R5F101ECDNA#W0, R5F101EDDNA#W0, R5F101EEDNA#W0, R5F101EFDNA#W0, R5F101EGDNA#W0, R5F101EHDNA#W0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2　24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

Top pins (13–18):
- 18: P22/ANI2
- 17: P147/ANI18
- 16: P10/SCK00/SCL00
- 15: P11/SI00/RxD0/TOOLRxD/SDA00
- 14: P12/SO00/TxD0/TOOLTxD
- 13: P16/TI01/TO01/INTP5

exposed die pad

Left pins (19–24):
- 19: P21/ANI1/AVREFM
- 20: P20/ANI0/AVREFP
- 21: P01/ANI16/TO00/RxD1
- 22: P00/ANI17/TI00/TxD1
- 23: P40/TOOL0
- 24: RESET

RL78/G13 (Top View)

INDEX MARK

Right pins (7–12):
- 12: P17/TI02/TO02/SO11
- 11: P50/INTP1/SI11/SDA11
- 10: P30/INTP3/SCK11/SCL11
- 9: P31/TI03/TO03/INTP4/PCLBUZ0
- 8: P61/SDAA0
- 7: P60/SCLA0

Bottom pins (1–6):
- 1: P137/INTP0
- 2: P122/X2/EXCLK
- 3: P121/X1
- 4: REGC
- 5: VSS
- 6: VDD

Caution　Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4　Pin Identification**.
　　　　　2. It is recommended to connect an exposed die pad to Vss.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

**(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)**

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+20		1/f$_{MCK}$+30		1/f$_{MCK}$+30		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+30		1/f$_{MCK}$+30		1/f$_{MCK}$+30		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+40		1/f$_{MCK}$+40		1/f$_{MCK}$+40		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		1/f$_{MCK}$+40		1/f$_{MCK}$+40		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$	1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+31		1/f$_{MCK}$+31		1/f$_{MCK}$+31		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+250		1/f$_{MCK}$+250		1/f$_{MCK}$+250		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		1/f$_{MCK}$+250		1/f$_{MCK}$+250		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note 4]	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+44		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+75		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+110		2/f$_{MCK}$+110		2/f$_{MCK}$+110	ns
			1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+220		2/f$_{MCK}$+220		2/f$_{MCK}$+220	ns
			1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		2/f$_{MCK}$+220		2/f$_{MCK}$+220	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. C is the load capacitance of the SOp output lines.

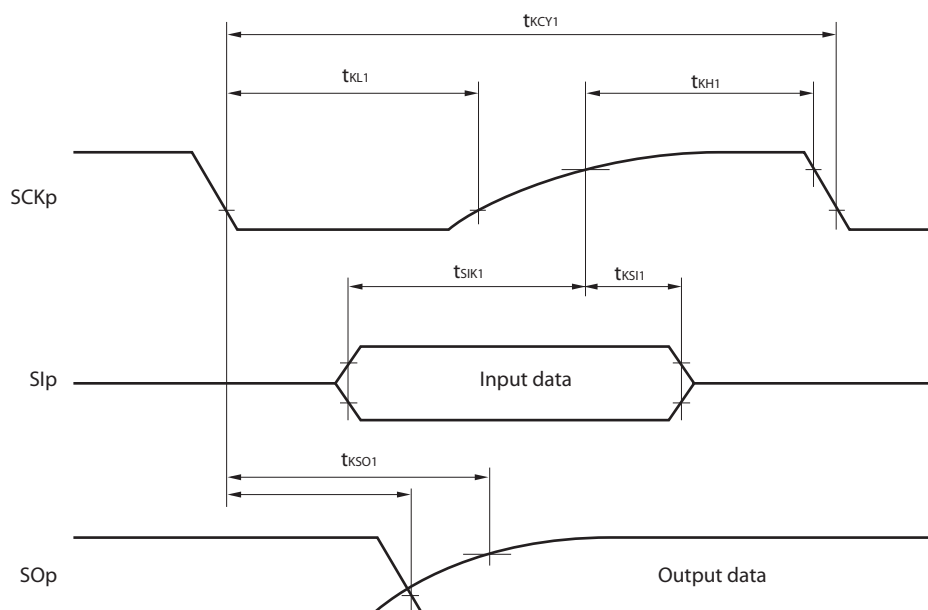   **5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
    n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

    2. f$_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
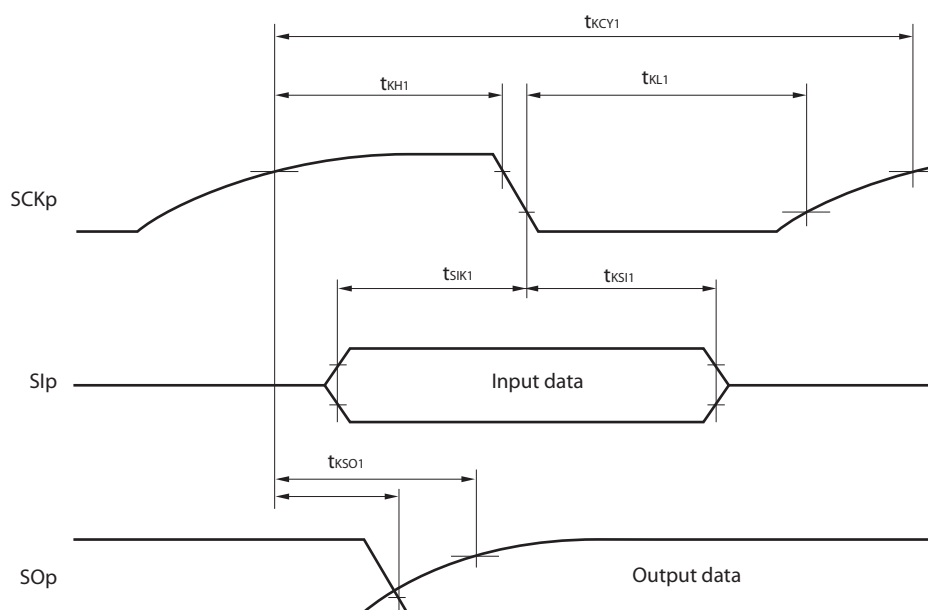
CSI mode connection diagram (during communication at different potential)
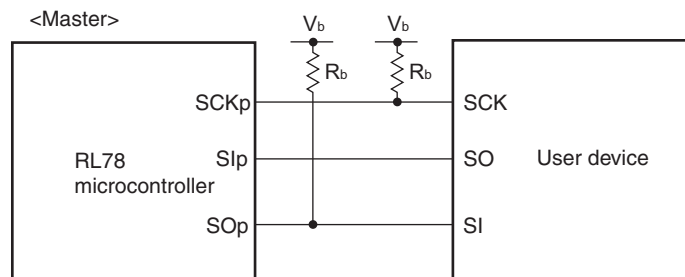
Remarks **1.** $R_b[\Omega]$:Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

        2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

        3. f_{MCK}: Serial array unit operation clock frequency

           (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

           m: Unit number, n: Channel number (mn = 00))

        4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
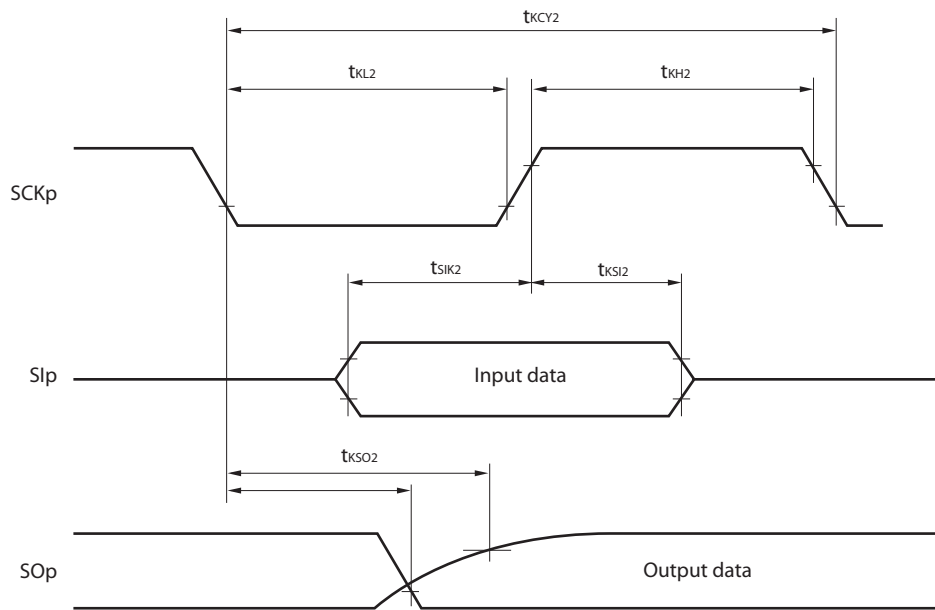**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

     2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
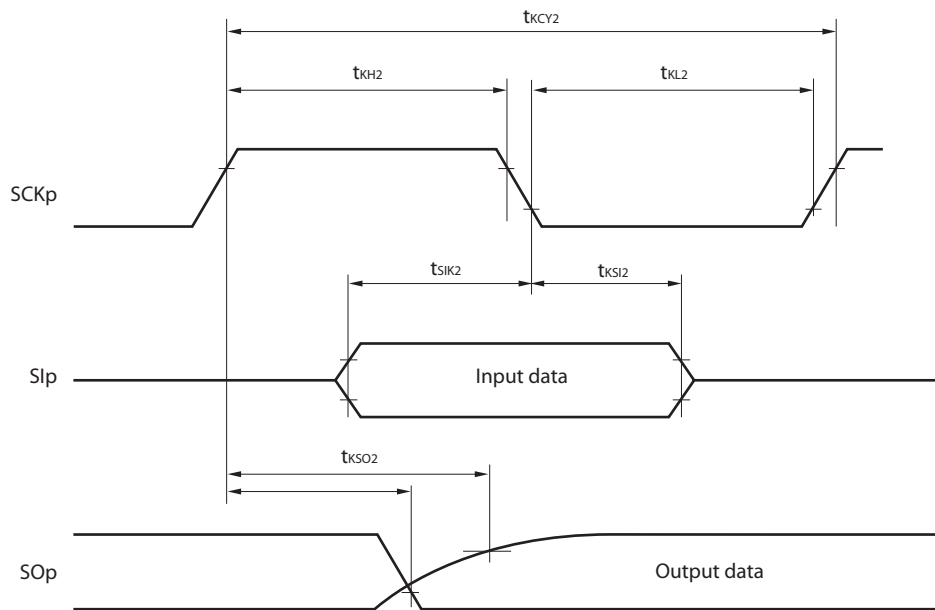**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

Simplified I^{2}C mode connection diagram (during communication at different potential)
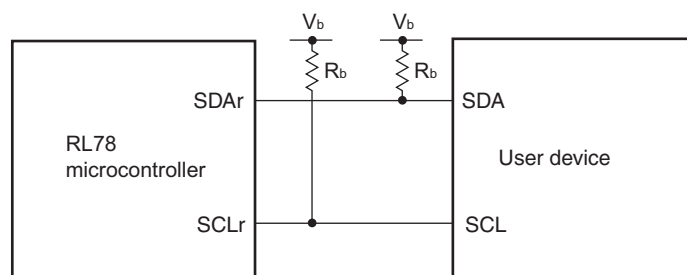
Simplified I^{2}C mode serial transfer timing (during communication at different potential)
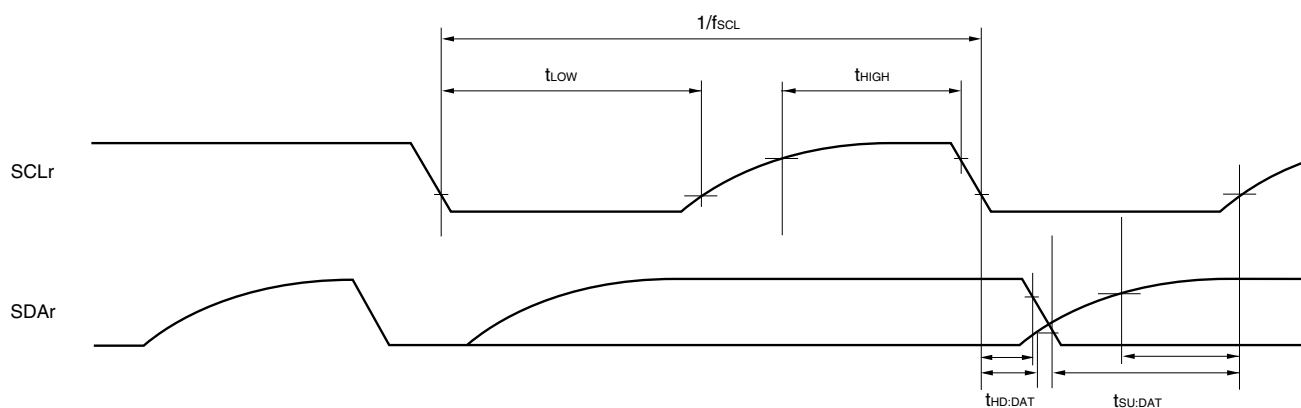
Remarks **1.** R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

    2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

    3. f$_{MCK}$: Serial array unit operation clock frequency

       (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

       n: Channel number (mn = 00, 01, 02, 10, 12, 13)

2.5.2 Serial interface IICA

(1) I^{2}C standard mode

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode MIN.	HS MAX.	LS (low-speed main) Mode MIN.	LS MAX.	LV (low-voltage main) Mode MIN.	LV MAX.	Unit
SCLA0 clock frequency	f$_{SCL}$	Standard mode: f$_{CLK}$ ≥ 1 MHz	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t$_{SU:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.7		4.7		µs
Hold time[Note 1]	t$_{HD:STA}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.0		4.0		µs
Hold time when SCLA0 = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.7		4.7		µs
Hold time when SCLA0 = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.0		4.0		µs
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		250		250		250		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		250		250		250		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		250		250		250		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		250		250		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	3.45	0	3.45	0	3.45	µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	3.45	0	3.45	0	3.45	µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		0	3.45	0	3.45	0	3.45	µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		0	3.45	0	3.45	µs
Setup time of stop condition	t$_{SU:STO}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.0		4.0		4.0		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.0		4.0		µs
Bus-free time	t$_{BUF}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		4.7		4.7		4.7		µs
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		4.7		4.7		µs

(**Notes**, **Caution** and **Remark** are listed on the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI14	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI26	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		–

(1) When reference voltage (+)= AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±5.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 5]		V

(**Notes** are listed on the next page.)

LVD Detection Voltage of Interrupt & Reset Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDA0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 0, falling reset voltage			1.60	1.63	1.66	V
	V$_{LVDA1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		1.74	1.77	1.81	V
			Falling interrupt voltage		1.70	1.73	1.77	V
	V$_{LVDA2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		1.84	1.88	1.91	V
			Falling interrupt voltage		1.80	1.84	1.87	V
	V$_{LVDA3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		2.86	2.92	2.97	V
			Falling interrupt voltage		2.80	2.86	2.91	V
	V$_{LVDB0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 1, falling reset voltage			1.80	1.84	1.87	V
	V$_{LVDB1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		1.94	1.98	2.02	V
			Falling interrupt voltage		1.90	1.94	1.98	V
	V$_{LVDB2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.05	2.09	2.13	V
			Falling interrupt voltage		2.00	2.04	2.08	V
	V$_{LVDB3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.07	3.13	3.19	V
			Falling interrupt voltage		3.00	3.06	3.12	V
	V$_{LVDC0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 0, falling reset voltage			2.40	2.45	2.50	V
	V$_{LVDC1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		2.56	2.61	2.66	V
			Falling interrupt voltage		2.50	2.55	2.60	V
	V$_{LVDC2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.66	2.71	2.76	V
			Falling interrupt voltage		2.60	2.65	2.70	V
	V$_{LVDC3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.68	3.75	3.82	V
			Falling interrupt voltage		3.60	3.67	3.74	V
	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 1, falling reset voltage			2.70	2.75	2.81	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage		2.86	2.92	2.97	V
			Falling interrupt voltage		2.80	2.86	2.91	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage		2.96	3.02	3.08	V
			Falling interrupt voltage		2.90	2.96	3.02	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage		3.98	4.06	4.14	V
			Falling interrupt voltage		3.90	3.98	4.06	V

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = −40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			2.4 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V

Caution   **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.54	2.90	mA
					V$_{DD}$ = 3.0 V		0.54	2.90	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	2.30	mA
					V$_{DD}$ = 3.0 V		0.44	2.30	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.40	1.70	mA
					V$_{DD}$ = 3.0 V		0.40	1.70	mA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.28	1.90	mA
					Resonator connection		0.45	2.00	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.19	1.02	mA
					Resonator connection		0.26	1.10	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.37	1.17	μA
					Resonator connection		0.56	1.36	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.53	1.97	μA
					Resonator connection		0.72	2.16	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		0.82	3.37	μA
					Resonator connection		1.01	3.56	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +105°C	Square wave input		3.01	15.37	μA
					Resonator connection		3.20	15.56	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	μA
			T$_A$ = +50°C				0.30	1.10	μA
			T$_A$ = +70°C				0.46	1.90	μA
			T$_A$ = +85°C				0.75	3.30	μA
			T$_A$ = +105°C				2.94	15.30	μA

(**Notes** and **Remarks** are listed on the next page.)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
Transfer rate		Transmission	4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V, 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V		**Note 1**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.6 [Note 2]	Mbps
			2.7 V $\leq$ EV$_{DD0}$ < 4.0 V, 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V		**Note 3**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 [Note 4]	Mbps
			2.4 V $\leq$ EV$_{DD0}$ < 3.3 V, 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V		**Note 5**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 [Note 6]	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V $\leq$ EV$_{DD0}$ $\leq$ 5.5 V and 2.7 V $\leq$ V$_b$ $\leq$ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f$_{MCK}$/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.4 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 24		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 36		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]		t$_{KCY2}$/2 − 100		ns
SIp setup time (to SCKp↑) [Note 2]	t$_{SIK2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ Note 3, Reference voltage (–) = AV$_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (–) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = AV$_{REFM}$.

3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
R5F100BAGNA, R5F100BCGNA, R5F100BDGNA,R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
Ⓔe	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	3.50	—
E_2	—	3.50	—
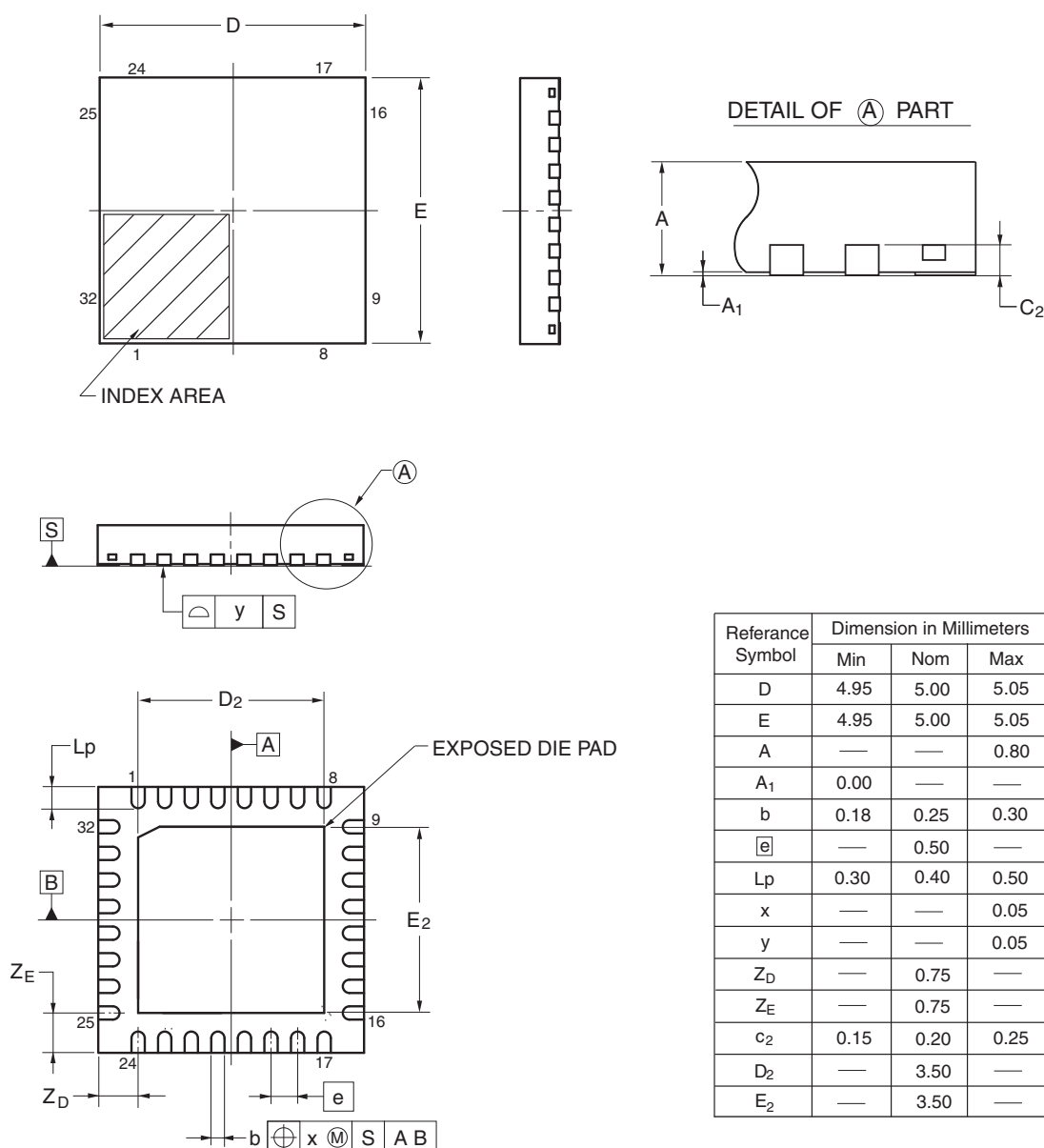
4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

INDEX MARK

DETAIL C

DETAIL D

DETAIL E

φb
(LAND PAD)

φ 0.34±0.05
(APERTURE OF
SOLDER RESIST)

0.70±0.05
0.55±0.05
0.75
0.55
R0.17±0.05
R0.12±0.05

0.55
0.75
0.55±0.05
0.70±0.05

R0.17±0.05
R0.12±0.05
0.70±0.05
0.55±0.05
0.75
0.55

0.55
0.75
R0.275±0.05
0.55±0.05
0.70±0.05
R0.35±0.05
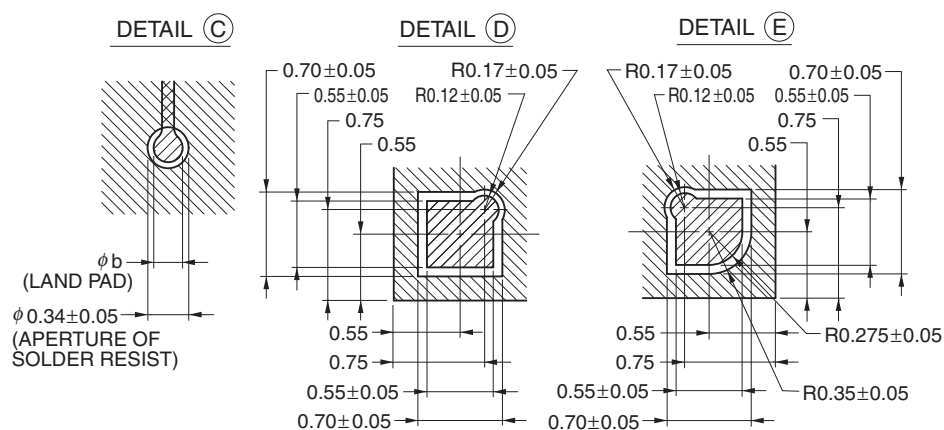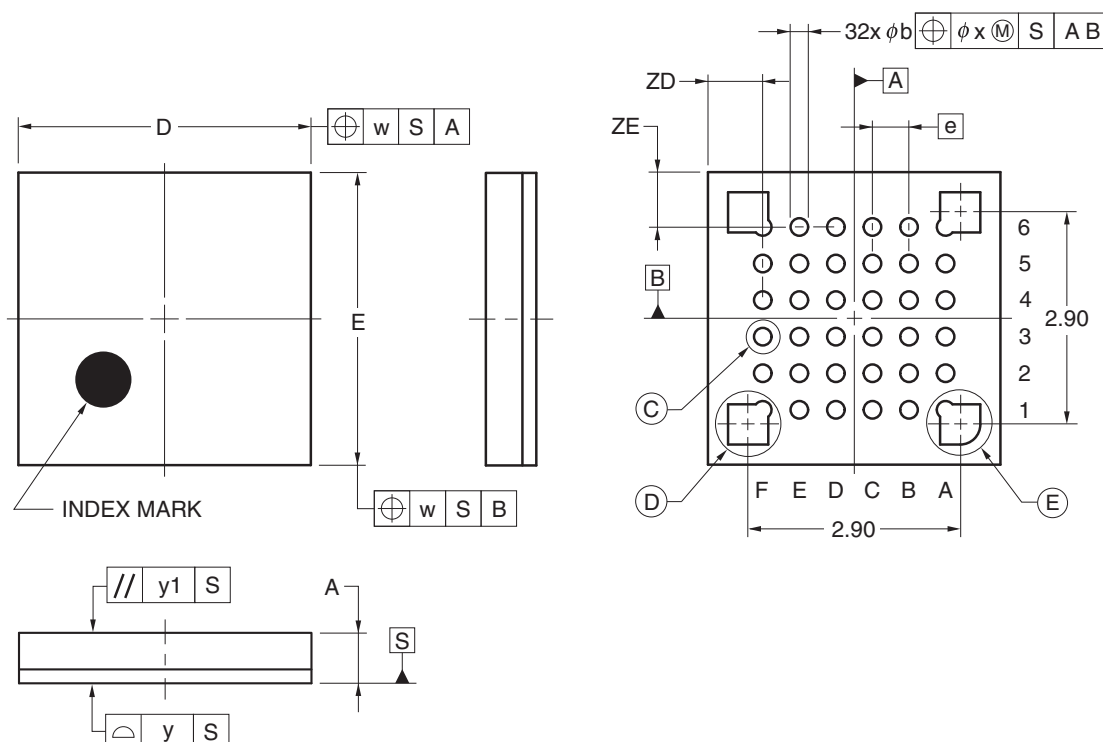
(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

		Description	
Rev.	**Date**	**Page**	**Summary**
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I^2C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I^2C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^2C mode) (2/2)
		109	Addition of (1) I^2C standard mode
		111	Addition of (2) I^2C fast mode
		112	Addition of (3) I^2C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)