**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

**Applications of "Embedded - Microcontrollers"**

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 82 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 20x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100phafb-x0 |

**Table 1-1. List of Ordering Part Numbers**

(9/12)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 64 pins | 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch) | Mounted | A | R5F100LCAFB#V0, R5F100LDAFB#V0, R5F100LEAFB#V0, R5F100LFAFB#V0, R5F100LGAFB#V0, R5F100LHAFB#V0, R5F100LJAFB#V0, R5F100LKAFB#V0, R5F100LLAFB#V0 R5F100LCAFB#X0, R5F100LDAFB#X0, R5F100LEAFB#X0, R5F100LFAFB#X0, R5F100LGAFB#X0, R5F100LHAFB#X0, R5F100LJAFB#X0, R5F100LKAFB#X0, R5F100LLAFB#X0 |
| | | | D | R5F100LCDFB#V0, R5F100LDDFB#V0, R5F100LEDFB#V0, R5F100LFDFB#V0, R5F100LGDFB#V0, R5F100LHDFB#V0, R5F100LJDFB#V0, R5F100LKDFB#V0, R5F100LLDFB#V0 R5F100LCDFB#X0, R5F100LDDFB#X0, R5F100LEDFB#X0, R5F100LFDFB#X0, R5F100LGDFB#X0, R5F100LHDFB#X0, R5F100LJDFB#X0, R5F100LKDFB#X0, R5F100LLDFB#X0 |
| | | | G | R5F100LCGFB#V0, R5F100LDGFB#V0, R5F100LEGFB#V0, R5F100LFGFB#V0 R5F100LCGFB#X0, R5F100LDGFB#X0, R5F100LEGFB#X0, R5F100LFGFB#X0 R5F100LGGFB#V0, R5F100LHGFB#V0, R5F100LJGFB#V0 R5F100LGGFB#X0, R5F100LHGFB#X0, R5F100LJGFB#X0 |
| | | Not mounted | A | R5F101LCAFB#V0, R5F101LDAFB#V0, R5F101LEAFB#V0, R5F101LFAFB#V0, R5F101LGAFB#V0, R5F101LHAFB#V0, R5F101LJAFB#V0, R5F101LKAFB#V0, R5F101LLAFB#V0 R5F101LCAFB#X0, R5F101LDAFB#X0, R5F101LEAFB#X0, R5F101LFAFB#X0, R5F101LGAFB#X0, R5F101LHAFB#X0, R5F101LJAFB#X0, R5F101LKAFB#X0, R5F101LLAFB#X0 |
| | | | D | R5F101LCDFB#V0, R5F101LDDFB#V0, R5F101LEDFB#V0, R5F101LFDFB#V0, R5F101LGDFB#V0, R5F101LHDFB#V0, R5F101LJDFB#V0, R5F101LKDFB#V0, R5F101LLDFB#V0 R5F101LCDFB#X0, R5F101LDDFB#X0, R5F101LEDFB#X0, R5F101LFDFB#X0, R5F101LGDFB#X0, R5F101LHDFB#X0, R5F101LJDFB#X0, R5F101LKDFB#X0, R5F101LLDFB#X0 |
| | 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch) | Mounted | A | R5F100LCABG#U0, R5F100LDABG#U0, R5F100LEABG#U0, R5F100LFABG#U0, R5F100LGABG#U0, R5F100LHABG#U0, R5F100LJABG#U0 R5F100LCABG#W0, R5F100LDABG#W0, R5F100LEABG#W0, R5F100LFABG#W0, R5F100LGABG#W0, R5F100LHABG#W0, R5F100LJABG#W0 |
| | | | G | R5F100LCGBG#U0, R5F100LDGBG#U0, R5F100LEGBG#U0, R5F100LFGBG#U0, R5F100LGGBG#U0, R5F100LHGBG#U0, R5F100LJGBG#U0 R5F100LCGBG#W0, R5F100LDGBG#W0, R5F100LEGBG#W0, R5F100LFGBG#W0, R5F100LGGBG#W0, R5F100LHGBG#W0, R5F100LJGBG#W0 |
| | | Not mounted | A | R5F101LCABG#U0, R5F101LDABG#U0, R5F101LEABG#U0, R5F101LFABG#U0, R5F101LGABG#U0, R5F101LHABG#U0, R5F101LJABG#U0 R5F101LCABG#W0, R5F101LDABG#W0, R5F101LEABG#W0, R5F101LFABG#W0, R5F101LGABG#W0, R5F101LHABG#W0, R5F101LJABG#W0 |

**Note** For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

**Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**
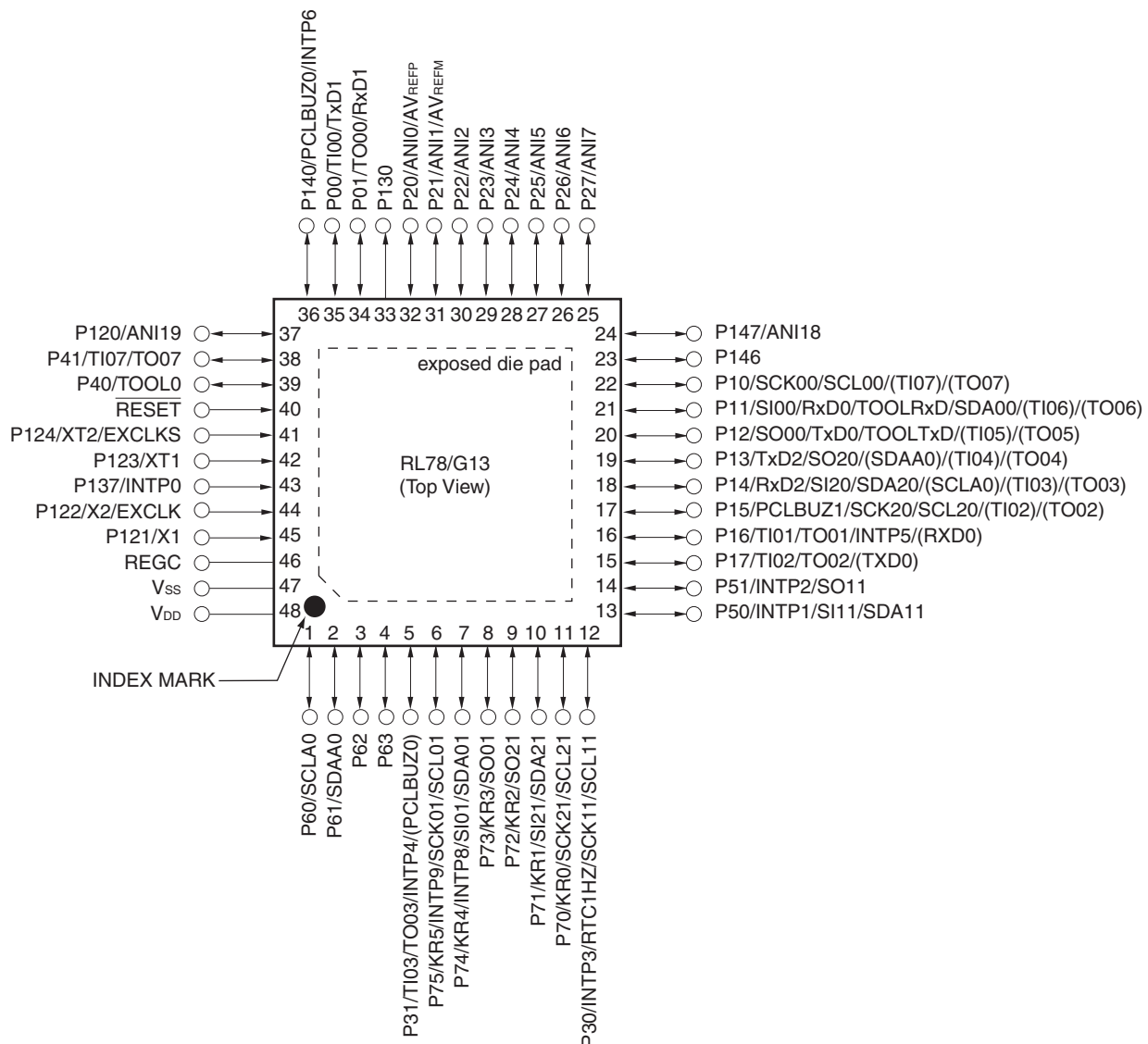
**Table 1-1.  List of Ordering Part Numbers**

(12/12)

| Pin count | Package | Data flash | Fields of Application [Note] | Ordering Part Number |
|---|---|---|---|---|
| 128 pins | 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch) | Mounted | A | R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0 |
| | | | D | R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0 |
| | | Not mounted | A | R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0 |
| | | | D | R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0 |

**Note**    For the fields of application, refer to **Figure 1-1  Part Number, Memory Size, and Package of RL78/G13**.

**Caution  The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Top pins (36–25):
P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Left pins:
- 37 P120/ANI19
- 38 P41/TI07/TO07
- 39 P40/TOOL0
- 40 $\overline{RESET}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 V$_{SS}$
- 48 V$_{DD}$

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RL78/G13
(Top View)

exposed die pad

Right pins:
- 24 P147/ANI18
- 23 P146
- 22 P10/SCK00/SCL00/(TI07)/(TO07)
- 21 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 P16/TI01/TO01/INTP5/(RXD0)
- 15 P17/TI02/TO02/(TXD0)
- 14 P51/INTP2/SO11
- 13 P50/INTP1/SI11/SDA11

Bottom pins (1–12):
P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

**Caution　Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

　　　　**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

　　　　**3.** It is recommended to connect an exposed die pad to Vss.

## 1.5.10　52-pin products
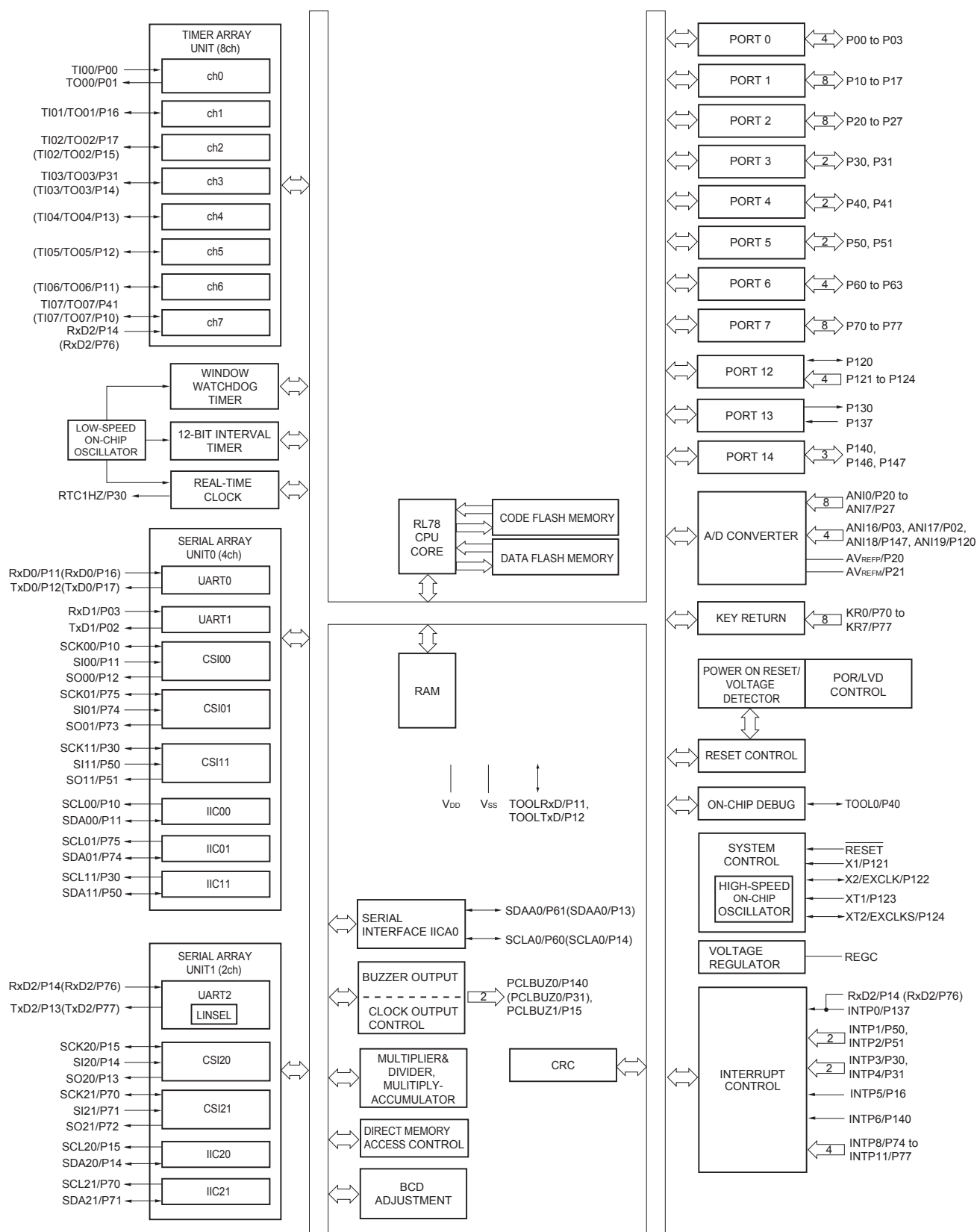


**Remark**　Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).　Refer to **Figure 4-8　Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

**Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F100Ex | R5F101Ex | R5F100Fx | R5F101Fx | R5F100Gx | R5F101Gx | R5F100Jx | R5F101Jx | R5F100Lx | R5F101Lx |
| Code flash memory (KB) | | 16 to 192 | | 16 to 512 | | 16 to 512 | | 32 to 512 | | 32 to 512 | |
| Data flash memory (KB) | | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – | 4 to 8 | – |
| RAM (KB) | | 2 to 16[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | | 2 to 32[Note1] | |
| Address space | | 1 MB | | | | | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz | | | | | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | | | | | |
| General-purpose registers | | (8-bit register × 8) × 4 banks | | | | | | | | | |
| Minimum instruction execution time | | 0.03125 $\mu$s (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | | | | | |
| | | 0.05 $\mu$s (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | | | | | |
| | | 30.5 $\mu$s (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | | | | | |
| I/O port | Total | 36 | | 40 | | 44 | | 48 | | 58 | |
| | CMOS I/O | 28<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 10) | | 31<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 10) | | 34<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 11) | | 38<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 13) | | 48<br>(N-ch O.D. I/O<br>[$V_{DD}$ withstand<br>voltage]: 15) | |
| | CMOS input | 5 | | 5 | | 5 | | 5 | | 5 | |
| | CMOS output | – | | – | | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 3 | | 4 | | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 8 channels | | | | | | | | | |
| | Watchdog timer | 1 channel | | | | | | | | | |
| | Real-time clock (RTC) | 1 channel | | | | | | | | | |
| | 12-bit interval timer (IT) | 1 channel | | | | | | | | | |
| | Timer output | 4 channels (PWM outputs: 3 [Note2]),<br>8 channels (PWM outputs: 7 [Note2][Note3]) | | 5 channels (PWM outputs: 4 [Note2]),<br>8 channels (PWM outputs: 7 [Note2]) [Note 3] | | | | | | 8 channels (PWM outputs: 7 [Note2]) | |
| | RTC output | 1 channel<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | | | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
        The target products and start address of the RAM areas used by the flash library are shown below.
          R5F100xD, R5F101xD (x = E to G, J, L):  Start address FF300H
          R5F100xE, R5F101xE (x = E to G, J, L):  Start address FEF00H
          R5F100xJ, R5F101xJ (x = F, G, J, L):     Start address FAF00H
          R5F100xL, R5F101xL (x = F, G, J, L):     Start address F7F00H
        For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 2.1  Absolute Maximum Ratings

**Absolute Maximum Ratings (T$_A$ = 25°C) (1/2)**

| Parameter | Symbols | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage | V$_{DD}$ | | −0.5 to +6.5 | V |
| | EV$_{DD0}$, EV$_{DD1}$ | EV$_{DD0}$ = EV$_{DD1}$ | −0.5 to +6.5 | V |
| | EV$_{SS0}$, EV$_{SS1}$ | EV$_{SS0}$ = EV$_{SS1}$ | −0.5 to +0.3 | V |
| REGC pin input voltage | V$_{IREGC}$ | REGC | −0.3 to +2.8 and −0.3 to V$_{DD}$ +0.3[Note 1] | V |
| Input voltage | V$_{I1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| | V$_{I2}$ | P60 to P63 (N-ch open-drain) | −0.3 to +6.5 | V |
| | V$_{I3}$ | P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{RESET}$ | −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| Output voltage | V$_{O1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| | V$_{O2}$ | P20 to P27, P150 to P156 | −0.3 to V$_{DD}$ +0.3[Note 2] | V |
| Analog input voltage | V$_{AI1}$ | ANI16 to ANI26 | −0.3 to EV$_{DD0}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3] | V |
| | V$_{AI2}$ | ANI0 to ANI14 | −0.3 to V$_{DD}$ +0.3 and −0.3 to AV$_{REF}$(+) +0.3[Notes 2, 3] | V |

**Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).  This value regulates the absolute maximum rating of the REGC pin.  Do not use this pin with voltage applied to it.
**2.** Must be 6.5 V or lower.
**3.** Do not exceed AV$_{REF}$(+) + 0.3 V in case of A/D conversion target pin**.**

**Caution  Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter.  That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remarks 1.**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
**2.**  AV$_{REF}$ (+) : + side reference voltage of the A/D converter.
**3.**  V$_{SS}$ : Reference voltage

## 2.4 AC Characteristics

**($T_A$ = –40 to +85°C, 1.6 V $\leq$ $EV_{DD0}$ = $EV_{DD1}$ $\leq$ $V_{DD}$ $\leq$ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Instruction cycle (minimum instruction execution time) | $T_{CY}$ | Main system clock ($f_{MAIN}$) operation | HS (high-speed main) mode | 2.7 V $\leq V_{DD} \leq$ 5.5 V | 0.03125 | | 1 | $\mu s$ |
| | | | | 2.4 V $\leq V_{DD} <$ 2.7 V | 0.0625 | | 1 | $\mu s$ |
| | | | LS (low-speed main) mode | 1.8 V $\leq V_{DD} \leq$ 5.5 V | 0.125 | | 1 | $\mu s$ |
| | | | LV (low-voltage main) mode | 1.6 V $\leq V_{DD} \leq$ 5.5 V | 0.25 | | 1 | $\mu s$ |
| | | Subsystem clock ($f_{SUB}$) operation | | 1.8 V $\leq V_{DD} \leq$ 5.5 V | 28.5 | 30.5 | 31.3 | $\mu s$ |
| | | In the self programming mode | HS (high-speed main) mode | 2.7 V $\leq V_{DD} \leq$ 5.5 V | 0.03125 | | 1 | $\mu s$ |
| | | | | 2.4 V $\leq V_{DD} <$ 2.7 V | 0.0625 | | 1 | $\mu s$ |
| | | | LS (low-speed main) mode | 1.8 V $\leq V_{DD} \leq$ 5.5 V | 0.125 | | 1 | $\mu s$ |
| | | | LV (low-voltage main) mode | 1.8 V $\leq V_{DD} \leq$ 5.5 V | 0.25 | | 1 | $\mu s$ |
| External system clock frequency | $f_{EX}$ | 2.7 V $\leq V_{DD} \leq$ 5.5 V | | | 1.0 | | 20.0 | MHz |
| | | 2.4 V $\leq V_{DD} <$ 2.7 V | | | 1.0 | | 16.0 | MHz |
| | | 1.8 V $\leq V_{DD} <$ 2.4 V | | | 1.0 | | 8.0 | MHz |
| | | 1.6 V $\leq V_{DD} <$ 1.8 V | | | 1.0 | | 4.0 | MHz |
| | $f_{EXS}$ | | | | 32 | | 35 | kHz |
| External system clock input high-level width, low-level width | $t_{EXH}$, $t_{EXL}$ | 2.7 V $\leq V_{DD} \leq$ 5.5 V | | | 24 | | | ns |
| | | 2.4 V $\leq V_{DD} <$ 2.7 V | | | 30 | | | ns |
| | | 1.8 V $\leq V_{DD} <$ 2.4 V | | | 60 | | | ns |
| | | 1.6 V $\leq V_{DD} <$ 1.8 V | | | 120 | | | ns |
| | $t_{EXHS}$, $t_{EXLS}$ | | | | 13.7 | | | $\mu s$ |
| TI00 to TI07, TI10 to TI17 input high-level width, low-level width | $t_{TIH}$, $t_{TIL}$ | | | | $1/f_{MCK}+10$ | | | ns[Note] |
| TO00 to TO07, TO10 to TO17 output frequency | $f_{TO}$ | HS (high-speed main) mode | 4.0 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 16 | MHz |
| | | | 2.7 V $\leq EV_{DD0} <$ 4.0 V | | | | 8 | MHz |
| | | | 1.8 V $\leq EV_{DD0} <$ 2.7 V | | | | 4 | MHz |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 4 | MHz |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.6 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 2 | MHz |
| PCLBUZ0, PCLBUZ1 output frequency | $f_{PCL}$ | HS (high-speed main) mode | 4.0 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 16 | MHz |
| | | | 2.7 V $\leq EV_{DD0} <$ 4.0 V | | | | 8 | MHz |
| | | | 1.8 V $\leq EV_{DD0} <$ 2.7 V | | | | 4 | MHz |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | | | 2 | MHz |
| | | LS (low-speed main) mode | 1.8 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 4 | MHz |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | | | 2 | MHz |
| | | LV (low-voltage main) mode | 1.8 V $\leq EV_{DD0} \leq$ 5.5 V | | | | 4 | MHz |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | | | 2 | MHz |
| Interrupt input high-level width, low-level width | $t_{INTH}$, $t_{INTL}$ | INTP0 | 1.6 V $\leq V_{DD} \leq$ 5.5 V | | 1 | | | $\mu s$ |
| | | INTP1 to INTP11 | 1.6 V $\leq EV_{DD0} \leq$ 5.5 V | | 1 | | | $\mu s$ |
| Key interrupt input low-level width | $t_{KR}$ | KR0 to KR7 | 1.8 V $\leq EV_{DD0} \leq$ 5.5 V | | 250 | | | ns |
| | | | 1.6 V $\leq EV_{DD0} <$ 1.8 V | | 1 | | | $\mu s$ |
| $\overline{RESET}$ low-level width | $t_{RSL}$ | | | | 10 | | | $\mu s$ |

(**Note** and **Remark** are listed on the next page.)

**Note**   The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$
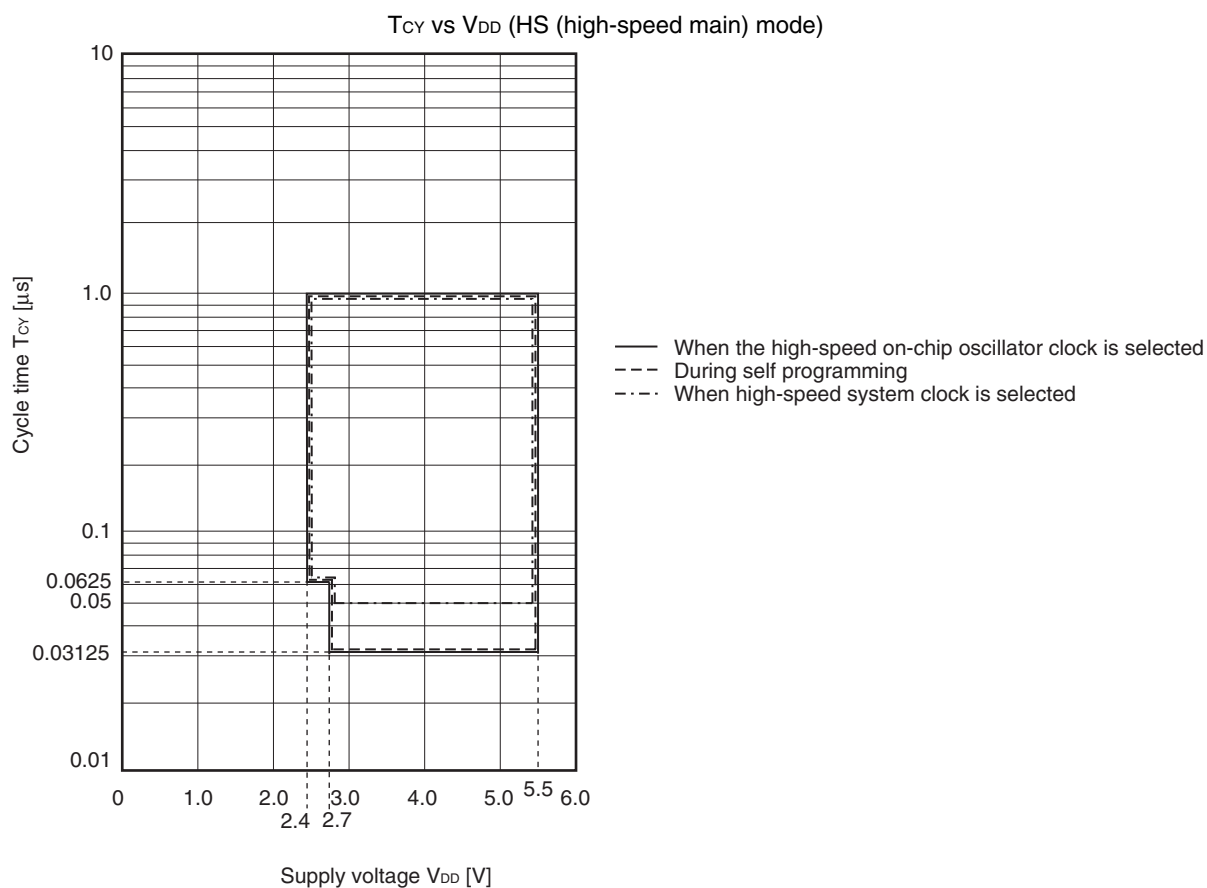
      $1.8\ V \leq EV_{DD0} < 2.7\ V$ : MIN. 125 ns

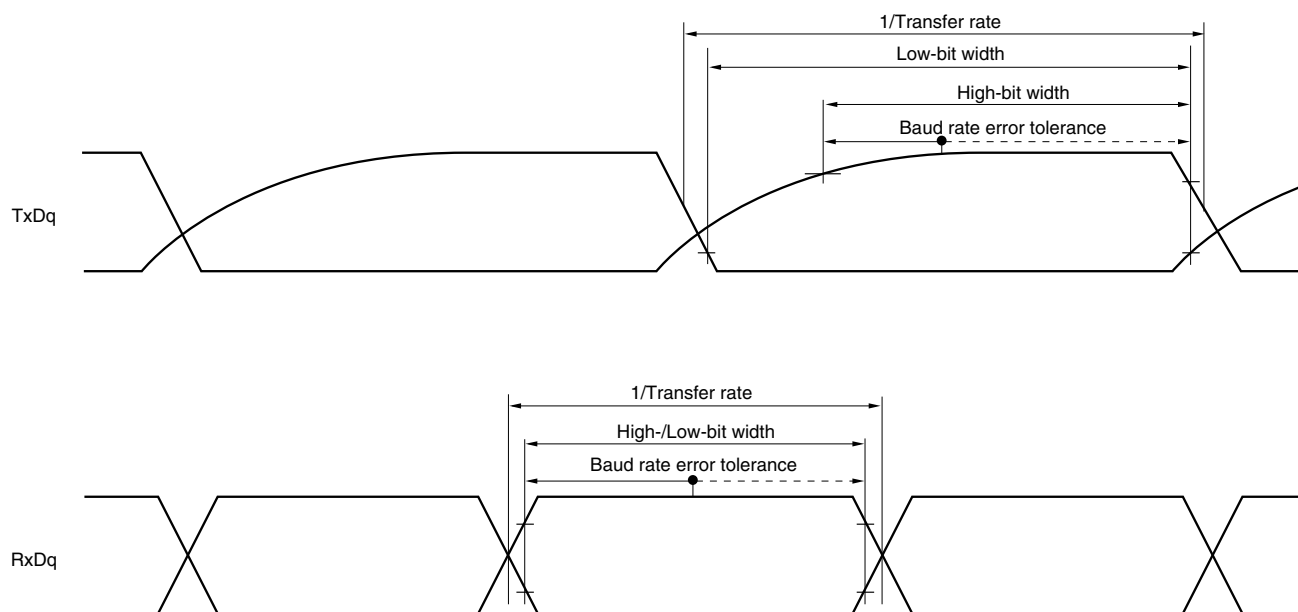      $1.6\ V \leq EV_{DD0} < 1.8\ V$ : MIN. 250 ns

**Remark**   $f_{MCK}$: Timer array unit operation clock frequency

      (Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

      m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

**Minimum Instruction Execution Time during Main System Clock Operation**



$T_{CY}$ vs $V_{DD}$ (HS (high-speed main) mode)

— When the high-speed on-chip oscillator clock is selected
- - - During self programming
-·- When high-speed system clock is selected

**UART mode bit width (during communication at different potential) (reference)**



Remarks 1. R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

## 2.6  Analog Characteristics

### 2.6.1  A/D converter characteristics

Classification of A/D converter characteristics

| Input channel | Reference Voltage | | |
| --- | --- | --- | --- |
| | Reference voltage (+) = $AV_{REFP}$ <br> Reference voltage (−) = $AV_{REFM}$ | Reference voltage (+) = $V_{DD}$ <br> Reference voltage (−) = $V_{SS}$ | Reference voltage (+) = $V_{BGR}$ <br> Reference voltage (−) = $AV_{REFM}$ |
| ANI0 to ANI14 | Refer to **2.6.1 (1)**. | Refer to **2.6.1 (3)**. | Refer to **2.6.1 (4)**. |
| ANI16 to ANI26 | Refer to **2.6.1 (2)**. | | |
| Internal reference voltage <br> Temperature sensor output voltage | Refer to **2.6.1 (1)**. | | − |

**(1)  When reference voltage (+)= $AV_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage**

**($T_A$ = –40 to +85°C, 1.6 V $\leq AV_{REFP} \leq V_{DD} \leq$ 5.5 V, $V_{SS}$ = 0 V, Reference voltage (+) = $AV_{REFP}$, Reference voltage (−) = $AV_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution <br> $AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V $\leq AV_{REFP} \leq$ 5.5 V | | 1.2 | ±3.5 | LSB |
| | | | 1.6 V $\leq AV_{REFP} \leq$ 5.5 V [Note 4] | | 1.2 | ±7.0 | LSB |
| Conversion time | $t_{CONV}$ | 10-bit resolution <br> Target pin: ANI2 to ANI14 | 3.6 V $\leq V_{DD} \leq$ 5.5 V | 2.125 | | 39 | $\mu$s |
| | | | 2.7 V $\leq V_{DD} \leq$ 5.5 V | 3.1875 | | 39 | $\mu$s |
| | | | 1.8 V $\leq V_{DD} \leq$ 5.5 V | 17 | | 39 | $\mu$s |
| | | | 1.6 V $\leq V_{DD} \leq$ 5.5 V | 57 | | 95 | $\mu$s |
| | | 10-bit resolution <br> Target pin: Internal reference voltage, and temperature sensor output voltage <br> (HS (high-speed main) mode) | 3.6 V $\leq V_{DD} \leq$ 5.5 V | 2.375 | | 39 | $\mu$s |
| | | | 2.7 V $\leq V_{DD} \leq$ 5.5 V | 3.5625 | | 39 | $\mu$s |
| | | | 2.4 V $\leq V_{DD} \leq$ 5.5 V | 17 | | 39 | $\mu$s |
| Zero-scale error[Notes 1, 2] | $E_{ZS}$ | 10-bit resolution <br> $AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V $\leq AV_{REFP} \leq$ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V $\leq AV_{REFP} \leq$ 5.5 V [Note 4] | | | ±0.50 | %FSR |
| Full-scale error[Notes 1, 2] | $E_{FS}$ | 10-bit resolution <br> $AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V $\leq AV_{REFP} \leq$ 5.5 V | | | ±0.25 | %FSR |
| | | | 1.6 V $\leq AV_{REFP} \leq$ 5.5 V [Note 4] | | | ±0.50 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution <br> $AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V $\leq AV_{REFP} \leq$ 5.5 V | | | ±2.5 | LSB |
| | | | 1.6 V $\leq AV_{REFP} \leq$ 5.5 V [Note 4] | | | ±5.0 | LSB |
| Differential linearity error[Note 1] | DLE | 10-bit resolution <br> $AV_{REFP}$ = $V_{DD}$ [Note 3] | 1.8 V $\leq AV_{REFP} \leq$ 5.5 V | | | ±1.5 | LSB |
| | | | 1.6 V $\leq AV_{REFP} \leq$ 5.5 V [Note 4] | | | ±2.0 | LSB |
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI14 | | 0 | | $AV_{REFP}$ | V |
| | | Internal reference voltage <br> (2.4 V $\leq V_{DD} \leq$ 5.5 V, HS (high-speed main) mode) | | | $V_{BGR}$ [Note 5] | | V |
| | | Temperature sensor output voltage <br> (2.4 V $\leq V_{DD} \leq$ 5.5 V, HS (high-speed main) mode) | | | $V_{TMPS25}$ [Note 5] | | V |

(**Notes** are listed on the next page.)

**Notes 1.** Excludes quantization error ($\pm$1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.

Overall error: Add $\pm$1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add $\pm$0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add $\pm$0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

**4.** Values when the conversion time is set to 57 $\mu$s (min.) and 95 $\mu$s (max.).

**5.** Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**(4)  When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$[Note 3], Reference voltage (−) = AV$_{REFM}$ = 0 V[Note 4], HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | t$_{CONV}$ | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | 17 | | 39 | $\mu$s |
| Zero-scale error[Notes 1, 2] | E$_{ZS}$ | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error[Note 1] | ILE | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error[Note 1] | DLE | 8-bit resolution | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | V$_{AIN}$ | | | 0 | | V$_{BGR}$[Note 3] | V |

**Notes  1.**  Excludes quantization error (±1/2 LSB).

**2.**  This value is indicated as a ratio (%FSR) to the full-scale value.

**3.**  Refer to **2.6.2  Temperature sensor/internal reference voltage characteristics**.

**4.**  When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

## 2.8  Flash Memory Programming Characteristics

**(T$_A$ = –40 to +85°C, 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | f$_{CLK}$ | 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites<br>Notes 1, 2, 3 | C$_{erwr}$ | Retained for 20 years<br>T$_A$ = 85°C | 1,000 | | | Times |
| Number of data flash rewrites<br>Notes 1, 2, 3 | | Retained for 1 years<br>T$_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years<br>T$_A$ = 85°C | 100,000 | | | |
| | | Retained for 20 years<br>T$_A$ = 85°C | 10,000 | | | |

**Notes  1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

**2.** When using flash memory programmer and Renesas Electronics self programming library

**3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

## 2.9  Dedicated Flash Memory Programmer Communication (UART)

**(T$_A$ = –40 to +85°C, 1.8 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

# 3.  ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G:    Industrial applications $T_A$ = −40 to +105°C

R5F100xxGxx

**Cautions 1.    The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation.  Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed.  Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.**

**2.    With products not provided with an $EV_{DD0}$, $EV_{DD1}$, $EV_{SS0}$, or $EV_{SS1}$ pin, replace $EV_{DD0}$ and $EV_{DD1}$ with $V_{DD}$, or replace $EV_{SS0}$ and $EV_{SS1}$ with $V_{SS}$.**

**3.    The pins mounted depend on the product.  Refer to 2.1 Port Function to 2.2.1 Functions for each product.**

**4.    Please contact Renesas Electronics sales office for derating of operation under $T_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.**

**Remark**    When RL78/G13 is used in the range of $T_A$ = −40 to +85°C, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS ($T_A$ = −40 to +85°C)**.

There are following differences between the products "G: Industrial applications ($T_A$ = −40 to +105°C)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter | Application | |
|---|---|---|
| | A: Consumer applications, D: Industrial applications | G: Industrial applications |
| Operating ambient temperature | $T_A$ = -40 to +85°C | $T_A$ = -40 to +105°C |
| Operating mode Operating voltage range | HS (high-speed main) mode: 2.7 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 32 MHz 2.4 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 4 MHz | HS (high-speed main) mode only: 2.7 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 32 MHz 2.4 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 16 MHz |
| High-speed on-chip oscillator clock accuracy | 1.8 V $\leq V_{DD} \leq$ 5.5 V $\pm$1.0%@ $T_A$ = -20 to +85°C $\pm$1.5%@ $T_A$ = -40 to -20°C 1.6 V $\leq V_{DD} <$ 1.8 V $\pm$5.0%@ $T_A$ = -20 to +85°C $\pm$5.5%@ $T_A$ = -40 to -20°C | 2.4 V $\leq V_{DD} \leq$ 5.5 V $\pm$2.0%@ $T_A$ = +85 to +105°C $\pm$1.0%@ $T_A$ = -20 to +85°C $\pm$1.5%@ $T_A$ = -40 to -20°C |
| Serial array unit | UART CSI: $f_{CLK}$/2 (supporting 16 Mbps), $f_{CLK}$/4 Simplified $I^2C$ communication | UART CSI: $f_{CLK}$/4 Simplified $I^2C$ communication |
| IICA | Normal mode Fast mode Fast mode plus | Normal mode Fast mode |
| Voltage detector | Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels) | Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels) |

(**Remark** is listed on the next page.)

**(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | V$_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA | EV$_{DD0}$ − 0.7 | | | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA | EV$_{DD0}$ − 0.6 | | | V |
| | | | 2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA | EV$_{DD0}$ − 0.5 | | | V |
| | V$_{OH2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 μA | V$_{DD}$ − 0.5 | | | V |
| Output voltage, low | V$_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | V$_{OL2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 μA | | | 0.4 | V |
| | V$_{OL3}$ | P60 to P63 | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution**  **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**5.** The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\ V \leq EV_{DD0} < 3.3\ V$ and $1.6\ V \leq V_b \leq 2.0\ V$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1-\frac{1.5}{V_b})\} \times 3}\ [bps]$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1-\frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100\ [\%]$$

*  This value is the theoretical value of the relative difference between the transmission and reception sides.

**6.** This value as an example is calculated when the conditions described in the "Conditions" column are met.  Refer to Note 5 above to calculate the maximum transfer rate under conditions of the customer.

**Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**
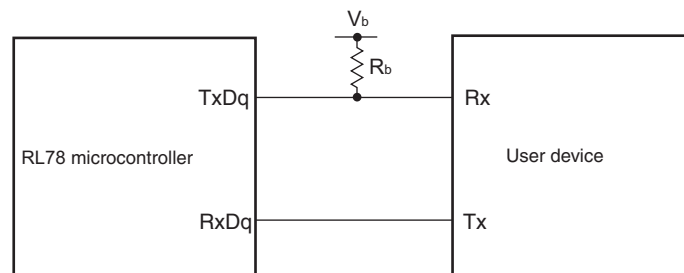
**(7)  Communication at different potential (1.8 V, 2.5 V, 3 V)  (CSI mode) (slave mode, SCKp... external clock input)**

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time [Note 1] | t$_{KCY2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | 24 MHz < f$_{MCK}$ | 28/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 24/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 20 MHz | 20/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 16/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 12/f$_{MCK}$ | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | 24 MHz < f$_{MCK}$ | 40/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 32/f$_{MCK}$ | | ns |
| | | | 16 MHz < f$_{MCK}$ ≤ 20 MHz | 28/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 16 MHz | 24/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 16/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 12/f$_{MCK}$ | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V | 24 MHz < f$_{MCK}$ | 96/f$_{MCK}$ | | ns |
| | | | 20 MHz < f$_{MCK}$ ≤ 24 MHz | 72/f$_{MCK}$ | | ns |
| | | | 16 MHz < f$_{MCK}$ ≤ 20 MHz | 64/f$_{MCK}$ | | ns |
| | | | 8 MHz < f$_{MCK}$ ≤ 16 MHz | 52/f$_{MCK}$ | | ns |
| | | | 4 MHz < f$_{MCK}$ ≤ 8 MHz | 32/f$_{MCK}$ | | ns |
| | | | f$_{MCK}$ ≤ 4 MHz | 20/f$_{MCK}$ | | ns |
| SCKp high-/low-level width | t$_{KH2}$, t$_{KL2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | | t$_{KCY2}$/2 − 24 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | | t$_{KCY2}$/2 − 36 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2] | | t$_{KCY2}$/2 − 100 | | ns |
| SIp setup time (to SCKp↑) [Note 2] | t$_{SIK2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V | | 1/f$_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V | | 1/f$_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V | | 1/f$_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) [Note 3] | t$_{KSI2}$ | | | 1/f$_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output [Note 4] | t$_{KSO2}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ | | | 2/f$_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ | | | 2/f$_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ | | | 2/f$_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26**

**(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | 8 | | 10 | bit |
| Overall error[Note 1] | AINL | 10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4] | 2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V | | 1.2 | ±5.0 | LSB |
| Conversion time | t$_{CONV}$ | 10-bit resolution Target pin : ANI16 to ANI26 | 3.6 V ≤ V$_{DD}$ ≤ 5.5 V | 2.125 | | 39 | $\mu$s |
| | | | 2.7 V ≤ V$_{DD}$ ≤ 5.5 V | 3.1875 | | 39 | $\mu$s |
| | | | 2.4 V ≤ V$_{DD}$ ≤ 5.5 V | 17 | | 39 | $\mu$s |
| Zero-scale error[Notes 1, 2] | E$_{ZS}$ | 10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4] | 2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Full-scale error[Notes 1, 2] | E$_{FS}$ | 10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4] | 2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V | | | ±0.35 | %FSR |
| Integral linearity error[Note 1] | ILE | 10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4] | 2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V | | | ±3.5 | LSB |
| Differential linearity error [Note 1] | DLE | 10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4] | 2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Analog input voltage | V$_{AIN}$ | ANI16 to ANI26 | | 0 | | AV$_{REFP}$ and EV$_{DD0}$ | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

**4.** When AV$_{REFP}$ < EV$_{DD0}$ ≤ V$_{DD}$, the MAX. values are as follows.

Overall error: Add ±4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

## 3.8 Flash Memory Programming Characteristics

**(T$_A$ = –40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CPU/peripheral hardware clock frequency | f$_{CLK}$ | 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V | 1 | | 32 | MHz |
| Number of code flash rewrites **Notes 1,2,3** | C$_{erwr}$ | Retained for 20 years T$_A$ = 85°C **Note 4** | 1,000 | | | Times |
| Number of data flash rewrites **Notes 1,2,3** | | Retained for 1 years T$_A$ = 25°C | | 1,000,000 | | |
| | | Retained for 5 years T$_A$ = 85°C **Note 4** | 100,000 | | | |
| | | Retained for 20 years T$_A$ = 85°C **Note 4** | 10,000 | | | |

**Notes 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.The retaining years are until next rewrite after the rewrite.

    **2.** When using flash memory programmer and Renesas Electronics self programming library.

    **3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

    **4.** This temperature is the average value at which data are retained.

## 3.9 Dedicated Flash Memory Programmer Communication (UART)

**(T$_A$ = –40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Transfer rate | | During serial programming | 115,200 | | 1,000,000 | bps |

### 3.10  Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | t$_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | t$_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | | $\mu$s |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | t$_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |
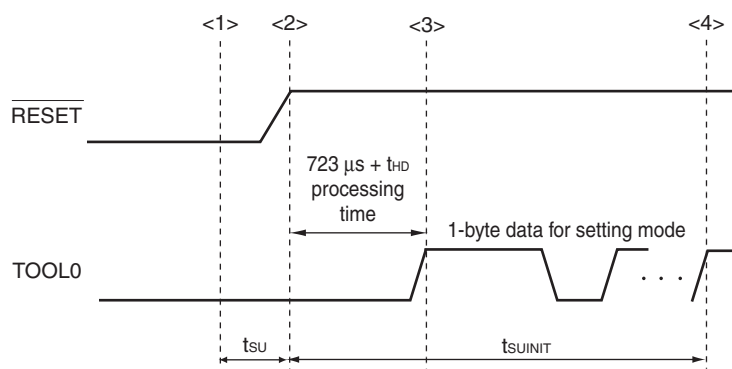


<1>  The low level is input to the TOOL0 pin.

<2>  The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3>  The TOOL0 pin is set to the high level.

<4>  Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark  t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t$_{SU}$:    Time to release the external reset after the TOOL0 pin is set to the low level

t$_{HD}$:    Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)