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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	82
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	20K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 20x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100pjafa-v0

Table 1-1. List of Ordering Part Numbers

(1/12)

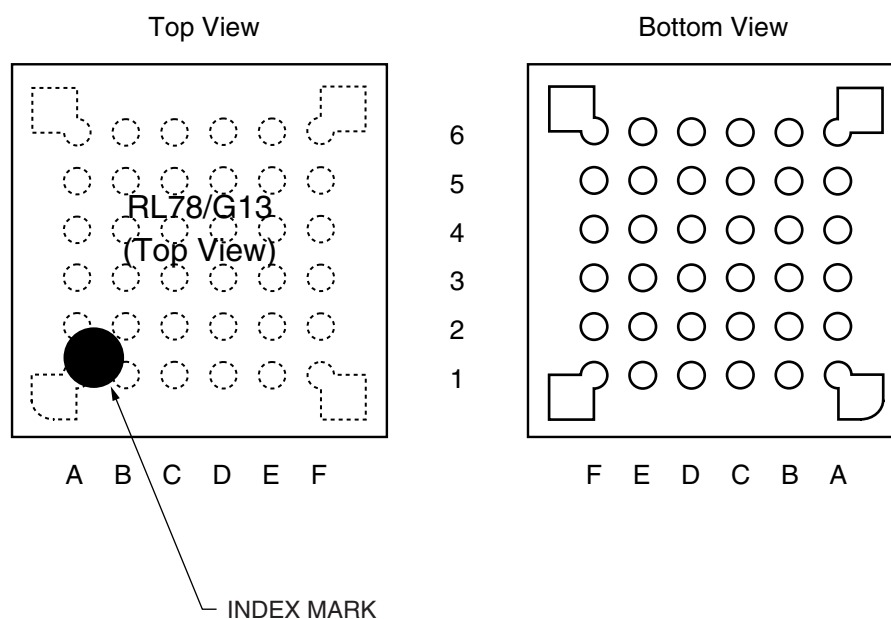
Pin count	Package	Data flash	Fields of Application ^{Note}	Ordering Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0 R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0 R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0 R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0
		Not mounted	A	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0 R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0 R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0
			G	R5F1016AGSP#V0, R5F1016CGSP#V0, R5F1016DGSP#V0, R5F1016EGSP#V0 R5F1016AGSP#X0, R5F1016CGSP#X0, R5F1016DGSP#X0, R5F1016EGSP#X0
24 pins	24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch)	Mounted	A	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0 R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0 R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0 R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0
		Not mounted	A	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0 R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0 R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0
			G	R5F1017AGNA#U0, R5F1017CGNA#U0, R5F1017DGNA#U0, R5F1017EGNA#U0 R5F1017AGNA#W0, R5F1017CGNA#W0, R5F1017DGNA#W0, R5F1017EGNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



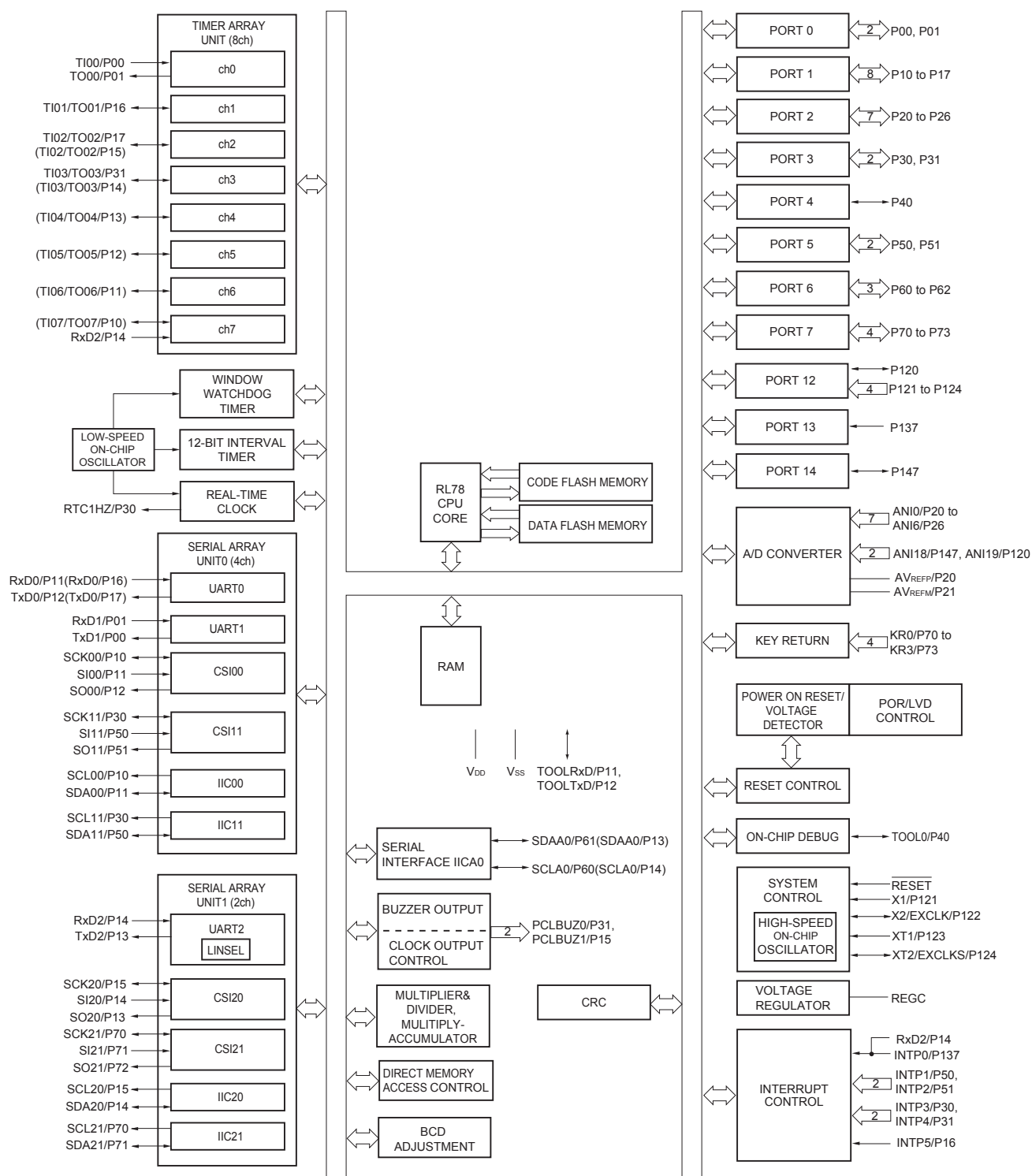
	A	B	C	D	E	F	
6	P60/SCLA0	V _{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V _{SS}	REGC	RESET	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV _{REFP}	P21/ANI1/ AV _{REFM}	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.7 40-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.6 Outline of Functions

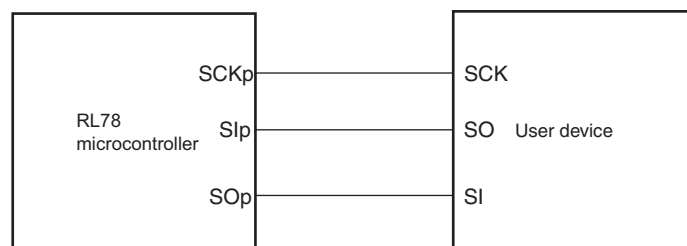
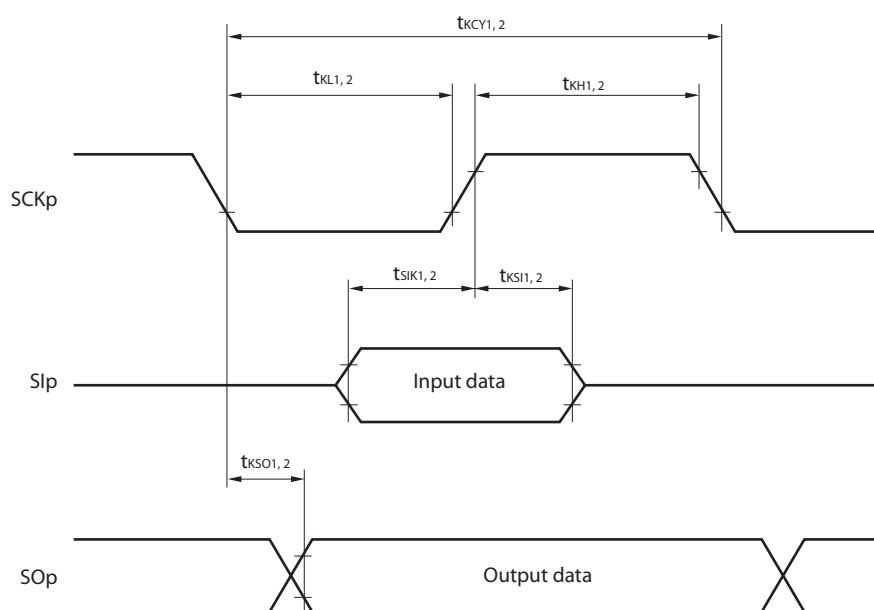
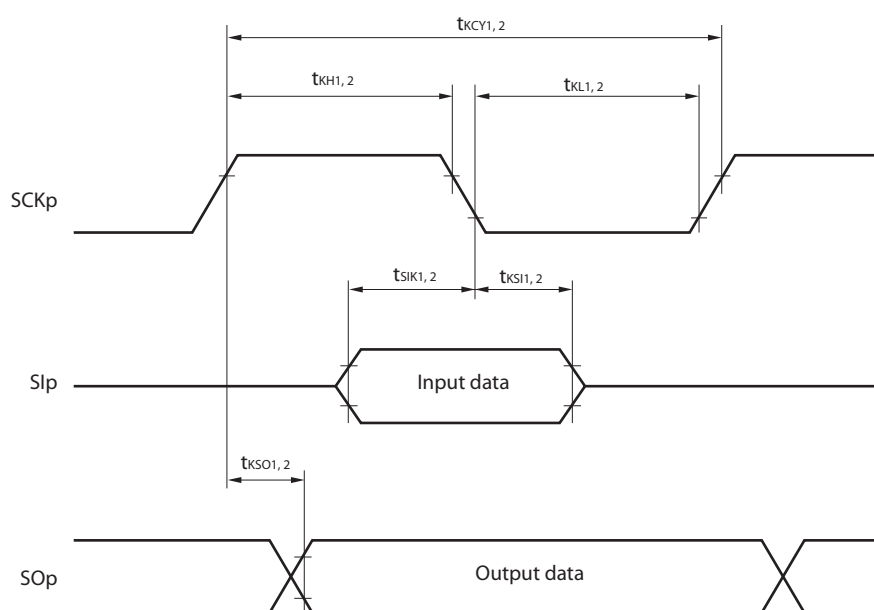
[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4 ^{Note1}		2 to 4 ^{Note1}		2 to 4 ^{Note1}		2 to 12 ^{Note1}		2 to 12 ^{Note1}		2 to 12 ^{Note1}	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation)											
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)											
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.											
I/O port	Total	16	20	21	26	28	32						
	CMOS I/O	13 (N-ch O.D. I/O [V _{DD} withstand voltage]: 5)	15 (N-ch O.D. I/O [V _{DD} withstand voltage]: 6)	15 (N-ch O.D. I/O [V _{DD} withstand voltage]: 6)	21 (N-ch O.D. I/O [V _{DD} withstand voltage]: 9)	22 (N-ch O.D. I/O [V _{DD} withstand voltage]: 9)	26 (N-ch O.D. I/O [V _{DD} withstand voltage]: 10)						
	CMOS input	3	3	3	3	3	3						
	CMOS output	–	–	1	–	–	–						
	N-ch O.D. I/O (withstand voltage: 6 V)	–	2	2	2	3	3						
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel ^{Note 2}											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2 ^{Note 3})	4 channels (PWM outputs: 3 ^{Note 3})				4 channels (PWM outputs: 3 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4}						
	RTC output	–											

- Notes**
- The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.
 - Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f_{IL}) is selected

CSI mode connection diagram (during communication at same potential)**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)****CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

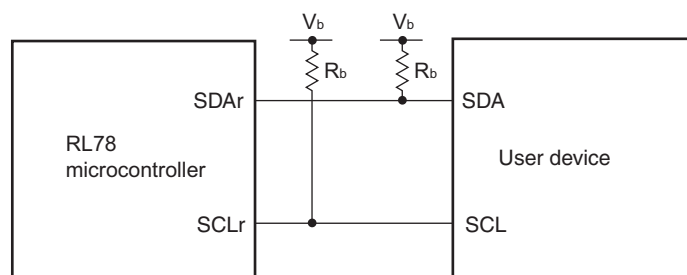
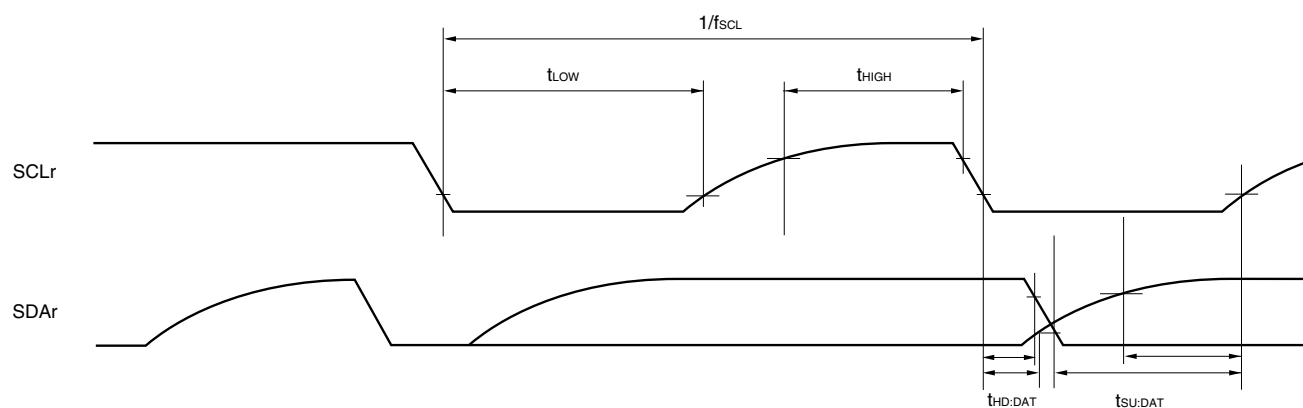
(5) During communication at same potential (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

- Remarks**
1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

2.5.2 Serial interface IICA

(1) I²C standard mode(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Hold time when SCLA0 = “L”	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	
Hold time when SCLA0 = “H”	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	250		250		250		ns	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		250		250		ns	
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		0	3.45	0	3.45	μs	
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.0		4.0		μs	
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EV _{DD0} ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EV _{DD0} ≤ 5.5 V	—		4.7		4.7		μs	

(Notes, Caution and Remark are listed on the next page.)

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM} = 0 V^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C_{erwr}	Retained for 20 years $T_A = 85^\circ\text{C}$	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

Absolute Maximum Ratings ($T_A = 25^{\circ}\text{C}$) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I _{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
	Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
I _{OL2}		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T _A	In normal operation mode		−40 to +105
	In flash memory programming mode				
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

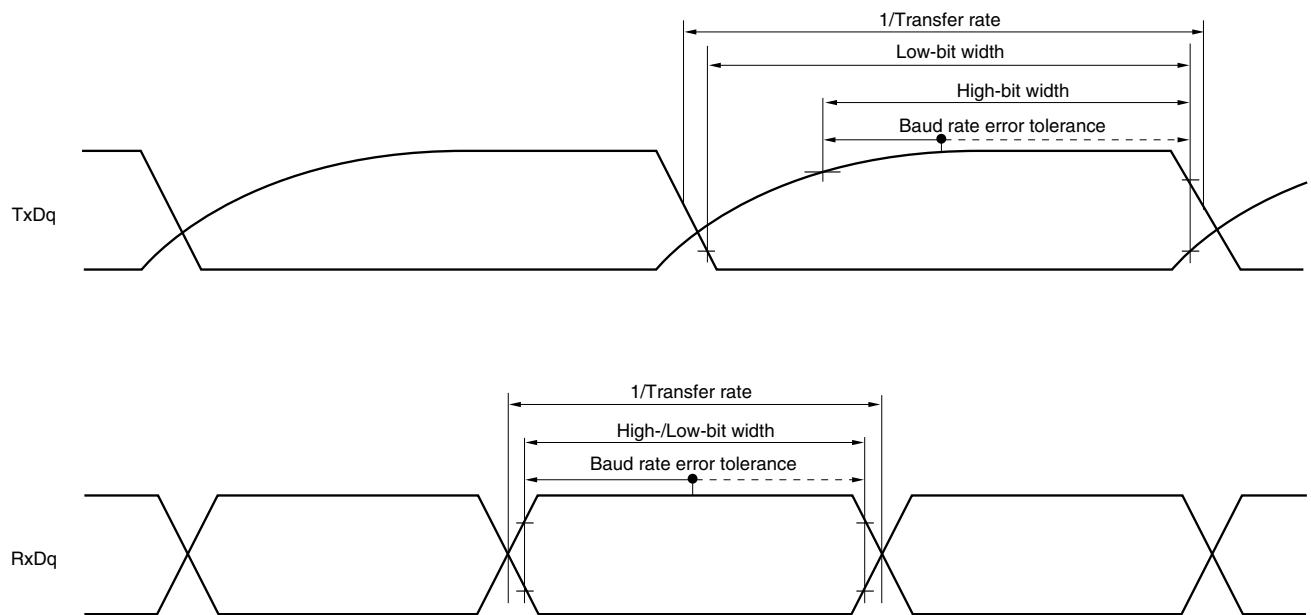
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$) (1/2)

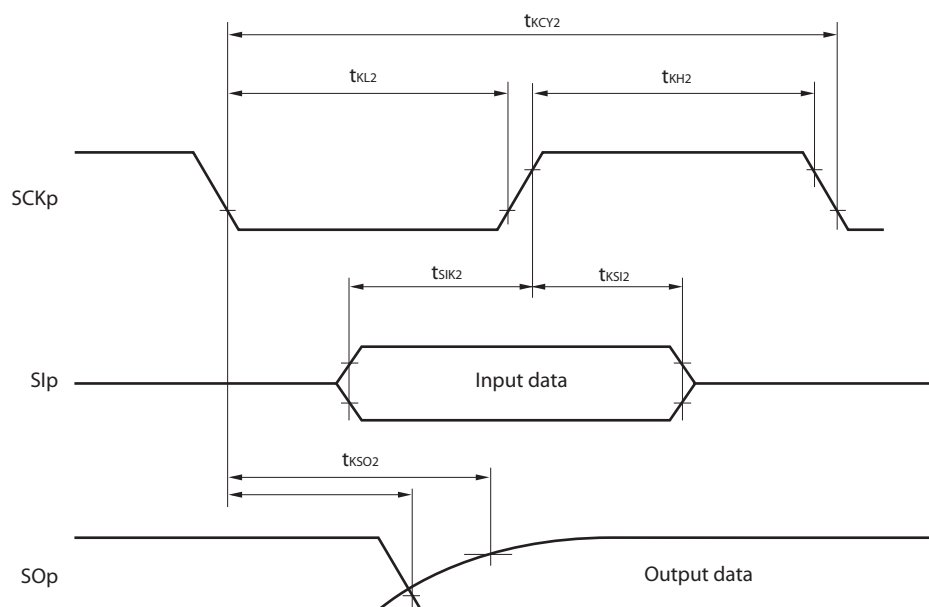
Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	$f_{\text{IH}} = 32\text{ MHz}$ Note 3	Basic operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		2.3		mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		2.3		mA
					Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		5.2	9.2	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		5.2	9.2	mA
				$f_{\text{IH}} = 24\text{ MHz}$ Note 3	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		4.1	7.0	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		4.1	7.0	mA
				$f_{\text{IH}} = 16\text{ MHz}$ Note 3	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		3.0	5.0	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		3.0	5.0	mA
			HS (high-speed main) mode Note 5	$f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				$f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				$f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
				$f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
		Subsystem clock operation		$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		10.0	46.0	μA
						Resonator connection		10.0	46.0	μA

(Notes and Remarks are listed on the next page.)

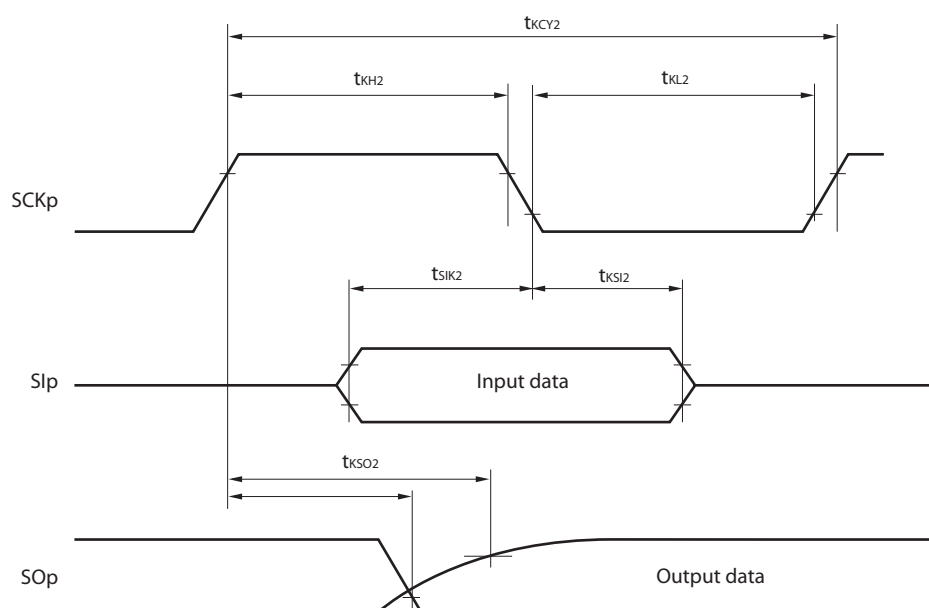
UART mode bit width (during communication at different potential) (reference)

- Remarks**
1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



- Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
 n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- 2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
 Use other CSI for communication at different potential.

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{BGR} ^{Note 3}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)		V_{TMPS25} ^{Note 3}			V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

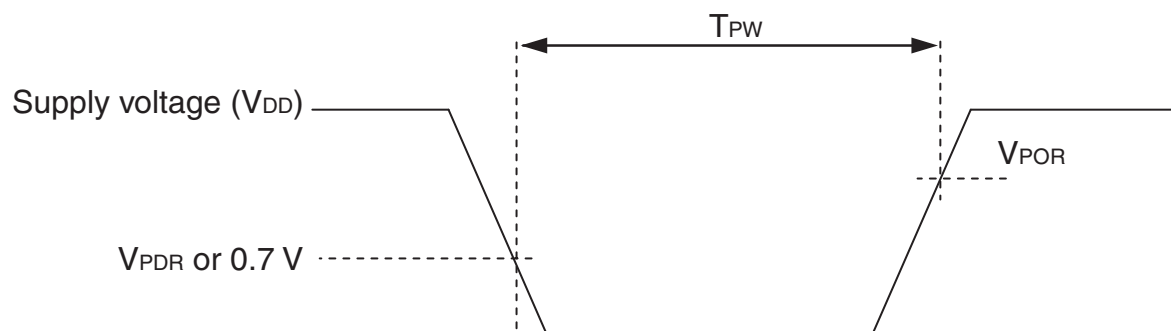
3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

3.6.3 POR circuit characteristics

 $(T_A = -40$ to $+105^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.45	1.51	1.57	V
	V_{PDR}	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T_{PW}		300			μs

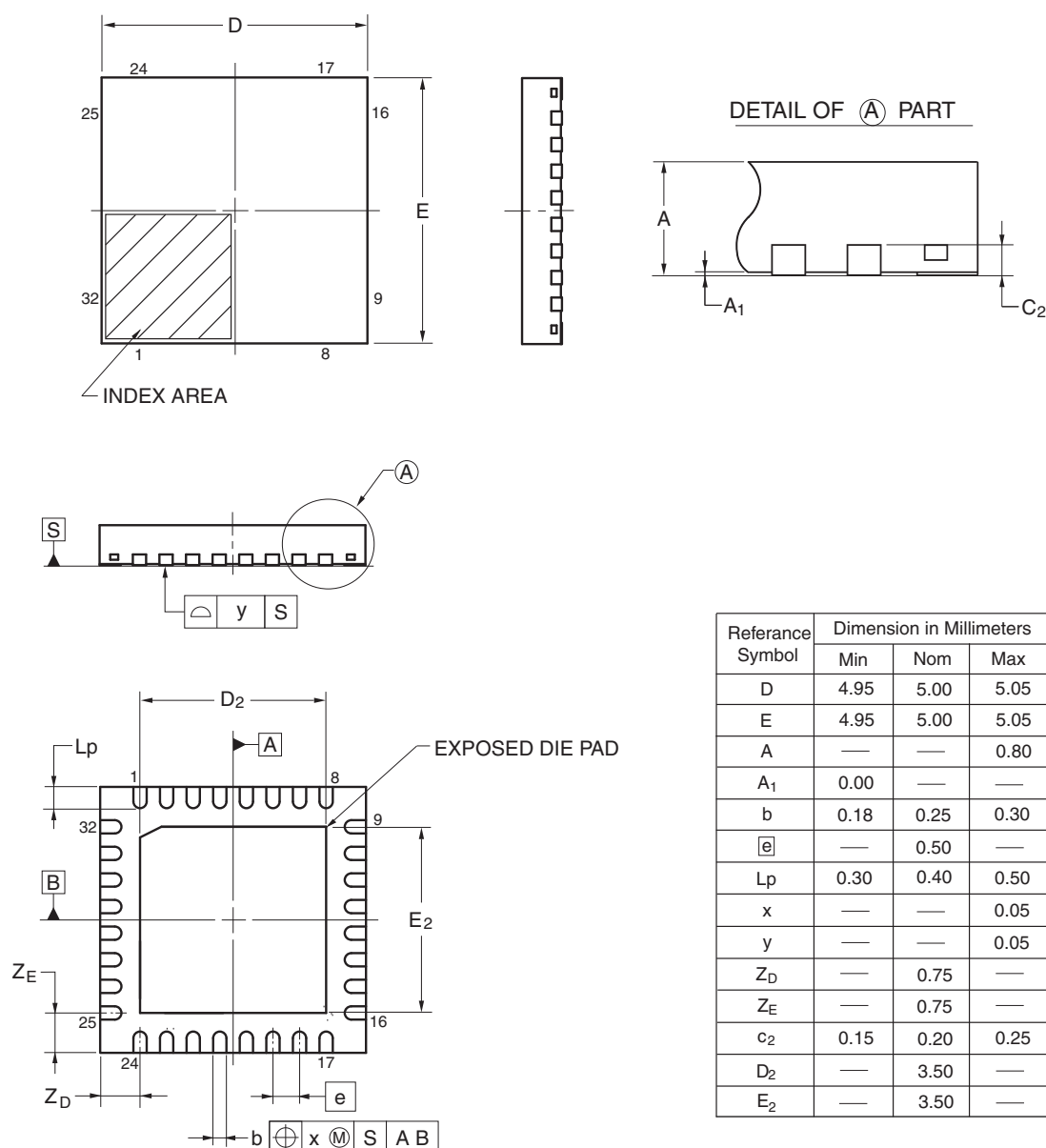
Note Minimum time required for a POR reset when V_{DD} exceeds below V_{PDR} . This is also the minimum time required for a POR reset from when V_{DD} exceeds below 0.7 V to when V_{DD} exceeds V_{POR} while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

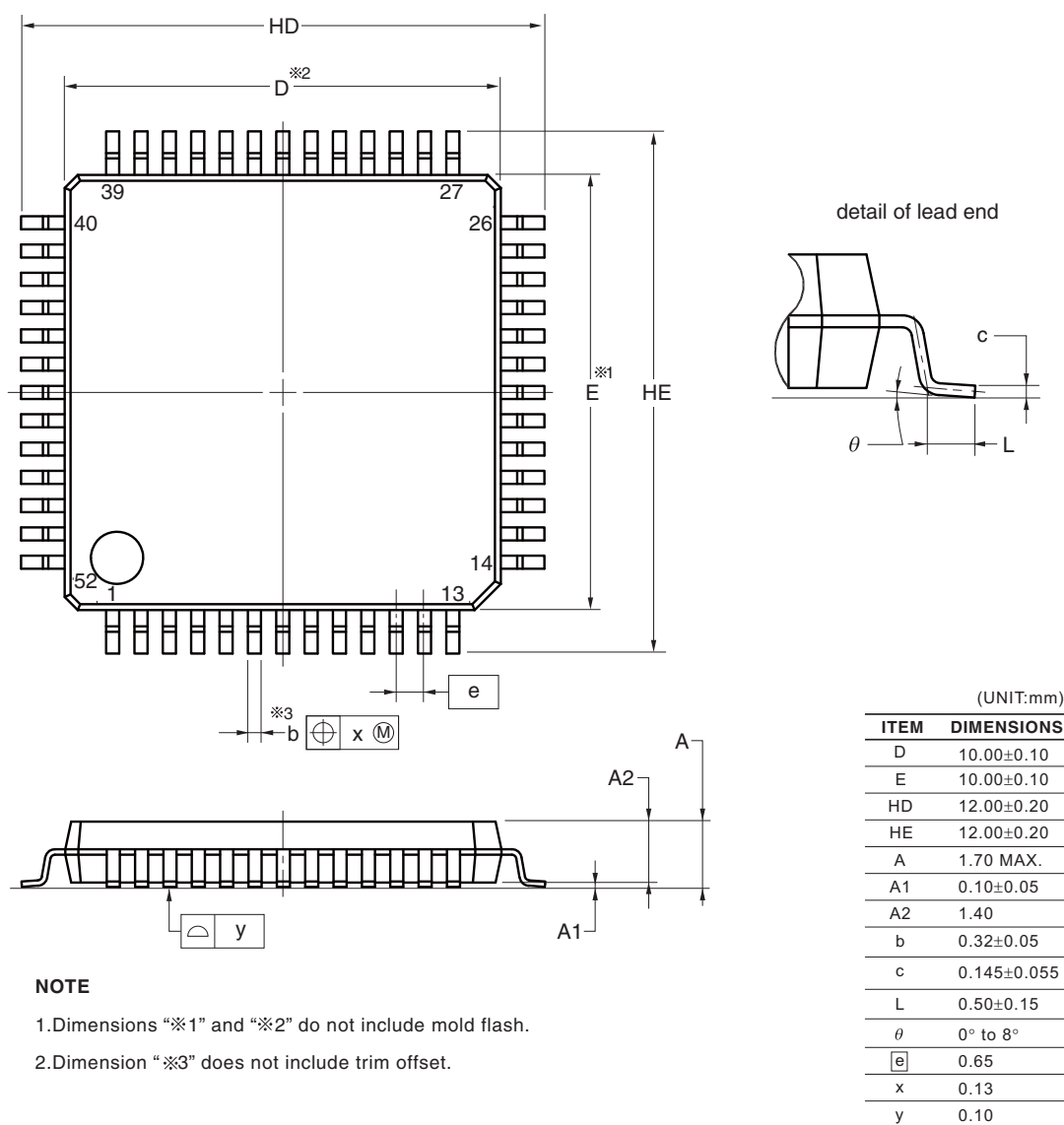


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4.10 52-pin Products

R5F100JCAFA, R5F100JDFA, R5F100JEFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFA, R5F100JKFA, R5F100JLAFA
 R5F101JCAFA, R5F101JDFA, R5F101JEFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFA, R5F101JKFA, R5F101JLAFA
 R5F100JCDA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDA, R5F100JDDFA, R5F100JKDA, R5F100JLDA
 R5F101JCDA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDA, R5F101JDDFA, R5F101JKDA, R5F101JLDA
 R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



NOTE

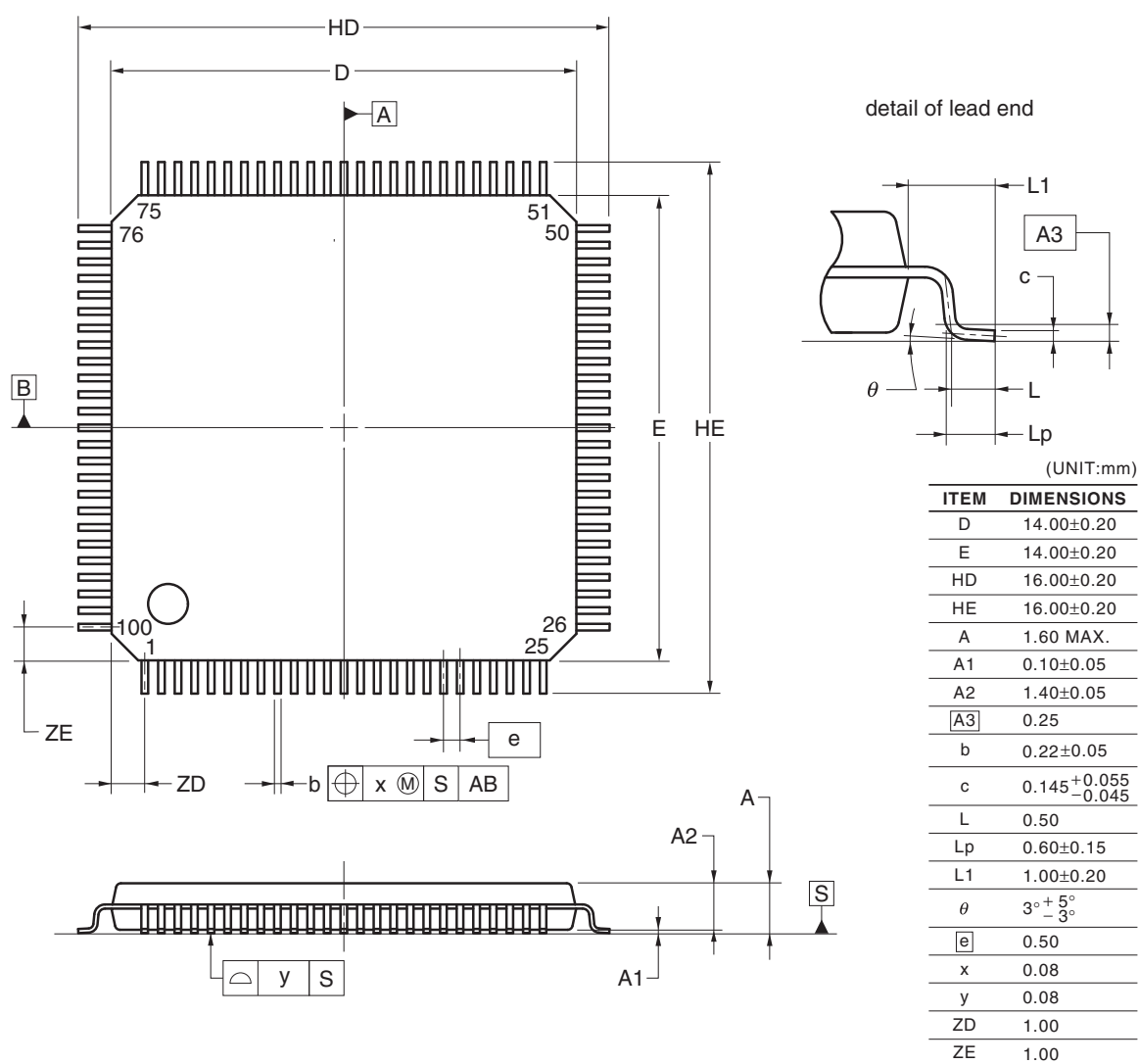
- Dimensions "※1" and "※2" do not include mold flash.
- Dimension "※3" does not include trim offset.

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4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFB, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDDB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
 R5F101PFDDB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	163	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		164, 165	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		166	Modification of table in 3.5.2 Serial interface IICA
		166	Modification of IICA serial transfer timing
		167	Addition of table in 3.6.1 A/D converter characteristics
		167, 168	Modification of table and notes 3 and 4 in 3.6.1 (1)
		169	Modification of description in 3.6.1 (2)
		170	Modification of description and note 3 in 3.6.1 (3)
		171	Modification of description and notes 3 and 4 in 3.6.1 (4)
		172	Modification of table and note in 3.6.3 POR circuit characteristics
		173	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		173	Modification from Supply Voltage Rise Time to 3.6.5 Power supply voltage rising slope characteristics
		174	Modification of 3.9 Dedicated Flash Memory Programmer Communication (UART)
		175	Modification of table, figure, and remark in 3.10 Timing Specs for Switching Flash Memory Programming Modes
3.10	Nov 15, 2013	123	Caution 4 added.
		125	Note for operating ambient temperature in 3.1 Absolute Maximum Ratings deleted.
3.30	Mar 31, 2016		Modification of the position of the index mark in 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch) of 1.3.3 25-pin products
			Modification of power supply voltage in 1.6 Outline of Functions [20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]
			Modification of power supply voltage in 1.6 Outline of Functions [80-pin, 100-pin, 128-pin products]
			$\overline{\text{ACK}}$ corrected to ACK
			$\overline{\text{ACK}}$ corrected to ACK

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