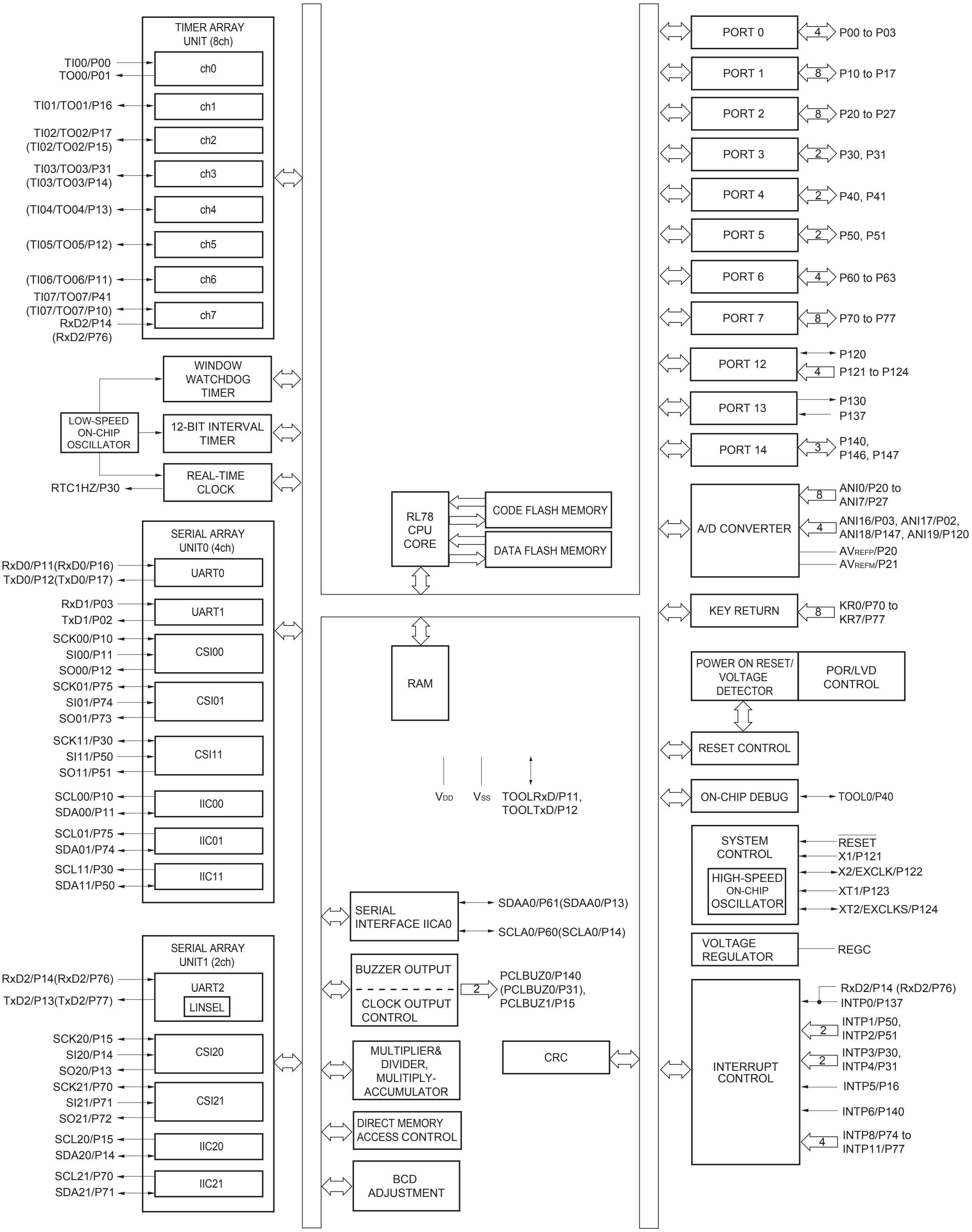
# Renesas Electronics America Inc - R5F100SHAFB#V0 Datasheet

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 110 |
| Program Memory Size | 192KB (192K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 8K x 8 |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 26x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-LQFP |
| Supplier Device Package | 128-LFQFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100shafb-v0 |

### 1.5.10 52-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[80-pin, 100-pin, 128-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 80-pin | | 100-pin | | 128-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Code flash memory (KB) | | 96 to 512 | | 96 to 512 | | 192 to 512 | |
| Data flash memory (KB) | | 8 | – | 8 | – | 8 | – |
| RAM (KB) | | 8 to 32 Note 1 | | 8 to 32 Note 1 | | 16 to 32 Note 1 | |
| Address space | | 1 MB | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 74 | | 92 | | 120 | |
| | CMOS I/O | 64<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 21) | | 82<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 24) | | 110<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 25) | |
| | CMOS input | 5 | | 5 | | 5 | |
| | CMOS output | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 12 channels | | 12 channels | | 16 channels | |
| | Watchdog timer | 1 channel | | 1 channel | | 1 channel | |
| | Real-time clock (RTC) | 1 channel | | 1 channel | | 1 channel | |
| | 12-bit interval timer (IT) | 1 channel | | 1 channel | | 1 channel | |
| | Timer output | 12 channels<br>(PWM outputs: 10 Note 2) | | 12 channels<br>(PWM outputs: 10 Note 2) | | 16 channels<br>(PWM outputs: 14 Note 2) | |
| | RTC output | 1 channel<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H
R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (3/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Input voltage, high | $V_{IH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0.8$EV_{DD0}$ | | $EV_{DD0}$ | V |
| | $V_{IH2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer<br>4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 2.2 | | $EV_{DD0}$ | V |
| | | | TTL input buffer<br>3.3 V ≤ $EV_{DD0}$ < 4.0 V | 2.0 | | $EV_{DD0}$ | V |
| | | | TTL input buffer<br>1.6 V ≤ $EV_{DD0}$ < 3.3 V | 1.5 | | $EV_{DD0}$ | V |
| | $V_{IH3}$ | P20 to P27, P150 to P156 | | 0.7$V_{DD}$ | | $V_{DD}$ | V |
| | $V_{IH4}$ | P60 to P63 | | 0.7$EV_{DD0}$ | | 6.0 | V |
| | $V_{IH5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0.8$V_{DD}$ | | $V_{DD}$ | V |
| Input voltage, low | $V_{IL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | Normal input buffer | 0 | | 0.2$EV_{DD0}$ | V |
| | $V_{IL2}$ | P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143 | TTL input buffer<br>4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 0 | | 0.8 | V |
| | | | TTL input buffer<br>3.3 V ≤ $EV_{DD0}$ < 4.0 V | 0 | | 0.5 | V |
| | | | TTL input buffer<br>1.6 V ≤ $EV_{DD0}$ < 3.3 V | 0 | | 0.32 | V |
| | $V_{IL3}$ | P20 to P27, P150 to P156 | | 0 | | 0.3$V_{DD}$ | V |
| | $V_{IL4}$ | P60 to P63 | | 0 | | 0.3$EV_{DD0}$ | V |
| | $V_{IL5}$ | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$ | | 0 | | 0.2$V_{DD}$ | V |

**Caution The maximum value of $V_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is $EV_{DD0}$, even in the N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –10.0 mA | $EV_{DD0}$ – 1.5 | | | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $EV_{DD0}$ – 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $EV_{DD0}$ – 0.6 | | | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $EV_{DD0}$ – 0.5 | | | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OH1}$ = –1.0 mA | $EV_{DD0}$ – 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = –100 $\mu$A | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 20 mA | | | 1.3 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OL1}$ = 0.3 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 $\mu$A | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |
| | | | 1.6 V ≤ $EV_{DD0}$ < 5.5 V, $I_{OL3}$ = 1.0 mA | | | 0.4 | V |

**Caution** **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

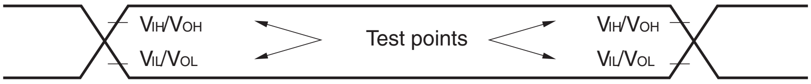
**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

## 2.5 Peripheral Functions Characteristics

**AC Timing Test Points**



### 2.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**
**($T_A$ = −40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate Note 1 | | 2.4 V≤ $EV_{DD0}$ ≤ 5.5 V | | | $f_{MCK}/6$ Note 2 | | $f_{MCK}/6$ | | $f_{MCK}/6$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.8 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | $f_{MCK}/6$ Note 2 | | $f_{MCK}/6$ | | $f_{MCK}/6$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | | $f_{MCK}/6$ Note 2 | | $f_{MCK}/6$ Note 2 | | $f_{MCK}/6$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | 1.6 V ≤ $EV_{DD0}$ ≤ 5.5 V | | — | | | $f_{MCK}/6$ Note 2 | | $f_{MCK}/6$ | bps |
| | | | Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$ Note 3 | — | | | 1.3 | | 0.6 | Mbps |

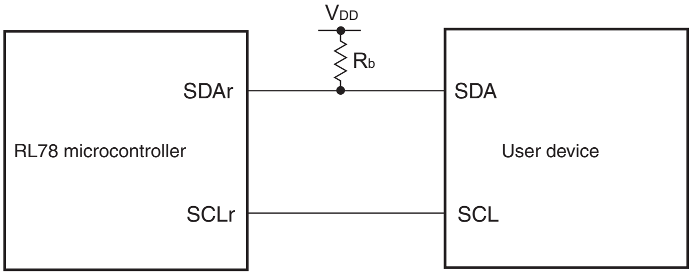
**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The following conditions are required for low voltage interface when $E_{VDD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps
1.6 V ≤ $EV_{DD0}$ < 1.8 V : MAX. 0.6 Mbps

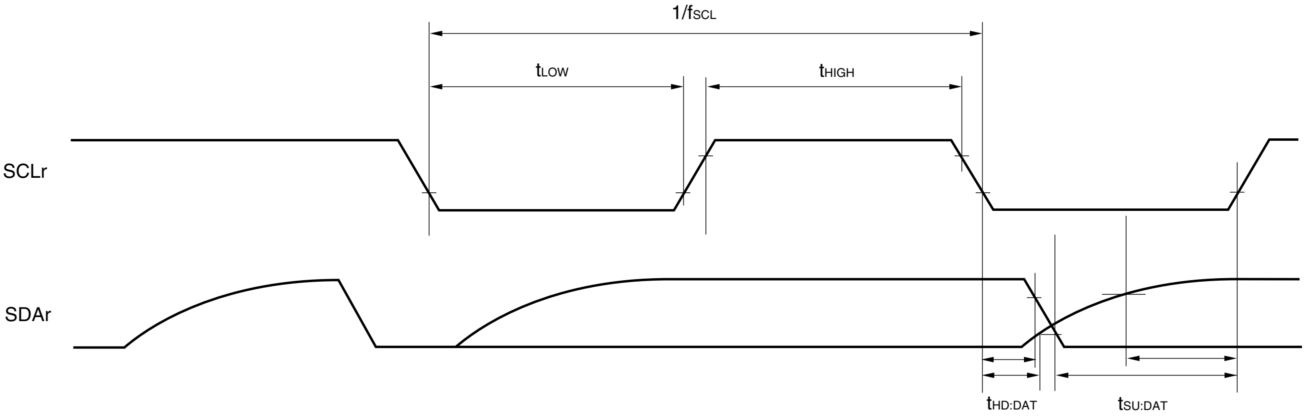
**3.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V)
16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V)
LS (low-speed main) mode: 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V)
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V)

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Simplified I²C mode mode connection diagram (during communication at same potential)**



**Simplified I²C mode serial transfer timing (during communication at same potential)**



**Remarks 1.** $R_b$[Ω]:Communication line (SDAr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance

**2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

### (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

**($T_A$ = −40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Transfer rate | | Reception | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V | | | $f_{MCK}/6$<br>Note 1 | | $f_{MCK}/6$<br>Note 1 | | $f_{MCK}/6$<br>Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V | | | $f_{MCK}/6$<br>Note 1 | | $f_{MCK}/6$<br>Note 1 | | $f_{MCK}/6$<br>Note 1 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |
| | | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V | | | $f_{MCK}/6$<br>Notes 1 to 3 | | $f_{MCK}/6$<br>Notes 1, 2 | | $f_{MCK}/6$<br>Notes 1, 2 | bps |
| | | | | Theoretical value of the maximum transfer rate<br>$f_{MCK}$ = $f_{CLK}$ Note 4 | | 5.3 | | 1.3 | | 0.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** Use it with $EV_{DD0} \geq V_b$.

**3.** The following conditions are required for low voltage interface when $E_{VDD0}$ < $V_{DD}$.
2.4 V ≤ $EV_{DD0}$ < 2.7 V : MAX. 2.6 Mbps
1.8 V ≤ $EV_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

**4.** The maximum operating frequencies of the CPU/peripheral hardware clock ($f_{CLK}$) are:

| | |
|---|---|
| HS (high-speed main) mode: | 32 MHz (2.7 V ≤ $V_{DD}$ ≤ 5.5 V) |
| | 16 MHz (2.4 V ≤ $V_{DD}$ ≤ 5.5 V) |
| LS (low-speed main) mode: | 8 MHz (1.8 V ≤ $V_{DD}$ ≤ 5.5 V) |
| LV (low-voltage main) mode: | 4 MHz (1.6 V ≤ $V_{DD}$ ≤ 5.5 V) |

**Caution** **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $V_b$[V]: Communication line voltage

**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**3.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ $EV_{DD0}$ < 4.0 V and 2.3 V ≤ $V_b$ ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ $EV_{DD0}$ < 3.3 V and 1.6 V ≤ $V_b$ ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

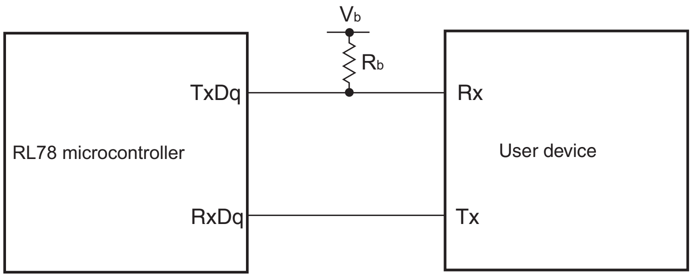
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

**7.** This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**



### (2) $I^2C$ fast mode

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLA0 clock frequency | $f_{SCL}$ | Fast mode: $f_{CLK} \geq 3.5$ MHz | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| | | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | 0 | 400 | 0 | 400 | 0 | 400 | kHz |
| Setup time of restart condition | $t_{SU:STA}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| Hold time[Note 1] | $t_{HD:STA}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| Hold time when SCLA0 = "L" | $t_{LOW}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 1.3 | | 1.3 | | 1.3 | | μs |
| Hold time when SCLA0 = "H" | $t_{HIGH}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| Data setup time (reception) | $t_{SU:DAT}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 100 | | 100 | | 100 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 100 | | 100 | | 100 | | μs |
| Data hold time (transmission)[Note 2] | $t_{HD:DAT}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0 | 0.9 | 0 | 0.9 | 0 | 0.9 | μs |
| Setup time of stop condition | $t_{SU:STO}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 0.6 | | 0.6 | | 0.6 | | μs |
| Bus-free time | $t_{BUF}$ | $2.7\ V \leq EV_{DD0} \leq 5.5\ V$ | | 1.3 | | 1.3 | | 1.3 | | μs |
| | | $1.8\ V \leq EV_{DD0} \leq 5.5\ V$ | | 1.3 | | 1.3 | | 1.3 | | μs |

**Notes 1.** The first clock pulse is generated after this period when the start/restart condition is detected.

<R> **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics ($I_{OH1}$, $I_{OL1}$, $V_{OH1}$, $V_{OL1}$) must satisfy the values in the redirect destination.**

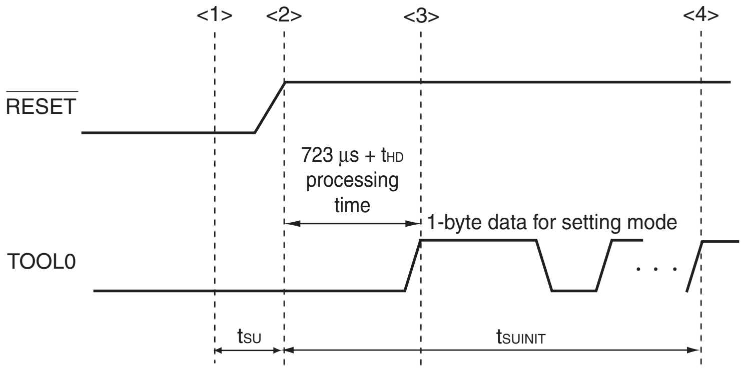
**Remark** The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: $C_b$ = 320 pF, $R_b$ = 1.1 kΩ

## 2.10 Timing of Entry to Flash Memory Programming Modes

**($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Time to complete the communication for the initial setting after the external reset is released | $t_{SUINIT}$ | POR and LVD reset must be released before the external reset is released. | | | 100 | ms |
| Time to release the external reset after the TOOL0 pin is set to the low level | $t_{SU}$ | POR and LVD reset must be released before the external reset is released. | 10 | | | μs |
| Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory) | $t_{HD}$ | POR and LVD reset must be released before the external reset is released. | 1 | | | ms |



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** $t_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

$t_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

$t_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

**Absolute Maximum Ratings ($T_A$ = 25°C) (2/2)**

| Parameter | Symbols | Conditions | | Ratings | Unit |
|---|---|---|---|---|---|
| Output current, high | $I_{OH1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | −40 | mA |
| | | Total of all pins<br>−170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | −70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | −100 | mA |
| | $I_{OH2}$ | Per pin | P20 to P27, P150 to P156 | −0.5 | mA |
| | | Total of all pins | | −2 | mA |
| Output current, low | $I_{OL1}$ | Per pin | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 40 | mA |
| | | Total of all pins<br>170 mA | P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 | 70 | mA |
| | | | P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 | 100 | mA |
| | $I_{OL2}$ | Per pin | P20 to P27, P150 to P156 | 1 | mA |
| | | Total of all pins | | 5 | mA |
| Operating ambient temperature | $T_A$ | In normal operation mode | | −40 to +105 | °C |
| | | In flash memory programming mode | | | |
| Storage temperature | $T_{stg}$ | | | −65 to +150 | °C |

**Caution** **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

### (4) During communication at same potential (simplified $I^2C$ mode)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SCLr clock frequency | $f_{SCL}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | | 400 Note1 | kHz |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | | 100 Note1 | kHz |
| Hold time when SCLr = “L” | $t_{LOW}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Hold time when SCLr = “H” | $t_{HIGH}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1200 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 4600 | | ns |
| Data setup time (reception) | $t_{SU:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 220 Note2 | | ns |
| | | 2.4 V ≤ $EV_{DD}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 1/$f_{MCK}$ + 580 Note2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>$C_b$ = 100 pF, $R_b$ = 3 kΩ | 0 | 1420 | ns |

**Notes** **1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the normal input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

### (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Data setup time (reception) | $t_{SU:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 340 Note 2 | | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 1/$f_{MCK}$ + 760 Note 2 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V,<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 1/$f_{MCK}$ + 570 Note 2 | | ns |
| Data hold time (transmission) | $t_{HD:DAT}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 50 pF, $R_b$ = 2.7 kΩ | 0 | 770 | ns |
| | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V,<br>2.7 V ≤ $V_b$ ≤ 4.0 V,<br>$C_b$ = 100 pF, $R_b$ = 2.8 kΩ | 0 | 1420 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V,<br>2.3 V ≤ $V_b$ ≤ 2.7 V,<br>$C_b$ = 100 pF, $R_b$ = 2.7 kΩ | 0 | 1420 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V,<br>1.6 V ≤ $V_b$ ≤ 2.0 V,<br>$C_b$ = 100 pF, $R_b$ = 5.5 kΩ | 0 | 1215 | ns |

**Notes 1.** The value must also be equal to or less than $f_{MCK}$/4.

**2.** Set the $f_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

**(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) = $AV_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V, Reference voltage (+) = $V_{BGR}$ Note 3, Reference voltage (–) = $AV_{REFM}$ Note 4 = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | 8 | | bit |
| Conversion time | $t_{CONV}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | 17 | | 39 | μs |
| Zero-scale error Notes 1, 2 | $E_{ZS}$ | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±0.60 | %FSR |
| Integral linearity error Note 1 | ILE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±2.0 | LSB |
| Differential linearity error Note 1 | DLE | 8-bit resolution | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | | | ±1.0 | LSB |
| Analog input voltage | $V_{AIN}$ | | | 0 | | $V_{BGR}$ Note 3 | V |

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

**4.** When reference voltage (–) = $V_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (–) = $AV_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (–) = $AV_{REFM}$.

### 3.6.2 Temperature sensor/internal reference voltage characteristics

**($T_A$ = –40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V, HS (high-speed main) mode)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Temperature sensor output voltage | $V_{TMPS25}$ | Setting ADS register = 80H, $T_A$ = +25°C | | 1.05 | | V |
| Internal reference voltage | $V_{BGR}$ | Setting ADS register = 81H | 1.38 | 1.45 | 1.5 | V |
| Temperature coefficient | $F_{VTMPS}$ | Temperature sensor that depends on the temperature | | –3.6 | | mV/°C |
| Operation stabilization wait time | $t_{AMP}$ | | 5 | | | μs |

### 3.6.4 LVD circuit characteristics

**LVD Detection Voltage of Reset Mode and Interrupt Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Detection voltage | Supply voltage level | $V_{LVD0}$ | Power supply rise time | 3.90 | 4.06 | 4.22 | V |
| | | | Power supply fall time | 3.83 | 3.98 | 4.13 | V |
| | | $V_{LVD1}$ | Power supply rise time | 3.60 | 3.75 | 3.90 | V |
| | | | Power supply fall time | 3.53 | 3.67 | 3.81 | V |
| | | $V_{LVD2}$ | Power supply rise time | 3.01 | 3.13 | 3.25 | V |
| | | | Power supply fall time | 2.94 | 3.06 | 3.18 | V |
| | | $V_{LVD3}$ | Power supply rise time | 2.90 | 3.02 | 3.14 | V |
| | | | Power supply fall time | 2.85 | 2.96 | 3.07 | V |
| | | $V_{LVD4}$ | Power supply rise time | 2.81 | 2.92 | 3.03 | V |
| | | | Power supply fall time | 2.75 | 2.86 | 2.97 | V |
| | | $V_{LVD5}$ | Power supply rise time | 2.70 | 2.81 | 2.92 | V |
| | | | Power supply fall time | 2.64 | 2.75 | 2.86 | V |
| | | $V_{LVD6}$ | Power supply rise time | 2.61 | 2.71 | 2.81 | V |
| | | | Power supply fall time | 2.55 | 2.65 | 2.75 | V |
| | | $V_{LVD7}$ | Power supply rise time | 2.51 | 2.61 | 2.71 | V |
| | | | Power supply fall time | 2.45 | 2.55 | 2.65 | V |
| Minimum pulse width | | $t_{LW}$ | | 300 | | | μs |
| Detection delay time | | | | | | 300 | μs |

**LVD Detection Voltage of Interrupt & Reset Mode**

**($T_A$ = –40 to +105°C, $V_{PDR} \le V_{DD} \le 5.5$ V, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Interrupt and reset mode | $V_{LVDD0}$ | $V_{POC2}$, $V_{POC1}$, $V_{POC0}$ = 0, 1, 1, falling reset voltage | | 2.64 | 2.75 | 2.86 | V |
| | $V_{LVDD1}$ | LVIS1, LVIS0 = 1, 0 | Rising release reset voltage | 2.81 | 2.92 | 3.03 | V |
| | | | Falling interrupt voltage | 2.75 | 2.86 | 2.97 | V |
| | $V_{LVDD2}$ | LVIS1, LVIS0 = 0, 1 | Rising release reset voltage | 2.90 | 3.02 | 3.14 | V |
| | | | Falling interrupt voltage | 2.85 | 2.96 | 3.07 | V |
| | $V_{LVDD3}$ | LVIS1, LVIS0 = 0, 0 | Rising release reset voltage | 3.90 | 4.06 | 4.22 | V |
| | | | Falling interrupt voltage | 3.83 | 3.98 | 4.13 | V |

### 3.6.5 Power supply voltage rising slope characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | $S_{VDD}$ | | | | 54 | V/ms |

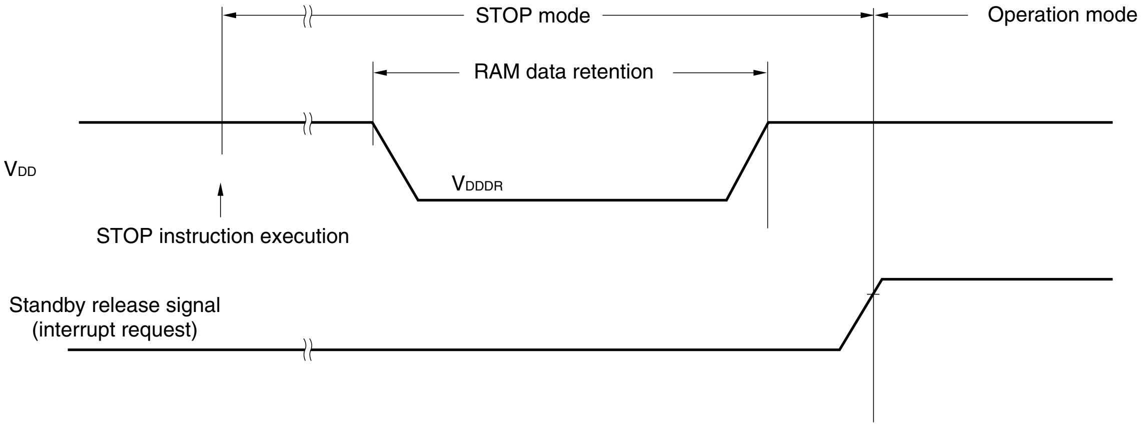
**Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until $V_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

## 3.7 RAM Data Retention Characteristics

**($T_A$ = –40 to +105°C, $V_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | $V_{DDDR}$ | | 1.44<sup>Note</sup> | | 5.5 | V |

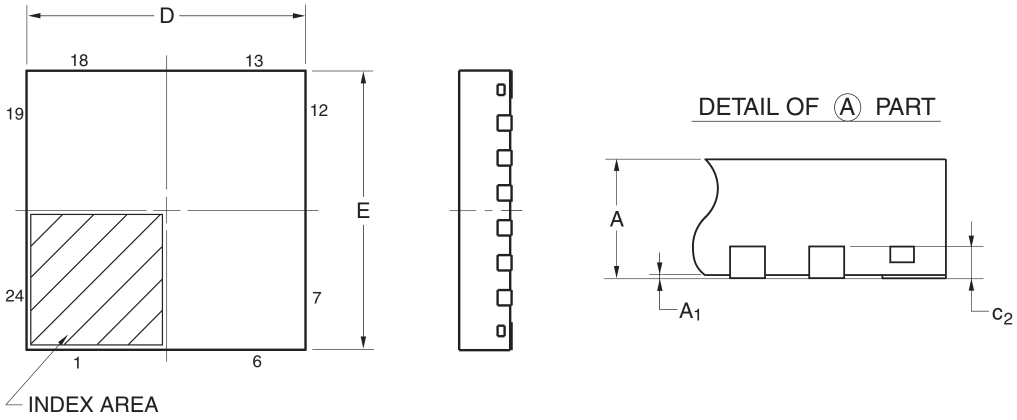
**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.

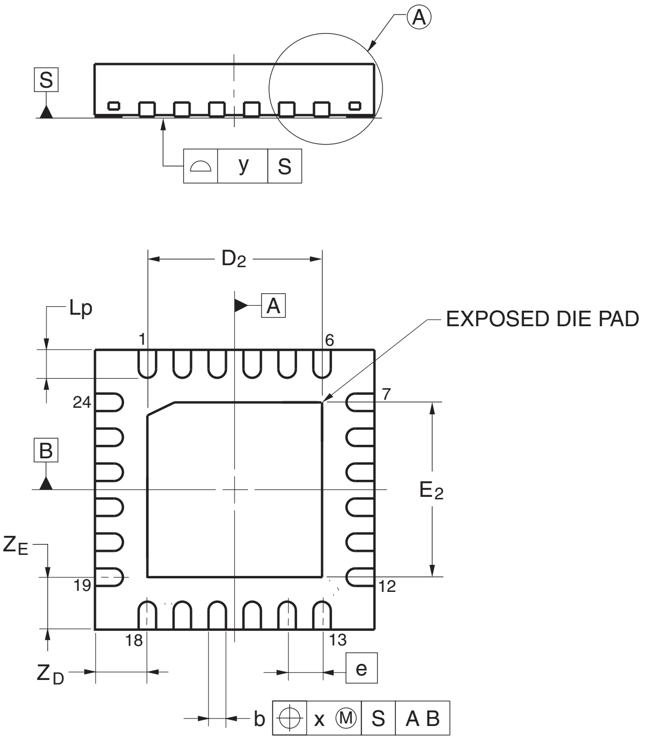


## 4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

| **JEITA Package code** | **RENESAS code** | **Previous code** | **MASS(TYP.)[g]** |
|---|---|---|---|
| P-HWQFN24-4x4-0.50 | PWQN0024KE-A | P24K8-50-CAB-3 | 0.04 |



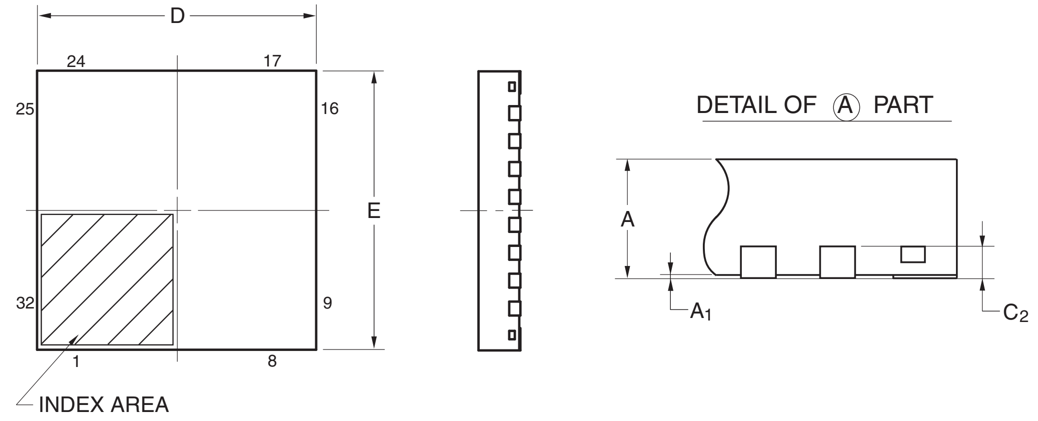


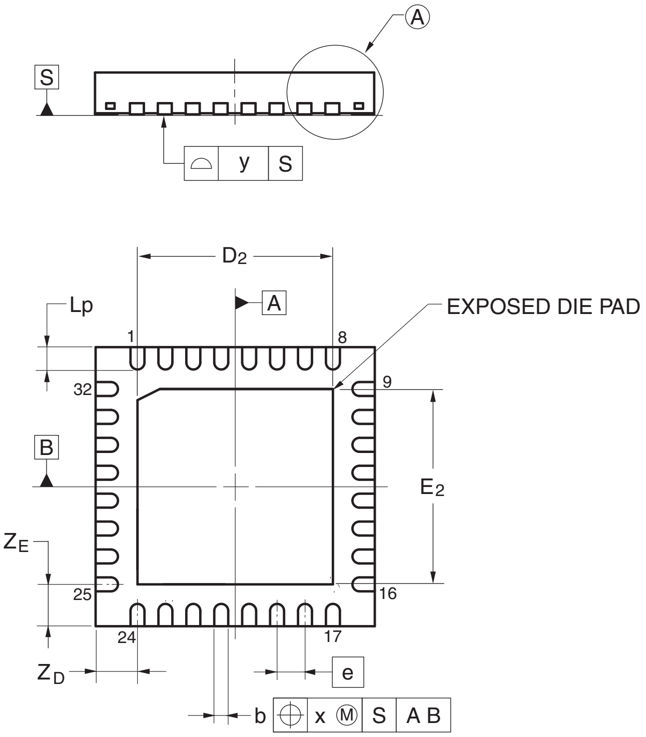
| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 3.95 | 4.00 | 4.05 |
| E | 3.95 | 4.00 | 4.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 2.50 | — |
| $E_2$ | — | 2.50 | — |

## 4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
R5F100BAGNA, R5F100BCGNA, R5F100BDGNA,R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.)[g] |
|---|---|---|---|
| P-HWQFN32-5x5-0.50 | PWQN0032KB-A | P32K8-50-3B4-5 | 0.06 |





| Referance Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | 4.95 | 5.00 | 5.05 |
| E | 4.95 | 5.00 | 5.05 |
| A | — | — | 0.80 |
| $A_1$ | 0.00 | — | — |
| b | 0.18 | 0.25 | 0.30 |
| e | — | 0.50 | — |
| Lp | 0.30 | 0.40 | 0.50 |
| x | — | — | 0.05 |
| y | — | — | 0.05 |
| $Z_D$ | — | 0.75 | — |
| $Z_E$ | — | 0.75 | — |
| $c_2$ | 0.15 | 0.20 | 0.25 |
| $D_2$ | — | 3.50 | — |
| $E_2$ | — | 3.50 | — |

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 3.00 | Aug 02, 2013 | 118 | Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics |
| | | 118 | Modification of table and note in 2.6.3 POR circuit characteristics |
| | | 119 | Modification of table in 2.6.4 LVD circuit characteristics |
| | | 120 | Modification of table of LVD Detection Voltage of Interrupt & Reset Mode |
| | | 120 | Renamed to 2.6.5 Power supply voltage rising slope characteristics |
| | | 122 | Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes |
| | | 123 | Modification of caution 1 and description |
| | | 124 | Modification of table and remark 3 in Absolute Maximum Ratings ($T_A$ = 25°C) |
| | | 126 | Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics |
| | | 126 | Modification of table in 3.2.2 On-chip oscillator characteristics |
| | | 127 | Modification of note 3 in 3.3.1 Pin characteristics (1/5) |
| | | 128 | Modification of note 3 in 3.3.1 Pin characteristics (2/5) |
| | | 133 | Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2) |
| | | 135 | Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2) |
| | | 137 | Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2) |
| | | 139 | Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2) |
| | | 140 | Modification of (3) Peripheral Functions (Common to all products) |
| | | 142 | Modification of table in 3.4 AC Characteristics |
| | | 143 | Addition of Minimum Instruction Execution Time during Main System Clock Operation |
| | | 143 | Modification of figure of AC Timing Test Points |
| | | 143 | Modification of figure of External System Clock Timing |
| | | 145 | Modification of figure of AC Timing Test Points |
| | | 145 | Modification of description, note 1, and caution in (1) During communication at same potential (UART mode) |
| | | 146 | Modification of description in (2) During communication at same potential (CSI mode) |
| | | 147 | Modification of description in (3) During communication at same potential (CSI mode) |
| | | 149 | Modification of table, note 1, and caution in (4) During communication at same potential (simplified $I^2C$ mode) |
| | | 151 | Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2) |
| | | 152 to 154 | Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2) |
| | | 155 | Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3) |
| | | 156 | Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3) |
| | | 157, 158 | Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3) |
| | | 160, 161 | Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) |