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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

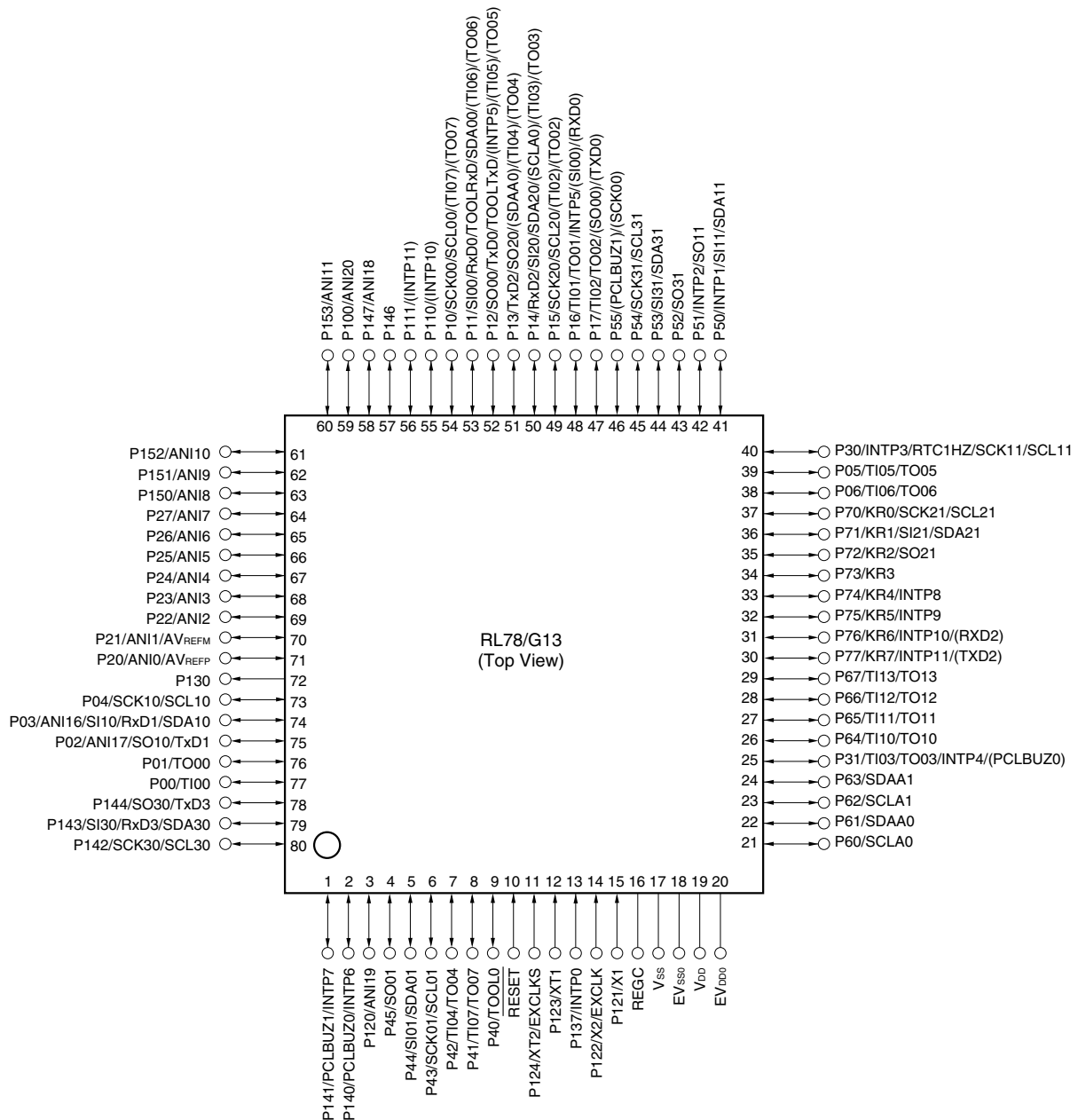
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	110
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 26x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	128-LQFP
Supplier Device Package	128-LFQFP (14x20)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100shdfb-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f100shdfb-v0</a>

## 1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)

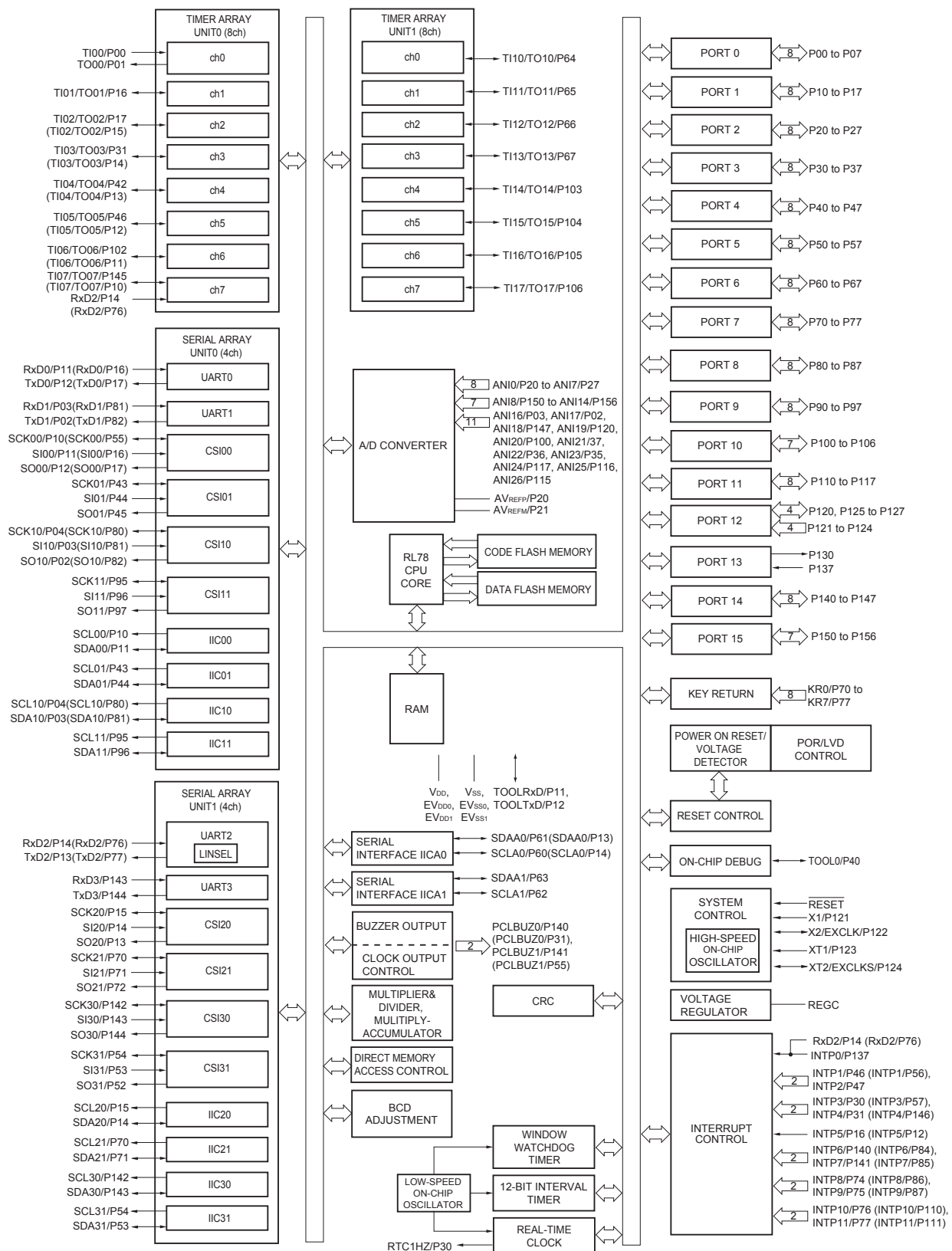


- Cautions**
1. Make EV<sub>SS0</sub> pin the same potential as V<sub>SS</sub> pin.
  2. Make V<sub>DD</sub> pin the potential that is higher than EV<sub>DD0</sub> pin.
  3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks** 1. For pin identification, see 1.4 Pin Identification.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub> and EV<sub>DD0</sub> pins and connect the V<sub>SS</sub> and EV<sub>SS0</sub> pins to separate ground lines.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.14 128-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4 <sup>Note1</sup>		2 to 4 <sup>Note1</sup>		2 to 4 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)											
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)											
Instruction set		<ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>											
I/O port	Total	16	20	21	26	28	32						
	CMOS I/O	13 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 5)	15 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 6)	15 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 6)	21 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 9)	22 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 9)	26 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)						
	CMOS input	3	3	3	3	3	3						
	CMOS output	–	–	1	–	–	–						
	N-ch O.D. I/O (withstand voltage: 6 V)	–	2	2	2	3	3						
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel <sup>Note 2</sup>											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2 <sup>Note 3</sup> )	4 channels (PWM outputs: 3 <sup>Note 3</sup> )				4 channels (PWM outputs: 3 <sup>Note 3</sup> ), 8 channels (PWM outputs: 7 <sup>Note 3</sup> ) <sup>Note 4</sup>						
	RTC output	–											

- Notes**
- The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.  
 R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H  
 R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H  
 For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.
  - Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f<sub>IL</sub>) is selected

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Ex	R5F101Ex	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—	4 to 8	—
RAM (KB)		2 to 16 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>		2 to 32 <sup>Note1</sup>	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)									
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)									
		30.5 μs (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)									
Instruction set		<ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)		31 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)		34 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 11)		38 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 13)		48 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	—		—		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3 <sup>Note2</sup> ), 8 channels (PWM outputs: 7 <sup>Note2, Note3</sup> )		5 channels (PWM outputs: 4 <sup>Note2</sup> ), 8 channels (PWM outputs: 7 <sup>Note2</sup> ) <sup>Note3</sup>						8 channels (PWM outputs: 7 <sup>Note2</sup> )	
	RTC output	1 channel • 1 Hz (subsystem clock: f <sub>SUB</sub> = 32.768 kHz)									

**Notes** 1. The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H

R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

(2/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		<ul style="list-style-type: none"><li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: <math>f_{\text{MAIN}} = 20 \text{ MHz}</math> operation)</li><li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: <math>f_{\text{SUB}} = 32.768 \text{ kHz}</math> operation)</li></ul>					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products]					
		<ul style="list-style-type: none"><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li></ul>					
	I <sup>2</sup> C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		<ul style="list-style-type: none"><li>16 bits <math>\times</math> 16 bits = 32 bits (Unsigned or signed)</li><li>32 bits <math>\div</math> 32 bits = 32 bits (Unsigned)</li><li>16 bits <math>\times</math> 16 bits + 32 bits = 32 bits (Unsigned or signed)</li></ul>					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		<ul style="list-style-type: none"><li>Reset by <math>\overline{\text{RESET}}</math> pin</li><li>Internal reset by watchdog timer</li><li>Internal reset by power-on-reset</li><li>Internal reset by voltage detector</li><li>Internal reset by illegal instruction execution <sup>Note</sup></li><li>Internal reset by RAM parity error</li><li>Internal reset by illegal-memory access</li></ul>					
Power-on-reset circuit		<ul style="list-style-type: none"><li>Power-on-reset: 1.51 V (TYP.)</li><li>Power-down-reset: 1.50 V (TYP.)</li></ul>					
Voltage detector		<ul style="list-style-type: none"><li>Rising edge : 1.67 V to 4.06 V (14 stages)</li><li>Falling edge : 1.63 V to 3.98 V (14 stages)</li></ul>					
On-chip debug function		Provided					
Power supply voltage		$V_{\text{DD}} = 1.6 \text{ to } 5.5 \text{ V}$ ( $T_{\text{A}} = -40 \text{ to } +85^{\circ}\text{C}$ ) $V_{\text{DD}} = 2.4 \text{ to } 5.5 \text{ V}$ ( $T_{\text{A}} = -40 \text{ to } +105^{\circ}\text{C}$ )					
Operating ambient temperature		$T_{\text{A}} = 40 \text{ to } +85^{\circ}\text{C}$ (A: Consumer applications, D: Industrial applications ) $T_{\text{A}} = 40 \text{ to } +105^{\circ}\text{C}$ (G: Industrial applications)					

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

&lt;R&gt;

## 2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +6.5	V
	EV <sub>DD0</sub> , EV <sub>DD1</sub>	EV <sub>DD0</sub> = EV <sub>DD1</sub>	-0.5 to +6.5	V
	EV <sub>SS0</sub> , EV <sub>SS1</sub>	EV <sub>SS0</sub> = EV <sub>SS1</sub>	-0.5 to +0.3	V
REGC pin input voltage	V <sub>IREGC</sub>	REGC	-0.3 to +2.8 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 1</sup>	V
Input voltage	V <sub>I1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>I2</sub>	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V <sub>I3</sub>	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Output voltage	V <sub>O1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
	V <sub>O2</sub>	P20 to P27, P150 to P156	-0.3 to V <sub>DD</sub> + 0.3 <sup>Note 2</sup>	V
Analog input voltage	V <sub>AI1</sub>	ANI16 to ANI26	-0.3 to EV <sub>DD0</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V
	V <sub>AI2</sub>	ANI0 to ANI14	-0.3 to V <sub>DD</sub> + 0.3 and -0.3 to AV <sub>REF</sub> (+) + 0.3 <sup>Notes 2, 3</sup>	V

**Notes 1.** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

**2.** Must be 6.5 V or lower.

**3.** Do not exceed AV<sub>REF</sub>(+) + 0.3 V in case of A/D conversion target pin.

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remarks 1.** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**2.** AV<sub>REF</sub>(+) : + side reference voltage of the A/D converter.

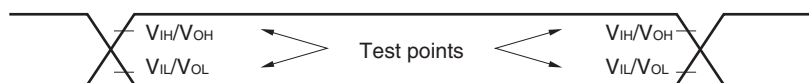
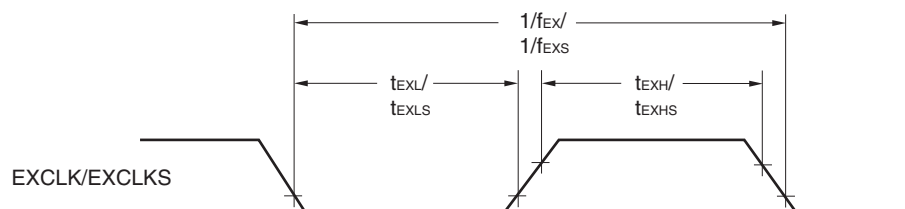
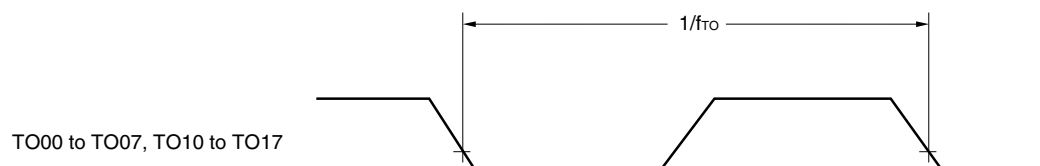
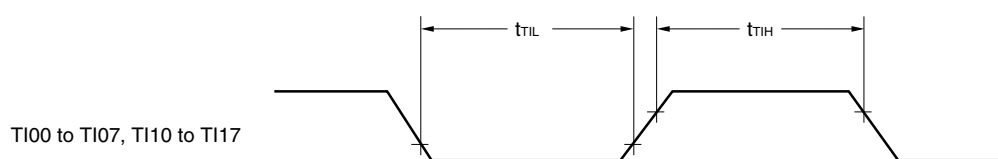
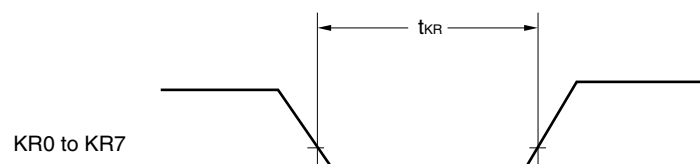
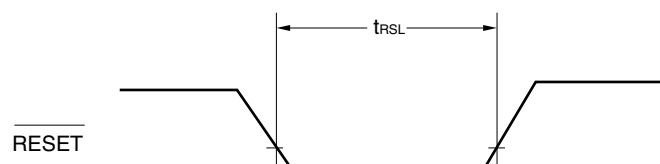
**3.** V<sub>SS</sub> : Reference voltage

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V <sub>OH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -10.0 mA	E <sub>VDD0</sub> - 1.5		V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -3.0 mA	E <sub>VDD0</sub> - 0.7		V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -2.0 mA	E <sub>VDD0</sub> - 0.6		V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OH1</sub> = -1.5 mA	E <sub>VDD0</sub> - 0.5		V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OH1</sub> = -1.0 mA	E <sub>VDD0</sub> - 0.5		V
	V <sub>OH2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OH2</sub> = -100 μA	V <sub>DD</sub> - 0.5		V
Output voltage, low	V <sub>OL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 20 mA		1.3	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 8.5 mA		0.7	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 3.0 mA		0.6	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 1.5 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL1</sub> = 0.6 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL1</sub> = 0.3 mA		0.4	V
	V <sub>OL2</sub>	P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V, I <sub>OL2</sub> = 400 μA		0.4	V
	V <sub>OL3</sub>	P60 to P63	4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 15.0 mA		2.0	V
			4.0 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 5.0 mA		0.4	V
			2.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 3.0 mA		0.4	V
			1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V, I <sub>OL3</sub> = 2.0 mA		0.4	V
			1.6 V ≤ E <sub>VDD0</sub> < 5.5 V, I <sub>OL3</sub> = 1.0 mA		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**AC Timing Test Points****External System Clock Timing****TI/TO Timing****Interrupt Request Input Timing****Key Interrupt Input Timing****RESET Input Timing**

## (4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) <sup>Note 1</sup>	t <sub>SIK2</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +20		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		1/f <sub>MCK</sub> +30		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +40		1/f <sub>MCK</sub> +40		ns
Slp hold time (from SCKp↑) <sup>Note 2</sup>	t <sub>KSI2</sub>	1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		1/f <sub>MCK</sub> +31		ns
		1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		ns
		1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		1/f <sub>MCK</sub> +250		1/f <sub>MCK</sub> +250		ns
Delay time from SCKp↓ to SOp output <sup>Note 3</sup>	t <sub>KSO2</sub>	C = 30 pF <sup>Note 4</sup>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +44		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			2.4 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +75		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110		2/f <sub>MCK</sub> +110	ns
			1.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220	ns
			1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		—		2/f <sub>MCK</sub> +220		2/f <sub>MCK</sub> +220	ns

- Notes**
1. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp setup time becomes “to SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  2. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The Slp hold time becomes “from SCKp↓” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  3. When DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 0, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 1. The delay time to SOp output becomes “from SCKp↑” when DAP<sub>mn</sub> = 0 and CKP<sub>mn</sub> = 1, or DAP<sub>mn</sub> = 1 and CKP<sub>mn</sub> = 0.
  4. C is the load capacitance of the SOp output lines.
  5. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),  
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)
  2. f<sub>MCK</sub>: Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>). m: Unit number,  
n: Channel number (mn = 00 to 03, 10 to 13))

3. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV<sub>DD0</sub> < 4.0 V and 2.3 V ≤ V<sub>b</sub> ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
5. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.
6. The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV<sub>DD0</sub> < 3.3 V and 1.6 V ≤ V<sub>b</sub> ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

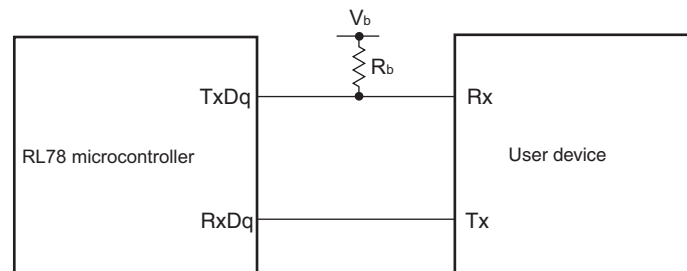
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the Rx<sub>Dq</sub> pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the Tx<sub>Dq</sub> pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



**(2) I<sup>2</sup>C fast mode****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode: f <sub>CLK</sub> ≥ 3.5 MHz	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	t <sub>SU:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t <sub>LOW</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t <sub>HIGH</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	t <sub>SU:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		100		100		100		μs
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	t <sub>SU:STO</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t <sub>BUF</sub>	2.7 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		1.3		1.3		1.3		μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.Fast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

&lt;R&gt;

- Notes**
1. Excludes quantization error ( $\pm 1/2$  LSB).
  2. This value is indicated as a ratio (%FSR) to the full-scale value.
  3. When  $AV_{REFP} < V_{DD}$ , the MAX. values are as follows.  
Overall error: Add  $\pm 1.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
Zero-scale error/Full-scale error: Add  $\pm 0.05\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .  
Integral linearity error/ Differential linearity error: Add  $\pm 0.5$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .
  4. Values when the conversion time is set to  $57\ \mu\text{s}$  (min.) and  $95\ \mu\text{s}$  (max.).
  5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

**( $T_A = -40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (5/5)**

Items	Symbol	Conditions	MIN.		TYP.	MAX.	Unit	
Input leakage current, high	I <sub>LH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>DD0</sub>			1	μA	
	I <sub>LH2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>DD</sub>			1	μA	
	I <sub>LH3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>DD</sub>	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	I <sub>LIL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub>			−1	μA	
	I <sub>LIL2</sub>	P20 to P27, P137, P150 to P156, RESET	V <sub>I</sub> = V <sub>SS</sub>			−1	μA	
	I <sub>LIL3</sub>	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V <sub>I</sub> = V <sub>SS</sub>	In input port or external clock input		−1	μA	
				In resonator connection		−10	μA	
On-chip pll-up resistance	R <sub>U</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V <sub>I</sub> = EV <sub>SS0</sub> , In input port		10	20	100	kΩ

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$  or  $I_{DD2}$  and  $I_{ADC}$  when the A/D converter is in operation.
7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of  $I_{DD1}$ ,  $I_{DD2}$  or  $I_{DD3}$  and  $I_{LVD}$  when the LVD circuit is in operation.
8. Current flowing only during data flash rewrite.
9. Current flowing only during self programming.
10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

- Remarks**
1.  $f_{IL}$ : Low-speed on-chip oscillator clock frequency
  2.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  3.  $f_{CLK}$ : CPU/peripheral hardware clock frequency
  4. Temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

## (2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V})$ 

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time	$t_{KCY1}$	$t_{KCY1} \geq 4/f_{CLK}$			
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	250		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	500		ns
SCKp high-/low-level width	$t_{KH1}$ , $t_{KL1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 24$		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 36$		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 76$		ns
Slp setup time (to SCKp $\uparrow$ ) <sup>Note 1</sup>	$t_{SIK1}$	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	66		ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	66		ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	113		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note 2</sup>	$t_{KSI1}$		38		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note 3</sup>	$t_{KSO1}$	$C = 30\text{ pF}$ <sup>Note 4</sup>		50	ns

- Notes**
1. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp setup time becomes “to SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  2. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The Slp hold time becomes “from SCKp $\downarrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  3. When  $DAPmn = 0$  and  $CKPmn = 0$ , or  $DAPmn = 1$  and  $CKPmn = 1$ . The delay time to SOp output becomes “from SCKp $\uparrow$ ” when  $DAPmn = 0$  and  $CKPmn = 1$ , or  $DAPmn = 1$  and  $CKPmn = 0$ .
  4. C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),  
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
  2.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**Notes** 1. Excludes quantization error ( $\pm 1/2$  LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When  $AV_{REFP} < V_{DD}$ , the MAX. values are as follows.

Overall error: Add  $\pm 1.0$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Zero-scale error/Full-scale error: Add  $\pm 0.05\%$ FSR to the MAX. value when  $AV_{REFP} = V_{DD}$ .

Integral linearity error/ Differential linearity error: Add  $\pm 0.5$  LSB to the MAX. value when  $AV_{REFP} = V_{DD}$ .

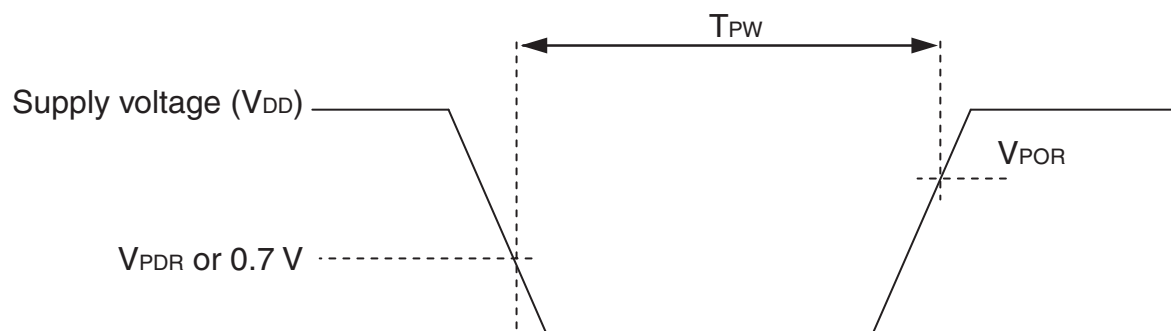
4. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

## 3.6.3 POR circuit characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	$V_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	$V_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	$T_{PW}$		300			$\mu\text{s}$

**Note** Minimum time required for a POR reset when  $V_{DD}$  exceeds below  $V_{PDR}$ . This is also the minimum time required for a POR reset from when  $V_{DD}$  exceeds below 0.7 V to when  $V_{DD}$  exceeds  $V_{POR}$  while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 3.6.5 Power supply voltage rising slope characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	$S_{VDD}$				54	V/ms

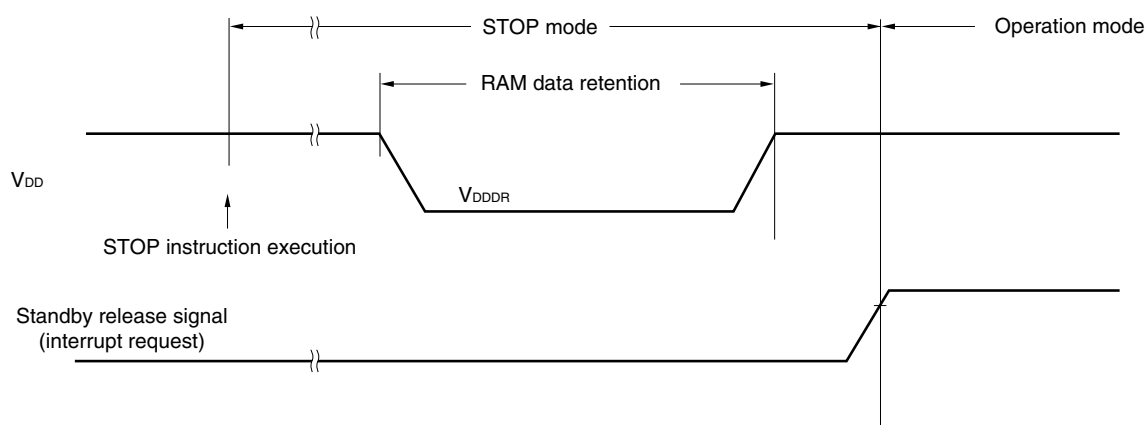
**Caution** Make sure to keep the internal reset state by the LVD circuit or an external reset until  $V_{DD}$  reaches the operating voltage range shown in 3.4 AC Characteristics.

## 3.7 RAM Data Retention Characteristics

 $(T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0$  V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	$V_{DDDR}$		1.44 <sup>Note</sup>		5.5	V

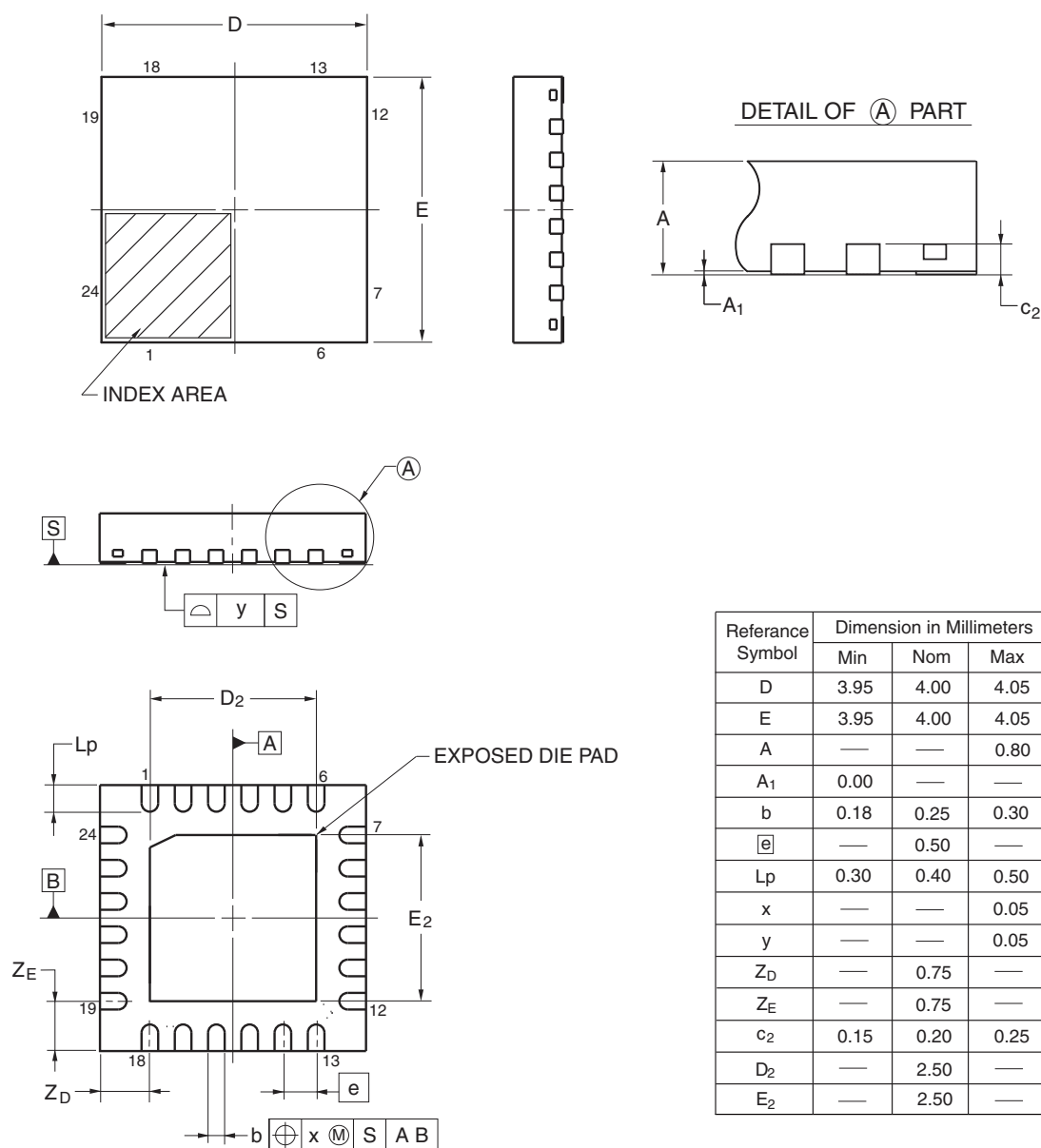
**Note** This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



## 4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA  
 R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA  
 R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA  
 R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA  
 R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

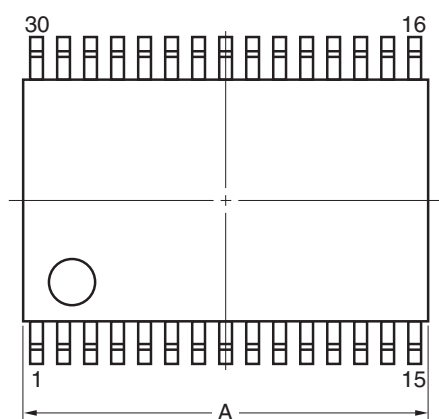
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04



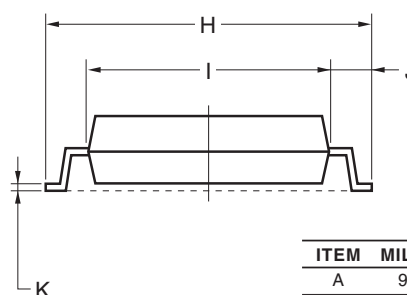
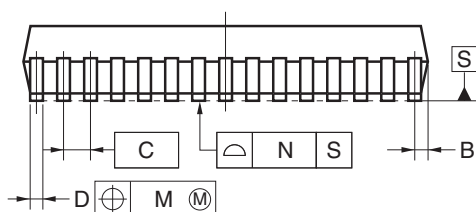
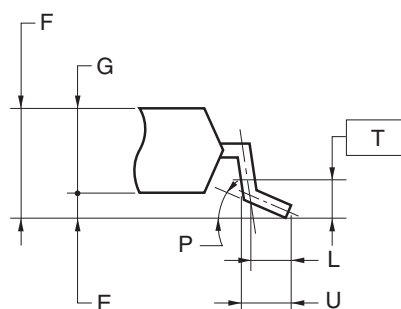
## 4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP  
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP  
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP  
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP  
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end

**NOTE**

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 <sup>+0.08</sup> <sub>-0.07</sub>
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° <sup>+5°</sup> <sub>-3°</sub>
T	0.25
U	0.6±0.15