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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

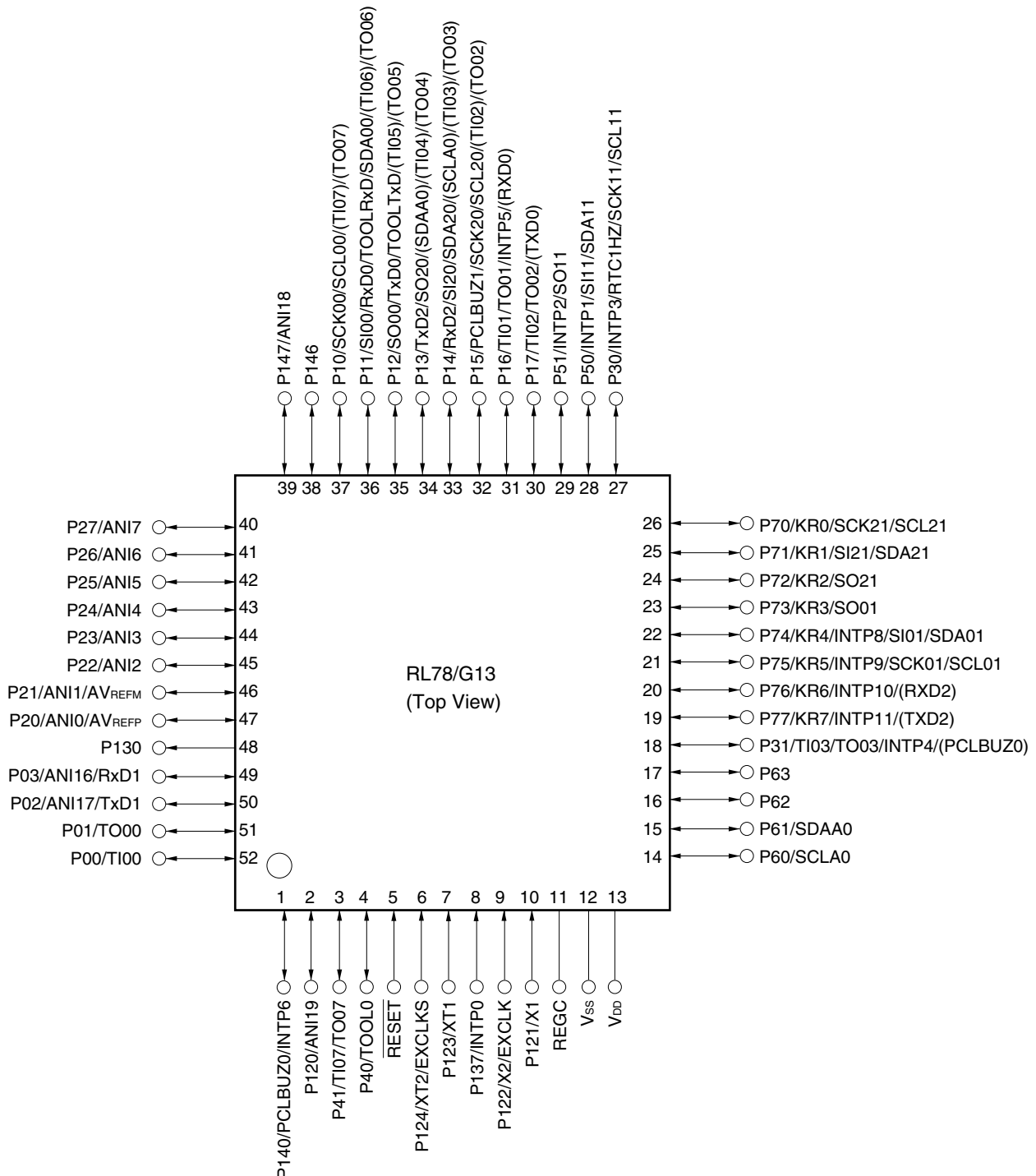
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1016dasp-v0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1016dasp-v0</a>

## 1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



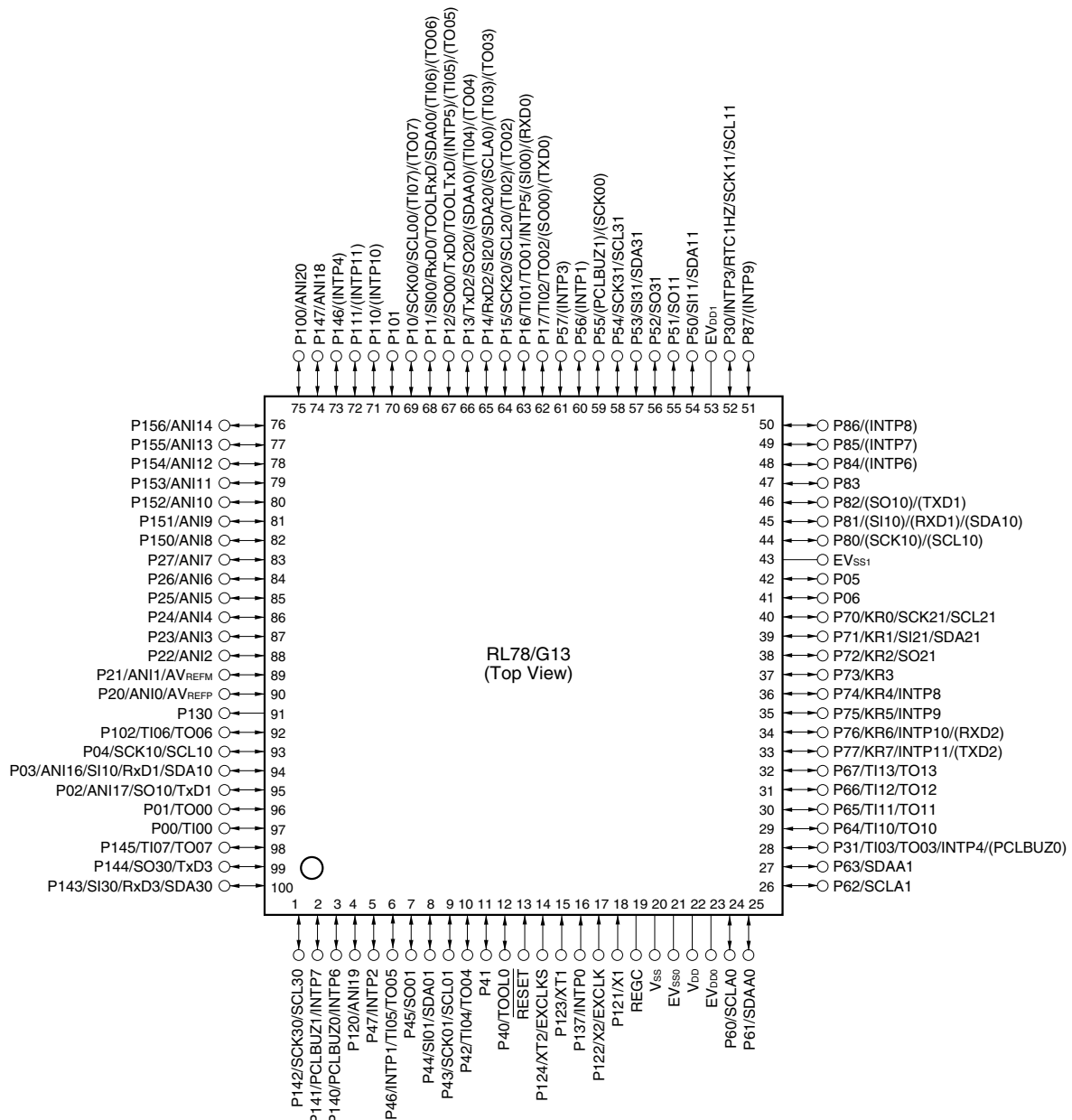
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.3.13 100-pin products

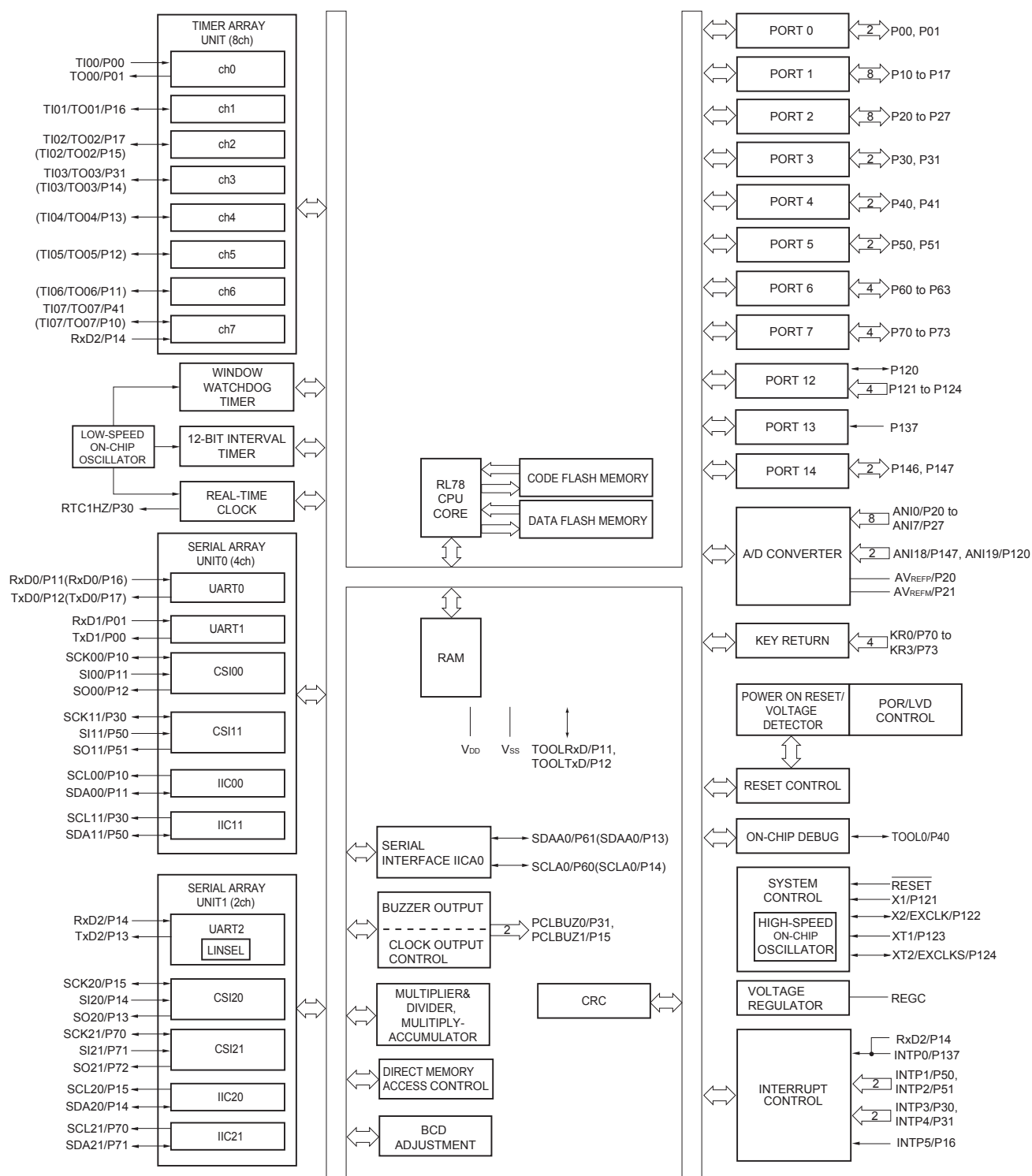
- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)



- Cautions**
1. Make EV<sub>SS0</sub>, EV<sub>SS1</sub> pins the same potential as V<sub>SS</sub> pin.
  2. Make V<sub>DD</sub> pin the potential that is higher than EV<sub>DD0</sub>, EV<sub>DD1</sub> pins (EV<sub>DD0</sub> = EV<sub>DD1</sub>).
  3. Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
  2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V<sub>DD</sub>, EV<sub>DD0</sub> and EV<sub>DD1</sub> pins and connect the V<sub>SS</sub>, EV<sub>SS0</sub> and EV<sub>SS1</sub> pins to separate ground lines.
  3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.8 44-pin products



**Remark** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[80-pin, 100-pin, 128-pin products]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Code flash memory (KB)		96 to 512		96 to 512		192 to 512	
Data flash memory (KB)		8	—	8	—	8	—
RAM (KB)		8 to 32 <sup>Note 1</sup>		8 to 32 <sup>Note 1</sup>		16 to 32 <sup>Note 1</sup>	
Address space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)					
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)					
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz					
Low-speed on-chip oscillator		15 kHz (TYP.)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)					
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)					
		30.5 μs (Subsystem clock: f <sub>SUB</sub> = 32.768 kHz operation)					
Instruction set		<ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>					
I/O port	Total	74		92		120	
	CMOS I/O	64 (N-ch O.D. I/O [EVD <sub>D</sub> withstand voltage]: 21)		82 (N-ch O.D. I/O [EVD <sub>D</sub> withstand voltage]: 24)		110 (N-ch O.D. I/O [EVD <sub>D</sub> withstand voltage]: 25)	
	CMOS input	5		5		5	
	CMOS output	1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	4		4		4	
Timer	16-bit timer	12 channels		12 channels		16 channels	
	Watchdog timer	1 channel		1 channel		1 channel	
	Real-time clock (RTC)	1 channel		1 channel		1 channel	
	12-bit interval timer (IT)	1 channel		1 channel		1 channel	
	Timer output	12 channels (PWM outputs: 10 <sup>Note 2</sup> )		12 channels (PWM outputs: 10 <sup>Note 2</sup> )		16 channels (PWM outputs: 14 <sup>Note 2</sup> )	
	RTC output	1 channel • 1 Hz (subsystem clock: f <sub>SUB</sub> = 32.768 kHz)					

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H

R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C) (2/2)**

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I <sub>OH1</sub>	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I <sub>OH2</sub>	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
	Output current, low	I <sub>OL1</sub>	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
I <sub>OL2</sub>		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T <sub>A</sub>	In normal operation mode		−40 to +85
	In flash memory programming mode				
Storage temperature	T <sub>stg</sub>			−65 to +150	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V <sub>IH1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV <sub>DD0</sub>	EV <sub>DD0</sub>	V
	V <sub>IH2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	2.2	EV <sub>DD0</sub>	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	2.0	EV <sub>DD0</sub>	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	1.5	EV <sub>DD0</sub>	V
	V <sub>IH3</sub>	P20 to P27, P150 to P156	0.7V <sub>DD</sub>		V <sub>DD</sub>	V
	V <sub>IH4</sub>	P60 to P63	0.7EV <sub>DD0</sub>		6.0	V
	V <sub>IH5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0.8V <sub>DD</sub>		V <sub>DD</sub>	V
Input voltage, low	V <sub>IL1</sub>	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	0.2EV <sub>DD0</sub>	V
	V <sub>IL2</sub>	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V	0	0.8	V
			TTL input buffer 3.3 V ≤ EV <sub>DD0</sub> < 4.0 V	0	0.5	V
			TTL input buffer 1.6 V ≤ EV <sub>DD0</sub> < 3.3 V	0	0.32	V
	V <sub>IL3</sub>	P20 to P27, P150 to P156	0		0.3V <sub>DD</sub>	V
	V <sub>IL4</sub>	P60 to P63	0		0.3EV <sub>DD0</sub>	V
	V <sub>IL5</sub>	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		0.2V <sub>DD</sub>	V

**Caution** The maximum value of V<sub>IH</sub> of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV<sub>DD0</sub>, even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz
    - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C



**(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products****( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (1/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current <sup>Note 1</sup>	$\text{I}_{\text{DD1}}$	Operating mode	HS (high-speed main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 32\text{ MHz}$ <sup>Note 3</sup>	Basic operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$	2.6		mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$	2.6		mA
					Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$	6.1	9.5	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$	6.1	9.5	mA
				$f_{\text{IH}} = 24\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$	4.8	7.4	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$	4.8	7.4	mA
				$f_{\text{IH}} = 16\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$	3.5	5.3	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$	3.5	5.3	mA
			LS (low-speed main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 8\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$	1.5	2.3	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$	1.5	2.3	mA
			LV (low-voltage main) mode <sup>Note 5</sup>	$f_{\text{IH}} = 4\text{ MHz}$ <sup>Note 3</sup>	Normal operation	$\text{V}_{\text{DD}} = 3.0\text{ V}$	1.5	2.0	mA
						$\text{V}_{\text{DD}} = 2.0\text{ V}$	1.5	2.0	mA
			HS (high-speed main) mode <sup>Note 5</sup>	$f_{\text{MX}} = 20\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input	3.9	6.1	mA
						Resonator connection	4.1	6.3	mA
				$f_{\text{MX}} = 20\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input	3.9	6.1	mA
						Resonator connection	4.1	6.3	mA
				$f_{\text{MX}} = 10\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input	2.5	3.7	mA
						Resonator connection	2.5	3.7	mA
				$f_{\text{MX}} = 10\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input	2.5	3.7	mA
						Resonator connection	2.5	3.7	mA
			LS (low-speed main) mode <sup>Note 5</sup>	$f_{\text{MX}} = 8\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input	1.4	2.2	mA
						Resonator connection	1.4	2.2	mA
				$f_{\text{MX}} = 8\text{ MHz}$ <sup>Note 2</sup> , $\text{V}_{\text{DD}} = 2.0\text{ V}$	Normal operation	Square wave input	1.4	2.2	mA
						Resonator connection	1.4	2.2	mA
			Subsystem clock operation	$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = -40^\circ\text{C}$	Normal operation	Square wave input	5.4	6.5	$\mu\text{A}$
						Resonator connection	5.5	6.6	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +25^\circ\text{C}$	Normal operation	Square wave input	5.5	6.5	$\mu\text{A}$
						Resonator connection	5.6	6.6	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +50^\circ\text{C}$	Normal operation	Square wave input	5.6	9.4	$\mu\text{A}$
						Resonator connection	5.7	9.5	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +70^\circ\text{C}$	Normal operation	Square wave input	5.9	12.0	$\mu\text{A}$
						Resonator connection	6.0	12.1	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ <sup>Note 4</sup> $T_A = +85^\circ\text{C}$	Normal operation	Square wave input	6.6	16.3	$\mu\text{A}$
						Resonator connection	6.7	16.4	$\mu\text{A}$

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
    - HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 32 MHz  
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 16 MHz
    - LS (low-speed main) mode:  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 8 MHz
    - LV (low-voltage main) mode:  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$  @ 1 MHz to 4 MHz
  8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks 1.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f<sub>IH</sub>: High-speed on-chip oscillator clock frequency
3. f<sub>SUB</sub>: Subsystem clock frequency (XT1 clock oscillation frequency)
4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T<sub>A</sub> = 25°C

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit	
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		Reception	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V			f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1	bps
						5.3		1.3		0.6	Mbps
			Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 4</sup>								
						5.3		1.3		0.6	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V			f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1		f <sub>MCK</sub> /6 Note 1	bps
						5.3		1.3		0.6	Mbps
1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V			f <sub>MCK</sub> /6 Notes 1 to 3		f <sub>MCK</sub> /6 Notes 1, 2		f <sub>MCK</sub> /6 Notes 1, 2	bps			
			5.3		1.3		0.6	Mbps			
Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 4</sup>											

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.**2.** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.**3.** The following conditions are required for low voltage interface when EV<sub>DD0</sub> < V<sub>DD</sub>.2.4 V ≤ EV<sub>DD0</sub> < 2.7 V : MAX. 2.6 Mbps1.8 V ≤ EV<sub>DD0</sub> < 2.4 V : MAX. 1.3 Mbps**4.** The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:HS (high-speed main) mode: 32 MHz (2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V)16 MHz (2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V)LS (low-speed main) mode: 8 MHz (1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V)LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

**Remarks 1.** V<sub>b</sub>[V]: Communication line voltage**2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)**3.** f<sub>MCK</sub>: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V		<b>Note 1</b>		<b>Note 1</b>		<b>Note 1</b>	bps
					2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V		<b>Note 3</b>		<b>Note 3</b>		<b>Note 3</b>	bps
					1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V		<b>Notes 5, 6</b>		<b>Notes 5, 6</b>		<b>Notes 5, 6</b>	bps
					0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

**Notes 1.** The smaller maximum transfer rate derived by using f<sub>MCK</sub>/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV<sub>DD0</sub> ≤ 5.5 V and 2.7 V ≤ V<sub>b</sub> ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

\* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)  
(1/3)(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t <sub>KCY1</sub>	t <sub>KCY1</sub> ≥ 4/f <sub>CLK</sub> 4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	300		1150		1150		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	500		1150		1150		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t <sub>KH1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 75		t <sub>KCY1</sub> /2 – 75		t <sub>KCY1</sub> /2 – 75		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 170		t <sub>KCY1</sub> /2 – 170		t <sub>KCY1</sub> /2 – 170		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 – 458		t <sub>KCY1</sub> /2 – 458		t <sub>KCY1</sub> /2 – 458		ns
SCKp low-level width	t <sub>KL1</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 1.4 kΩ	t <sub>KCY1</sub> /2 – 12		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 30 pF, R <sub>b</sub> = 2.7 kΩ	t <sub>KCY1</sub> /2 – 18		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note</sup> , C <sub>b</sub> = 30 pF, R <sub>b</sub> = 5.5 kΩ	t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		t <sub>KCY1</sub> /2 – 50		ns

**Note** Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output (V<sub>DD</sub> tolerance (When 20- to 52-pin products)/EV<sub>DD</sub> tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (3/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	$\text{V}_{\text{IH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	$0.8\text{EV}_{\text{DD0}}$	$\text{EV}_{\text{DD0}}$	V
	$\text{V}_{\text{IH2}}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	2.2	$\text{EV}_{\text{DD0}}$	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	2.0	$\text{EV}_{\text{DD0}}$	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	1.5	$\text{EV}_{\text{DD0}}$	V
	$\text{V}_{\text{IH3}}$	P20 to P27, P150 to P156	$0.7\text{V}_{\text{DD}}$		$\text{V}_{\text{DD}}$	V
	$\text{V}_{\text{IH4}}$	P60 to P63	$0.7\text{EV}_{\text{DD0}}$		6.0	V
	$\text{V}_{\text{IH5}}$	P121 to P124, P137, EXCLK, EXCLKS, RESET	$0.8\text{V}_{\text{DD}}$		$\text{V}_{\text{DD}}$	V
Input voltage, low	$\text{V}_{\text{IL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0	$0.2\text{EV}_{\text{DD0}}$	V
	$\text{V}_{\text{IL2}}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer $4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	0	0.8	V
			TTL input buffer $3.3\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	0	0.5	V
			TTL input buffer $2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$	0	0.32	V
	$\text{V}_{\text{IL3}}$	P20 to P27, P150 to P156	0		$0.3\text{V}_{\text{DD}}$	V
	$\text{V}_{\text{IL4}}$	P60 to P63	0		$0.3\text{EV}_{\text{DD0}}$	V
	$\text{V}_{\text{IL5}}$	P121 to P124, P137, EXCLK, EXCLKS, RESET	0		$0.2\text{V}_{\text{DD}}$	V

**Caution** The maximum value of  $\text{V}_{\text{IH}}$  of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is  $\text{EV}_{\text{DD0}}$ , even in the N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$

- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. During HALT instruction execution by flash memory.
  3. When high-speed on-chip oscillator and subsystem clock are stopped.
  4. When high-speed system clock and subsystem clock are stopped.
  5. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $RTCLPC = 1$  and setting ultra-low current consumption ( $AMPHS1 = 1$ ). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
  7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$   
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)****( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp $\uparrow$ ) <sup>Note</sup>	$t_{\text{SIK1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	162		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	354		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 5.5\text{ k}\Omega$	958		ns
Slp hold time (from SCKp $\uparrow$ ) <sup>Note</sup>	$t_{\text{KSI1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$	38		ns
Delay time from SCKp $\downarrow$ to SOp output <sup>Note</sup>	$t_{\text{KSO1}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 1.4\text{ k}\Omega$		200	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 2.7\text{ k}\Omega$		390	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $\text{C}_b = 30\text{ pF}$ , $\text{R}_b = 5.5\text{ k}\Omega$		966	ns

**Note** When  $\text{DAPmn} = 0$  and  $\text{CKPmn} = 0$ , or  $\text{DAPmn} = 1$  and  $\text{CKPmn} = 1$ .

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output ( $\text{V}_{\text{DD}}$  tolerance (for the 20- to 52-pin products)/ $\text{EV}_{\text{DD}}$  tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $\text{V}_{\text{IH}}$  and  $\text{V}_{\text{IL}}$ , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

## (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

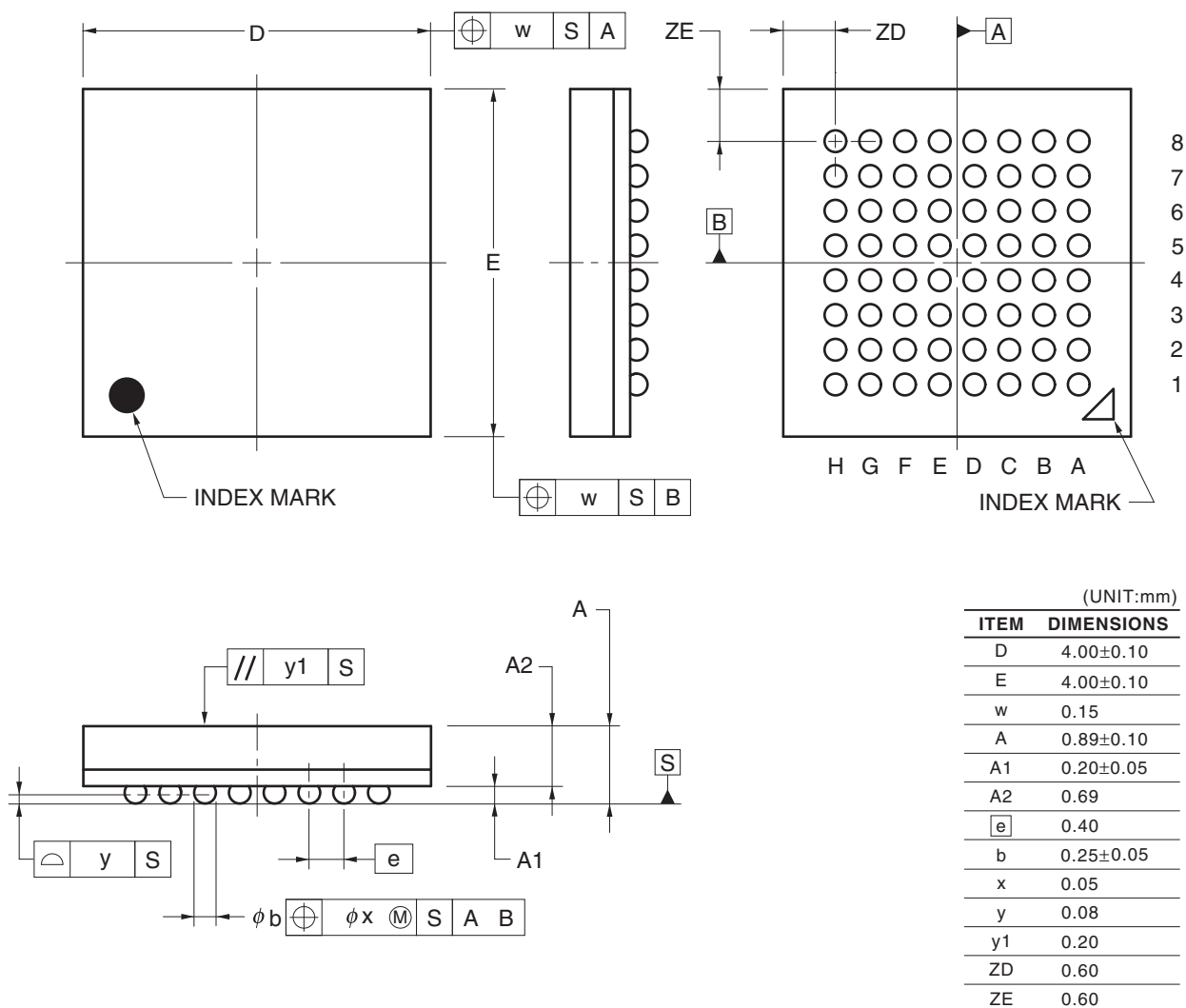
(T<sub>A</sub> =  $-40$  to  $+105^{\circ}\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ )

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time <sup>Note 1</sup>	t <sub>KCY2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$28/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$20/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$40/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$28/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$24/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$16/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$12/f_{\text{MCK}}$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$	$24\text{ MHz} < f_{\text{MCK}}$	$96/f_{\text{MCK}}$		ns
			$20\text{ MHz} < f_{\text{MCK}} \leq 24\text{ MHz}$	$72/f_{\text{MCK}}$		ns
			$16\text{ MHz} < f_{\text{MCK}} \leq 20\text{ MHz}$	$64/f_{\text{MCK}}$		ns
			$8\text{ MHz} < f_{\text{MCK}} \leq 16\text{ MHz}$	$52/f_{\text{MCK}}$		ns
			$4\text{ MHz} < f_{\text{MCK}} \leq 8\text{ MHz}$	$32/f_{\text{MCK}}$		ns
			$f_{\text{MCK}} \leq 4\text{ MHz}$	$20/f_{\text{MCK}}$		ns
SCKp high-/low-level width	t <sub>KH2</sub> , t <sub>KL2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		t <sub>KCY2</sub> /2 – 24		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		t <sub>KCY2</sub> /2 – 36		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ <sup>Note 2</sup>		t <sub>KCY2</sub> /2 – 100		ns
Slp setup time (to SCKp↑) <sup>Note 2</sup>	t <sub>SIK2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$1/f_{\text{MCK}} + 40$		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$1/f_{\text{MCK}} + 60$		ns
Slp hold time (from SCKp↑) <sup>Note 3</sup>	t <sub>KSI2</sub>			$1/f_{\text{MCK}} + 62$		ns
Delay time from SCKp↓ to SOp output <sup>Note 4</sup>	t <sub>KSO2</sub>	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 1.4\text{ k}\Omega$			$2/f_{\text{MCK}} + 240$	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$ , $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 2.7\text{ k}\Omega$			$2/f_{\text{MCK}} + 428$	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 3.3\text{ V}$ , $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ , $C_b = 30\text{ pF}$ , $R_b = 5.5\text{ k}\Omega$			$2/f_{\text{MCK}} + 1146$	ns

(Notes, Caution and Remarks are listed on the next page.)

R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,  
 R5F100LJABG  
 R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,  
 R5F101LJABG  
 R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,  
 R5F100LJGBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03



Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I <sup>2</sup> C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I <sup>2</sup> C mode) (2/2)
		109	Addition of (1) I <sup>2</sup> C standard mode
		111	Addition of (2) I <sup>2</sup> C fast mode
		112	Addition of (3) I <sup>2</sup> C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)

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