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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	13
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1016easp-v0

1.2 List of Part Numbers

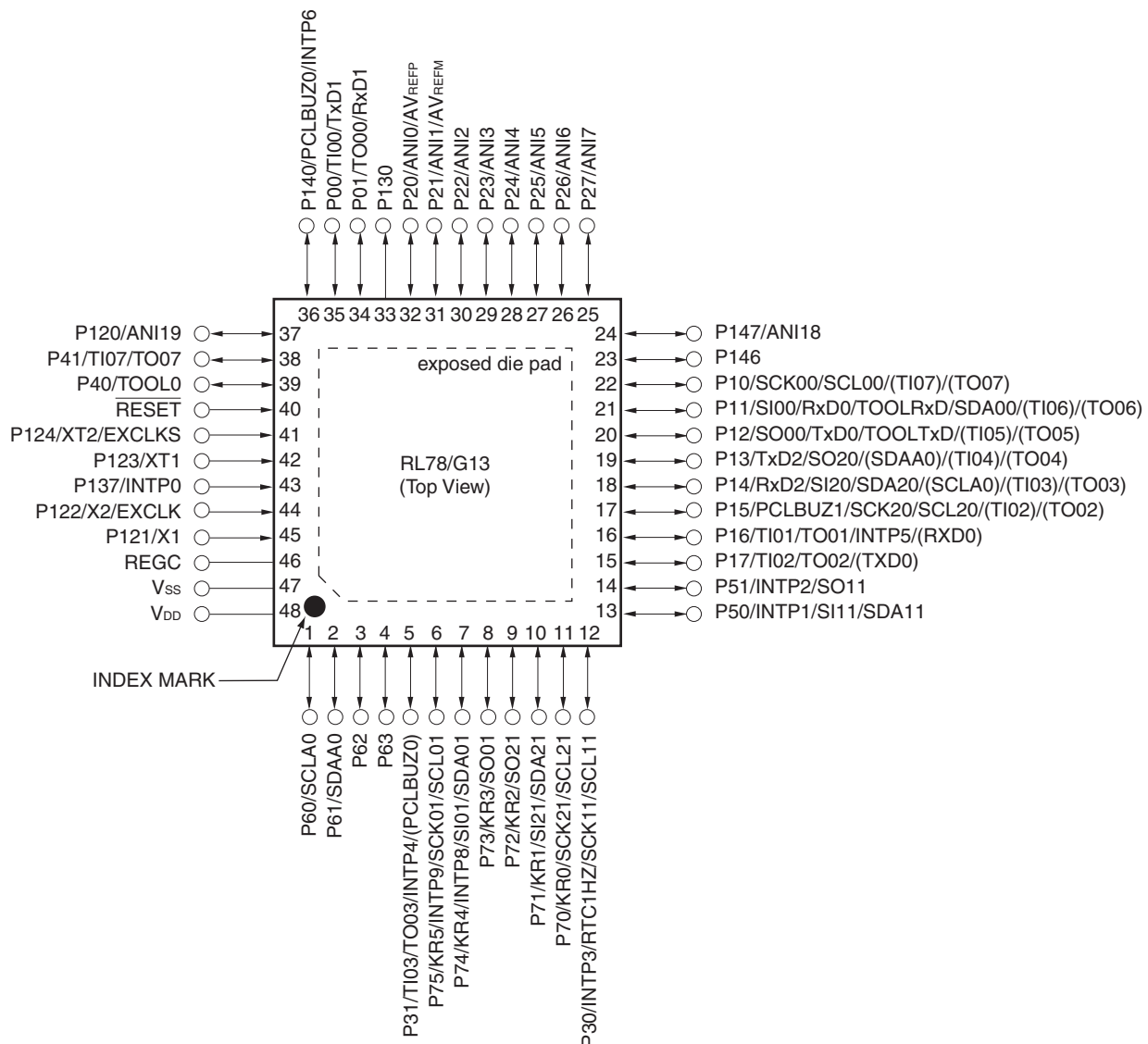**Figure 1-1. Part Number, Memory Size, and Package of RL78/G13**

Part No. R 5 F 1 0 0 L E A x x x F B #V0

Packaging specification
- #U0 : Tray (HWQFN,VFBGA,WFLGA)
- #V0 : Tray (LFQFP,LQFP,LSSOP)
- #W0 : Embossed Tape (HWQFN,VFBGA,WFLGA)
- #X0 : Embossed Tape (LFQFP, LQFP, LSSOP)

Package type:
- SP: LSSOP, 0.65 mm pitch
- FP : LFQFP, 0.80 mm pitch
- FA : LFQFP, 0.65 mm pitch
- FB : LFQFP, 0.50 mm pitch
- NA : HWQFN, 0.50 mm pitch
- LA : WFLGA, 0.50 mm pitch [Note 1]
- BG : VFBGA, 0.40 mm pitch [Note 1]

ROM number (Omitted with blank products)

Fields of application:
- A : Consumer applications, operating ambient temperature : -40°C to +85°C
- D : Industrial applications, operating ambient temperature : -40°C to +85°C
- G : Industrial applications, operating ambient temperature : -40°C to +105°C

ROM capacity:
- A :   16 KB
- C :   32 KB
- D :   48 KB
- E :   64 KB
- F :   96 KB
- G : 128 KB
- H : 192 KB
- J : 256 KB
- K : 384 KB [Note 2]
- L : 512 KB [Note 2]

Pin count:
- 6 : 20-pin
- 7 : 24-pin
- 8 : 25-pin [Note 1]
- A : 30-pin
- B : 32-pin
- C : 36-pin [Note 1]
- E : 40-pin
- F : 44-pin
- G : 48-pin
- J : 52-pin
- L : 64-pin
- M : 80-pin
- P : 100-pin
- S : 128-pin [Note 2]

RL78/G13 group
- 100 : Data flash is provided
- 101 : Data flash is not provided [Note 2]

Memory type:
- F : Flash memory

Renesas MCU

Renesas semiconductor product

Notes **1.** Products only for "A: Consumer applications (T$_A$ = −40 to +85°C)", and "G: Industrial applications (T$_A$ = −40 to +105°C)"
  2. Products only for "A: Consumer applications (T$_A$ = −40 to +85°C)", and "D: Industrial applications (T$_A$ = −40 to +85°C)"

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A	R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAFA#X0, R5F100JLAFA#X0
			D	R5F100JCDFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDFA#V0, R5F100JGDFA#V0, R5F100JHDFA#V0, R5F100JJDFA#V0, R5F100JKDFA#V0, R5F100JLDFA#V0 R5F100JCDFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDFA#X0, R5F100JGDFA#X0, R5F100JHDFA#X0, R5F100JJDFA#X0, R5F100JKDFA#X0, R5F100JLDFA#X0
			G	R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0,R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0,R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0
		Not mounted	A	R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAFA#X0, R5F101JLAFA#X0
			D	R5F101JCDFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDFA#V0, R5F101JGDFA#V0, R5F101JHDFA#V0, R5F101JJDFA#V0, R5F101JKDFA#V0, R5F101JLDFA#V0 R5F101JCDFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDFA#X0, R5F101JGDFA#X0, R5F101JHDFA#X0, R5F101JJDFA#X0, R5F101JKDFA#X0, R5F101JLDFA#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)

Pins (top side, left to right): P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Top pin numbers: 36 35 34 33 32 31 30 29 28 27 26 25

Left side:
- P120/ANI19 — 37
- P41/TI07/TO07 — 38
- P40/TOOL0 — 39
- $\overline{\text{RESET}}$ — 40
- P124/XT2/EXCLKS — 41
- P123/XT1 — 42
- P137/INTP0 — 43
- P122/X2/EXCLK — 44
- P121/X1 — 45
- REGC — 46
- V$_{SS}$ — 47
- V$_{DD}$ — 48

Center label: exposed die pad / RL78/G13 (Top View)

Right side:
- 24 — P147/ANI18
- 23 — P146
- 22 — P10/SCK00/SCL00/(TI07)/(TO07)
- 21 — P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 — P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 — P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 — P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 — P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 — P16/TI01/TO01/INTP5/(RXD0)
- 15 — P17/TI02/TO02/(TXD0)
- 14 — P51/INTP2/SO11
- 13 — P50/INTP1/SI11/SDA11

Bottom pin numbers: 1 2 3 4 5 6 7 8 9 10 11 12

INDEX MARK

Bottom pins (left to right): P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to Vss.

- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)

RL78/G13
(Top View)

Top pins (80–51):
P140/PCLBUZ0/INTP6, P141/PCLBUZ1/INTP7, P142/SCK30/SCL30, P143/SI30/RxD3/SDA30, P144/SO30/TxD3, P145/TI07/TO07, P00/TI00, P01/TO00, P02/ANI17/SO10/TxD1, P03/ANI16/SI10/RxD1/SDA10, P04/SCK10/SCL10, P102/TI06/TO06, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7, P150/ANI8, P151/ANI9, P152/ANI10, P153/ANI11, P154/ANI12, P155/ANI13, P156/ANI14, P100/ANI20, P147/ANI18

Left pins (81–100):
- 81 P120/ANI19
- 82 P47/INTP2
- 83 P46/INTP1/TI05/TO05
- 84 P45/SO01
- 85 P44/SI01/SDA01
- 86 P43/SCK01/SCL01
- 87 P42/TI04/TO04
- 88 P41
- 89 P40/TOOL0
- 90 RESET
- 91 P124/XT2/EXCLKS
- 92 P123/XT1
- 93 P137/INTP0
- 94 P122/X2/EXCLK
- 95 P121/X1
- 96 REGC
- 97 V$_{SS}$
- 98 EV$_{SS0}$
- 99 V$_{DD}$
- 100 EV$_{DD0}$

Right pins (50–31):
- 50 P146/(INTP4)
- 49 P111/(INTP11)
- 48 P110/(INTP10)
- 47 P101
- 46 P10/SCK00/SCL00/(TI07)/(TO07)
- 45 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 44 P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)
- 43 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 42 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 41 P15/SCK20/SCL20/(TI02)/(TO02)
- 40 P16/TI01/TO01/INTP5/(SI00)/(RXD0)
- 39 P17/TI02/TO02/(SO00)/(TXD0)
- 38 P57/(INTP3)
- 37 P56/(INTP1)
- 36 P55/(PCLBUZ1)/(SCK00)
- 35 P54/SCK31/SCL31
- 34 P53/SI31/SDA31
- 33 P52/SO31
- 32 P51/SO11
- 31 P50/SI11/SDA11

Bottom pins (1–30):
P60/SCLA0, P61/SDAA0, P62/SCLA1, P63/SDAA1, P31/TI03/TO03/INTP4/(PCLBUZ0), P64/TI10/TO10, P65/TI11/TO11, P66/TI12/TO12, P67/TI13/TO13, P77/KR7/INTP11/(TXD2), P76/KR6/INTP10/(RXD2), P75/KR5/INTP9, P74/KR4/INTP8, P73/KR3, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P06, P05, EV$_{SS1}$, P80/(SCK10)/(SCL10), P81/(SI10)/(RXD1)/(SDA10), P82/(SO10)/(TXD1), P83, P84/(INTP6), P85/(INTP7), P86/(INTP8), P87/(INTP9), P30/INTP3/RTC1HZ/SCK11/SCL11, EV$_{DD1}$

Cautions　1. **Make EV$_{SS0}$, EV$_{SS1}$ pins the same potential as V$_{SS}$ pin.**
2. **Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$, EV$_{DD1}$ pins (EV$_{DD0}$ = EV$_{DD1}$).**
3. **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks　1. For pin identification, see **1.4 Pin Identification**.
2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$, EV$_{DD0}$ and EV$_{DD1}$ pins and connect the V$_{SS}$, EV$_{SS0}$ and EV$_{SS1}$ pins to separate ground lines.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T_A = –40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (5/5)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV$_{DD0}$				1	μA
	I_{LIH2}	P20 to P27, P137, P150 to P156, $\overline{RESET}$	V_I = V$_{DD}$				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I_{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV$_{SS0}$				−1	μA
	I_{LIL2}	P20 to P27, P137, P150 to P156, $\overline{RESET}$	V_I = V$_{SS}$				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V$_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R_U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V_I = EV$_{SS0}$, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

RENESAS

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. When high-speed on-chip oscillator and subsystem clock are stopped.

    3. When high-speed system clock and subsystem clock are stopped.

    4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

    5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

         HS (high-speed main) mode: 2.7 V $\leq$ V_{DD} $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                        2.4 V $\leq$ V_{DD} $\leq$ 5.5 V @ 1 MHz to 16 MHz

         LS (low-speed main) mode: 1.8 V $\leq$ V_{DD} $\leq$ 5.5 V @ 1 MHz to 8 MHz

         LV (low-voltage main) mode: 1.6 V $\leq$ V_{DD} $\leq$ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f_{MX}:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

        2. f_{IH}:   High-speed on-chip oscillator clock frequency

        3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

        4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	1.86	mA
					V$_{DD}$ = 3.0 V		0.62	1.86	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	1.45	mA
					V$_{DD}$ = 3.0 V		0.50	1.45	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.11	mA
					V$_{DD}$ = 3.0 V		0.44	1.11	mA
			LS (low-speed main) mode [Note 7]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		290	620	μA
					V$_{DD}$ = 2.0 V		290	620	μA
			LV (low-voltage main) mode [Note 7]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		440	680	μA
					V$_{DD}$ = 2.0 V		440	680	μA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
			LS (low-speed main) mode [Note 7]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.19	0.52	μA
			T$_A$ = +25°C				0.25	0.52	μA
			T$_A$ = +50°C				0.32	2.21	μA
			T$_A$ = +70°C				0.55	3.94	μA
			T$_A$ = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

AC Timing Test Points
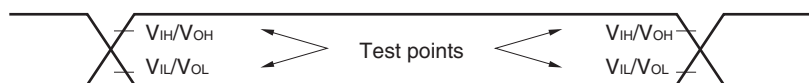
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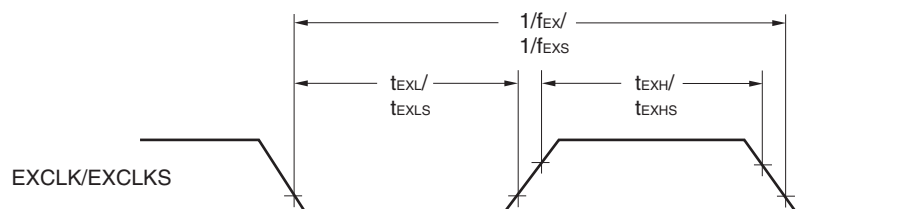
TI/TO Timing
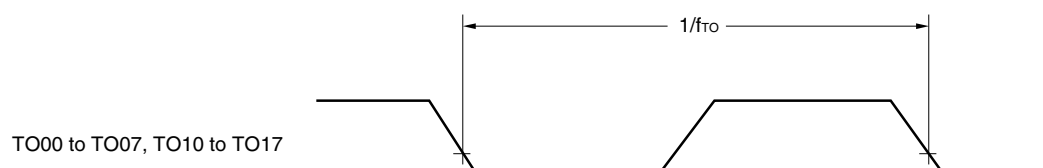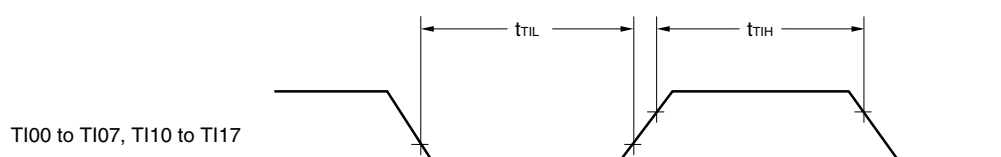
Interrupt Request Input Timing
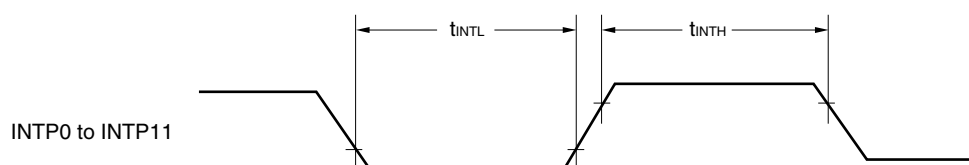
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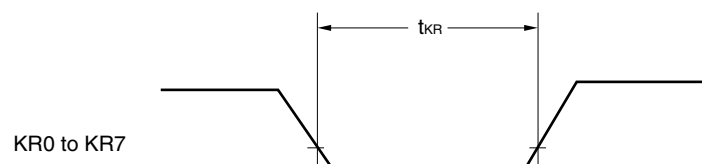
RESET Input Timing
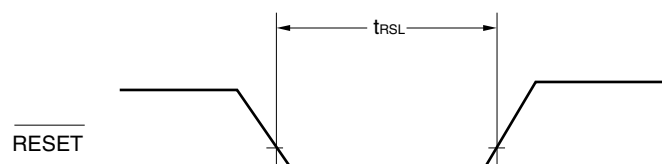
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
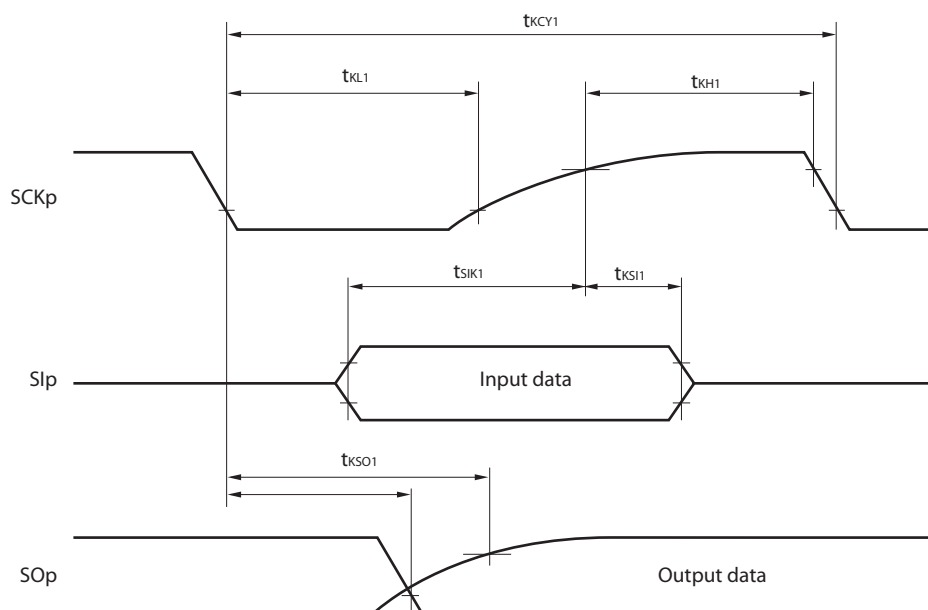
SCKp

t_{KCY1}
t_{KL1}
t_{KH1}

SIp

t_{SIK1}
t_{KSI1}

Input data

SOp

t_{KSO1}

Output data

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

SCKp

t_{KCY1}
t_{KH1}
t_{KL1}

SIp

t_{SIK1}
t_{KSI1}

Input data

SOp

t_{KSO1}

Output data
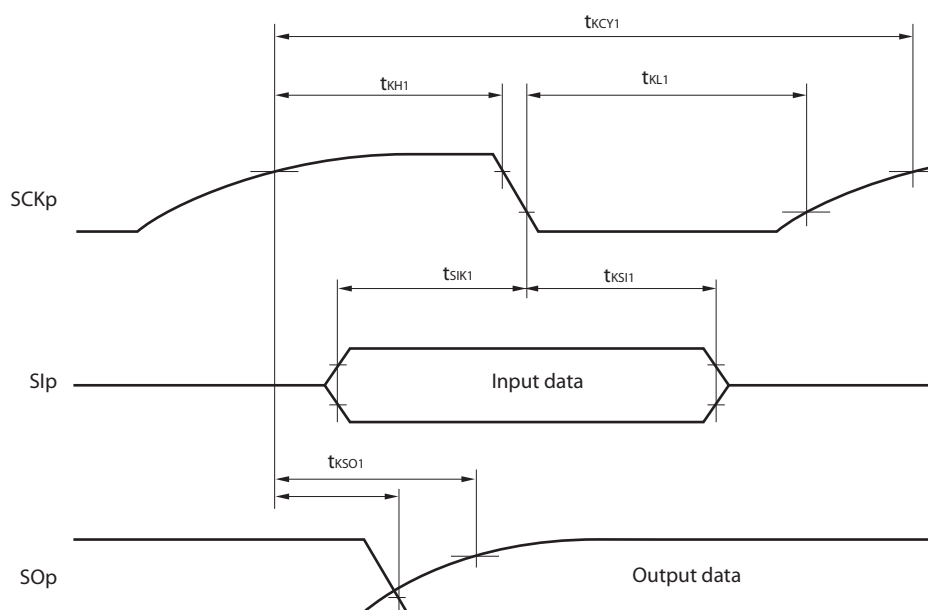
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(2) I^2C fast mode

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: $f_{CLK} \geq$ 3.5 MHz	2.7 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EV_{DD0} ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time[Note 1]	$t_{HD:STA}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Hold time when SCLA0 = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
Hold time when SCLA0 = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		100		100		100		μs
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0	0.9	0	0.9	0	0.9	μs
Setup time of stop condition	$t_{SU:STO}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		0.6		0.6		0.6		μs
Bus-free time	t_{BUF}	2.7 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		1.3		1.3		1.3		μs

Notes   **1.**   The first clock pulse is generated after this period when the start/restart condition is detected.

         2.   The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

<R>

Caution   **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Remark   The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

         Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI14	Refer to **2.6.1 (1)**.	Refer to **2.6.1 (3)**.	Refer to **2.6.1 (4)**.
ANI16 to ANI26	Refer to **2.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **2.6.1 (1)**.		−

(1) When reference voltage (+)= AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±0.50	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±5.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	1.8 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
			1.6 V ≤ AV$_{REFP}$ ≤ 5.5 V [Note 4]			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$[Note 5]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$[Note 5]		V

(**Notes** are listed on the next page.)

LVD Detection Voltage of Interrupt & Reset Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDA0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V$_{LVDA1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V$_{LVDA2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V$_{LVDA3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V$_{LVDB0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V$_{LVDB1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V$_{LVDB2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V$_{LVDB3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V$_{LVDC0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V$_{LVDC1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V$_{LVDC2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V$_{LVDC3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution **Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (high-speed main) mode [Note 5]	f$_{IH}$ = 32 MHz [Note 3]	Basic operation	V$_{DD}$ = 5.0 V		2.3		mA
						V$_{DD}$ = 3.0 V		2.3		mA
					Normal operation	V$_{DD}$ = 5.0 V		5.2	9.2	mA
						V$_{DD}$ = 3.0 V		5.2	9.2	mA
				f$_{IH}$ = 24 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		4.1	7.0	mA
						V$_{DD}$ = 3.0 V		4.1	7.0	mA
				f$_{IH}$ = 16 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		3.0	5.0	mA
						V$_{DD}$ = 3.0 V		3.0	5.0	mA
			HS (high-speed main) mode [Note 5]	f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = −40°C	Normal operation	Square wave input		4.8	5.9	µA
						Resonator connection		4.9	6.0	µA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C	Normal operation	Square wave input		4.9	5.9	µA
						Resonator connection		5.0	6.0	µA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C	Normal operation	Square wave input		5.0	7.6	µA
						Resonator connection		5.1	7.7	µA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C	Normal operation	Square wave input		5.2	9.3	µA
						Resonator connection		5.3	9.4	µA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C	Normal operation	Square wave input		5.7	13.3	µA
						Resonator connection		5.8	13.4	µA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +105°C	Normal operation	Square wave input		10.0	46.0	µA
						Resonator connection		10.0	46.0	µA

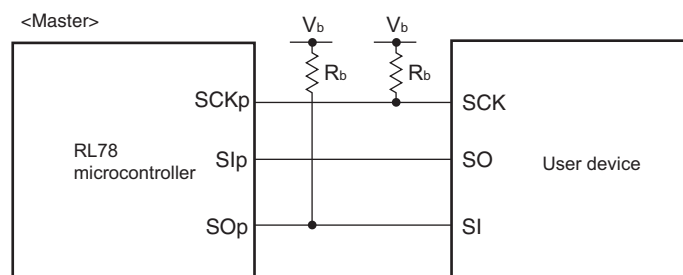(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

   2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

TI/TO Timing
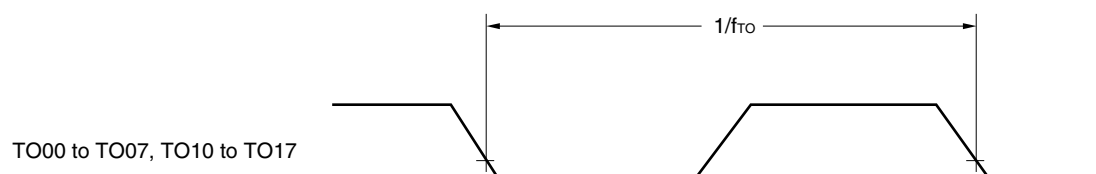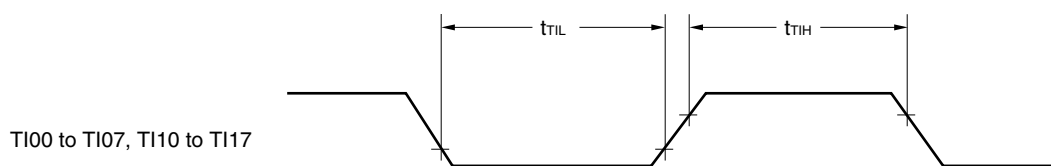
TI00 to TI07, TI10 to TI17

TO00 to TO07, TO10 to TO17

Interrupt Request Input Timing

INTP0 to INTP11

Key Interrupt Input Timing

KR0 to KR7
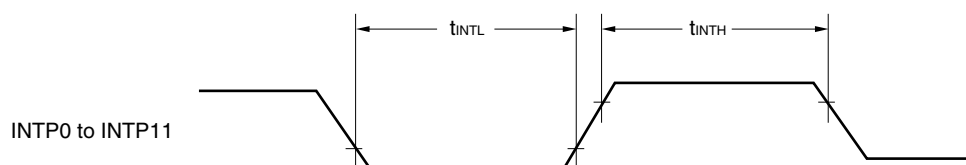
$\overline{\text{RESET}}$ **Input Timing**

$\overline{\text{RESET}}$

CSI mode connection diagram (during communication at different potential)

Remarks **1.** R$_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, C$_b$[F]: Communication line (SCKp, SOp) load capacitance, V$_b$[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

RENESAS

3.5.2 Serial interface IICA

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f$_{SCL}$	Fast mode: f$_{CLK}$ ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f$_{CLK}$ ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t$_{SU:STA}$		4.7		0.6		μs
Hold time[Note 1]	t$_{HD:STA}$		4.0		0.6		μs
Hold time when SCLA0 = "L"	t$_{LOW}$		4.7		1.3		μs
Hold time when SCLA0 = "H"	t$_{HIGH}$		4.0		0.6		μs
Data setup time (reception)	t$_{SU:DAT}$		250		100		ns
Data hold time (transmission)[Note 2]	t$_{HD:DAT}$		0	3.45	0	0.9	μs
Setup time of stop condition	t$_{SU:STO}$		4.0		0.6		μs
Bus-free time	t$_{BUF}$		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of t$_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I$_{OH1}$, I$_{OL1}$, V$_{OH1}$, V$_{OL1}$) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C$_b$ = 400 pF, R$_b$ = 2.7 kΩ
Fast mode: C$_b$ = 320 pF, R$_b$ = 1.1 kΩ

IICA serial transfer timing
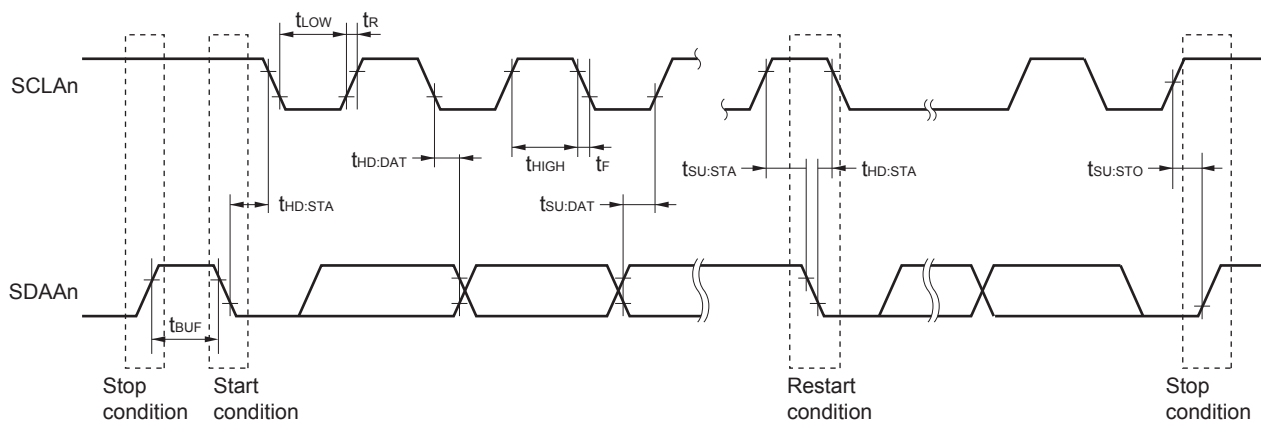
Remark n = 0, 1

3.10 Timing of Entry to Flash Memory Programming Modes

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t$_{SUINIT}$	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t$_{SU}$	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t$_{HD}$	POR and LVD reset must be released before the external reset is released.	1			ms
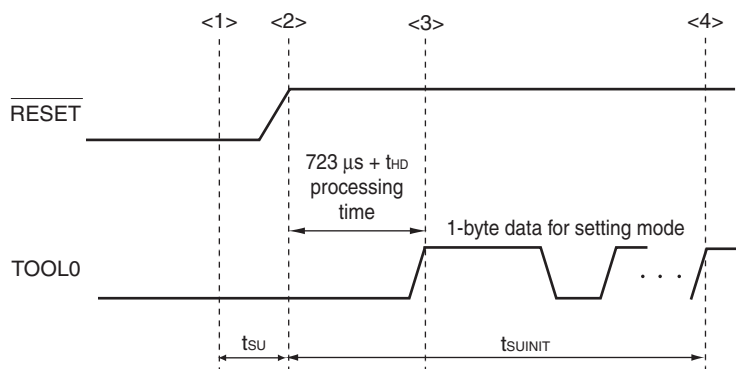
<1> The low level is input to the TOOL0 pin.
<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t$_{SUINIT}$: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

  t$_{SU}$: Time to release the external reset after the TOOL0 pin is set to the low level

  t$_{HD}$: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.