What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

| Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	15
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 6x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	25-WFLGA
Supplier Device Package	25-LGA (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f1018eala-u0

Table 1-1. List of Ordering Part Numbers

(4/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)	Mounted	A	R5F100FAAFP#V0, R5F100FCAFP#V0, R5F100FDAFP#V0, R5F100FEAFP#V0, R5F100FFAFP#V0, R5F100FGAFP#V0, R5F100FHAFP#V0, R5F100FJAFP#V0, R5F100FKAFP#V0, R5F100FLAFP#V0 R5F100FAAFP#X0, R5F100FCAFP#X0, R5F100FDAFP#X0, R5F100FEAFP#X0, R5F100FFAFP#X0, R5F100FGAFP#X0, R5F100FHAFP#X0, R5F100FJAFP#X0, R5F100FKAFP#X0, R5F100FLAFP#X0
			D	R5F100FADFP#V0, R5F100FCDFP#V0, R5F100FDDFP#V0, R5F100FEDFP#V0, R5F100FFDFP#V0, R5F100FGDFP#V0, R5F100FHDFP#V0, R5F100FJDFP#V0, R5F100FKDFP#V0, R5F100FLDFP#V0 R5F100FADFP#X0, R5F100FCDFP#X0, R5F100FDDFP#X0, R5F100FEDFP#X0, R5F100FFDFP#X0, R5F100FGDFP#X0, R5F100FHDFP#X0, R5F100FJDFP#X0, R5F100FKDFP#X0, R5F100FLDFP#X0
			G	R5F100FAGFP#V0, R5F100FCGFP#V0, R5F100FDGFP#V0, R5F100FEGFP#V0, R5F100FFGFP#V0, R5F100FGGFP#V0, R5F100FHGFP#V0, R5F100FJGFP#V0 R5F100FAGFP#X0, R5F100FCGFP#X0, R5F100FDGFP#X0, R5F100FEGFP#X0, R5F100FFGFP#X0, R5F100FGGFP#X0, R5F100FHGFP#X0, R5F100FJGFP#X0
		Not mounted	A	R5F101FAAFP#V0, R5F101FCAFP#V0, R5F101FDAFP#V0, R5F101FEAFP#V0, R5F101FFAFP#V0, R5F101FGAFP#V0, R5F101FHAFP#V0, R5F101FJAFP#V0, R5F101FKAFP#V0, R5F101FLAFP#V0 R5F101FAAFP#X0, R5F101FCAFP#X0, R5F101FDAFP#X0, R5F101FEAFP#X0, R5F101FFAFP#X0, R5F101FGAFP#X0, R5F101FHAFP#X0, R5F101FJAFP#X0, R5F101FKAFP#X0, R5F101FLAFP#X0
			D	R5F101FADFP#V0, R5F101FCDFP#V0, R5F101FDDFP#V0, R5F101FEDFP#V0, R5F101FFDFP#V0, R5F101FGDFP#V0, R5F101FHDFP#V0, R5F101FJDFP#V0, R5F101FKDFP#V0, R5F101FLDFP#V0 R5F101FADFP#X0, R5F101FCDFP#X0, R5F101FDDFP#X0, R5F101FEDFP#X0, R5F101FFDFP#X0, R5F101FGDFP#X0, R5F101FHDFP#X0, R5F101FJDFP#X0, R5F101FKDFP#X0, R5F101FLDFP#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)
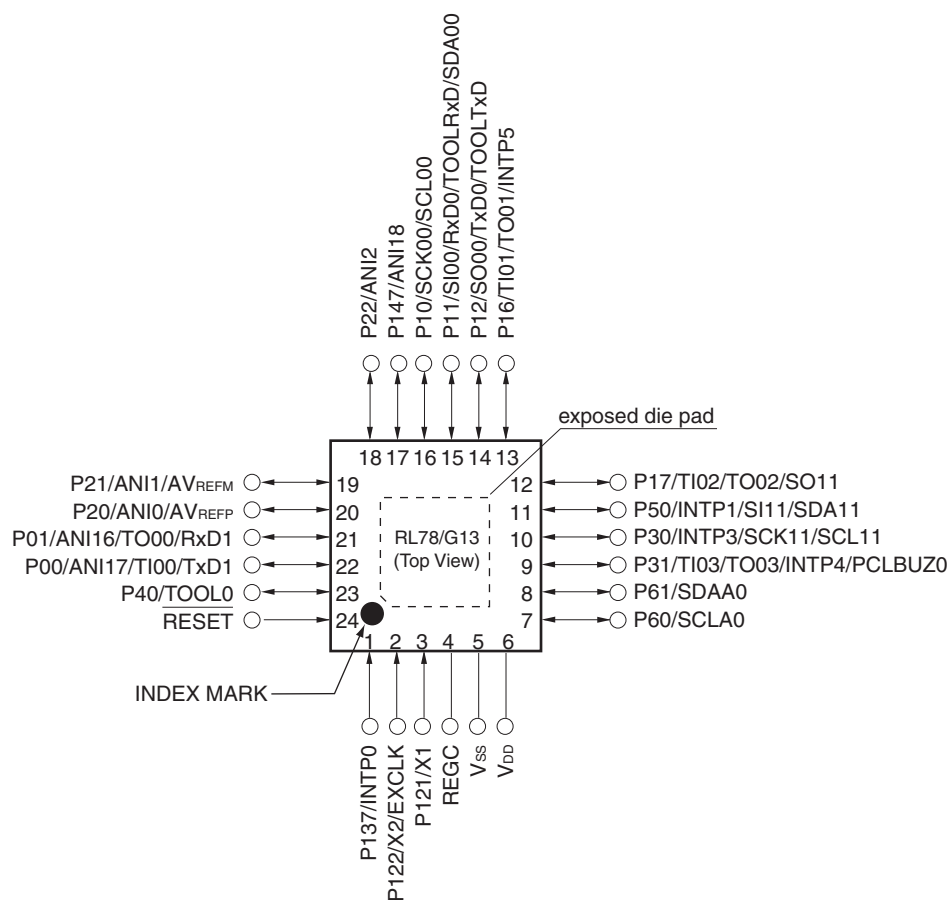
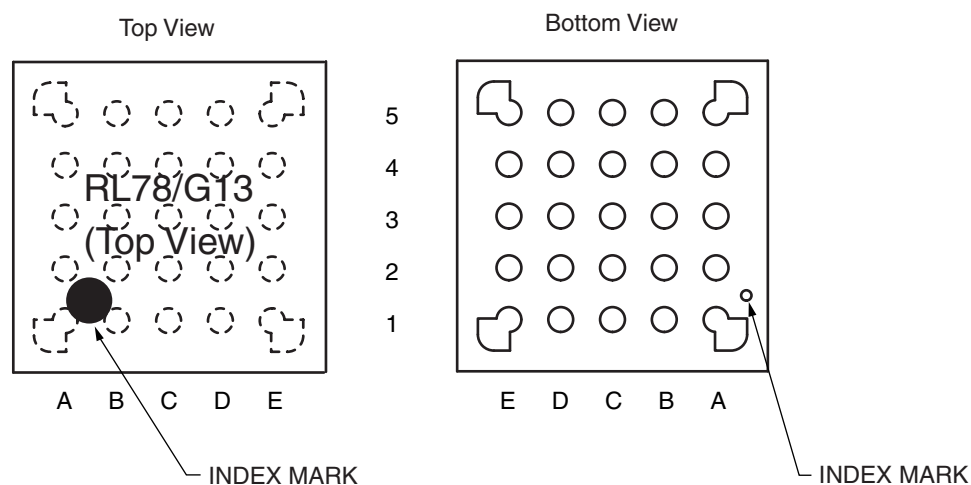**Caution** **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks 1. For pin identification, see **1.4 Pin Identification**.

      2. It is recommended to connect an exposed die pad to Vss.

1.3.3 25-pin products
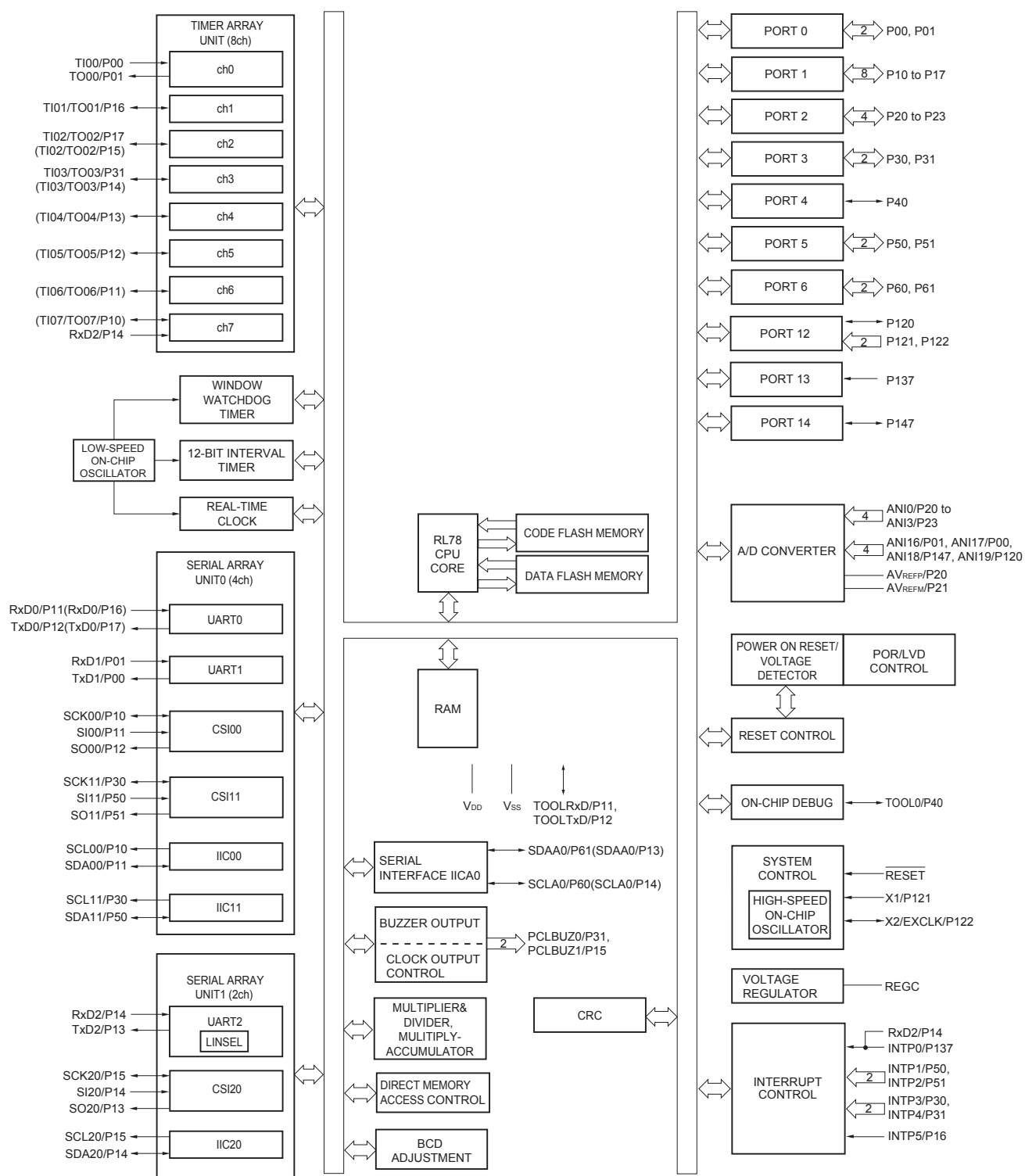
- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

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Top View   Bottom View

INDEX MARK   INDEX MARK

	A	B	C	D	E	
5	P40/TOOL0	$\overline{\text{RESET}}$	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AV_{REFM}	P10/SCK00/ SCL00	4
3	P121/X1	V_{DD}	P20/ANI0/ AV_{REFP}	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V_{SS}	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

Caution   **Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remark   For pin identification, see **1.4 Pin Identification**.

1.5.4 30-pin products

TIMER ARRAY UNIT (8ch)
- TI00/P00, TO00/P01 — ch0
- TI01/TO01/P16 — ch1
- TI02/TO02/P17 (TI02/TO02/P15) — ch2
- TI03/TO03/P31 (TI03/TO03/P14) — ch3
- (TI04/TO04/P13) — ch4
- (TI05/TO05/P12) — ch5
- (TI06/TO06/P11) — ch6
- (TI07/TO07/P10) RxD2/P14 — ch7

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12-BIT INTERVAL TIMER

REAL-TIME CLOCK

RL78 CPU CORE

CODE FLASH MEMORY

DATA FLASH MEMORY

SERIAL ARRAY UNIT0 (4ch)
- RxD0/P11(RxD0/P16), TxD0/P12(TxD0/P17) — UART0
- RxD1/P01, TxD1/P00 — UART1
- SCK00/P10, SI00/P11, SO00/P12 — CSI00
- SCK11/P30, SI11/P50, SO11/P51 — CSI11
- SCL00/P10, SDA00/P11 — IIC00
- SCL11/P30, SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)
- RxD2/P14, TxD2/P13 — UART2 (LINSEL)
- SCK20/P15, SI20/P14, SO20/P13 — CSI20
- SCL20/P15, SDA20/P14 — IIC20

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL — 2 PCLBUZ0/P31, PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

CRC

PORT 0 — 2 P00, P01
PORT 1 — 8 P10 to P17
PORT 2 — 4 P20 to P23
PORT 3 — 2 P30, P31
PORT 4 — P40
PORT 5 — 2 P50, P51
PORT 6 — 2 P60, P61
PORT 12 — P120, 2 P121, P122
PORT 13 — P137
PORT 14 — P147

A/D CONVERTER
- 4 ANI0/P20 to ANI3/P23
- 4 ANI16/P01, ANI17/P00, ANI18/P147, ANI19/P120
- AV_{REFP}/P20
- AV_{REFM}/P21

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL — RESET
HIGH-SPEED ON-CHIP OSCILLATOR — X1/P121, X2/EXCLK/P122

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- RxD2/P14, INTP0/P137
- 2 INTP1/P50, INTP2/P51
- 2 INTP3/P30, INTP4/P31
- INTP5/P16

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output		−		1		1		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)												
8/10-bit resolution A/D converter		6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface		[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel												
	I²C bus	−		1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)												
DMA controller		2 channels												
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt		−												
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access												
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)												
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)												
On-chip debug function		Provided												
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)												
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)												

Note   The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

3. When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
	I^2C bus	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access									
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)									
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)									
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)									

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Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(TA = −40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (fx)[Note]	Crystal resonator		32	32.768	35	kHz

Note   Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(TA = −40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	fIH			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ VDD ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ VDD < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ VDD ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ VDD < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	fIL				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1.   High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

  2.   This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.54	1.63	mA
					V$_{DD}$ = 3.0 V		0.54	1.63	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.28	mA
					V$_{DD}$ = 3.0 V		0.44	1.28	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.40	1.00	mA
					V$_{DD}$ = 3.0 V		0.40	1.00	mA
			LS (low-speed main) mode [Note 7]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		260	530	μA
					V$_{DD}$ = 2.0 V		260	530	μA
			LV (low-voltage main) mode [Note 7]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		420	640	μA
					V$_{DD}$ = 2.0 V		420	640	μA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			LS (low-speed main) mode [Note 7]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.37	1.17	μA
					Resonator connection		0.56	1.36	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.53	1.97	μA
					Resonator connection		0.72	2.16	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		0.82	3.37	μA
					Resonator connection		1.01	3.56	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.18	0.50	μA
			T$_A$ = +25°C				0.23	0.50	μA
			T$_A$ = +50°C				0.30	1.10	μA
			T$_A$ = +70°C				0.46	1.90	μA
			T$_A$ = +85°C				0.75	3.30	μA

(**Notes** and **Remarks** are listed on the next page.)

Note The following conditions are required for low voltage interface when EV$_{DD0}$ < V$_{DD}$

1.8 V ≤ EV$_{DD0}$ < 2.7 V : MIN. 125 ns

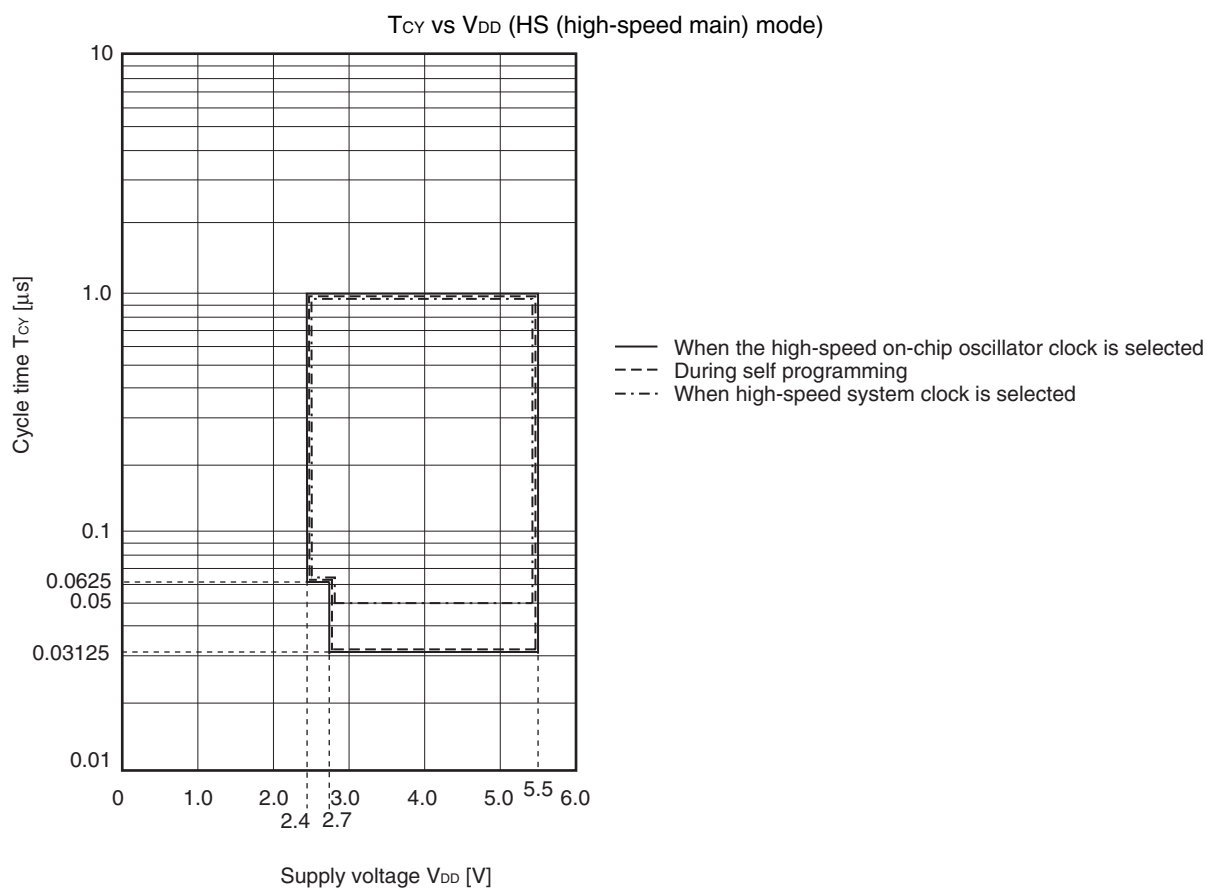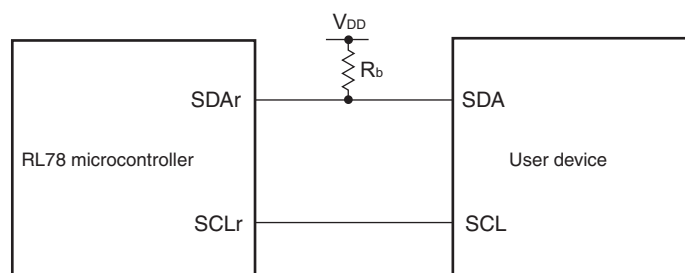1.6 V ≤ EV$_{DD0}$ < 1.8 V : MIN. 250 ns

Remark f$_{MCK}$: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

Minimum Instruction Execution Time during Main System Clock Operation

T$_{CY}$ vs V$_{DD}$ (HS (high-speed main) mode)

When the high-speed on-chip oscillator clock is selected
During self programming
When high-speed system clock is selected

Simplified I²C mode mode connection diagram (during communication at same potential)

V$_{DD}$

R$_b$

RL78 microcontroller

SDAr   SDA

User device

SCLr   SCL

Simplified I²C mode serial transfer timing (during communication at same potential)

1/f$_{SCL}$

t$_{LOW}$ t$_{HIGH}$

SCLr

SDAr

t$_{HD:DAT}$ t$_{SU:DAT}$
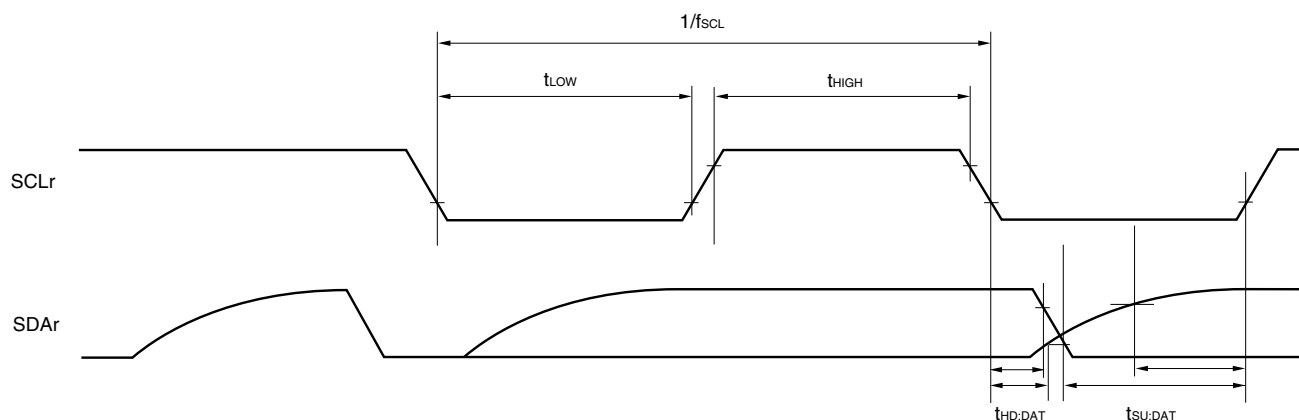
Remarks   **1.** R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

     2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
        h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

     3. f$_{MCK}$: Serial array unit operation clock frequency

        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

        n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		**Note 1**		**Note 1**		**Note 1**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 1.4 kΩ, V$_b$ = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		**Note 3**		**Note 3**		**Note 3**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 2.7 kΩ, V$_b$ = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		**Notes 5, 6**		**Notes 5, 6**		**Notes 5, 6**	bps
			Theoretical value of the maximum transfer rate C$_b$ = 50 pF, R$_b$ = 5.5 kΩ, V$_b$ = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Notes 1. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V and 2.7 V ≤ V$_b$ ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD1}$	Operating mode	HS (high-speed main) mode Note 5	f$_{IH}$ = 32 MHz Note 3	Basic operation	V$_{DD}$ = 5.0 V		2.1		mA
						V$_{DD}$ = 3.0 V		2.1		mA
					Normal operation	V$_{DD}$ = 5.0 V		4.6	7.5	mA
						V$_{DD}$ = 3.0 V		4.6	7.5	mA
				f$_{IH}$ = 24 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		3.7	5.8	mA
						V$_{DD}$ = 3.0 V		3.7	5.8	mA
				f$_{IH}$ = 16 MHz Note 3	Normal operation	V$_{DD}$ = 5.0 V		2.7	4.2	mA
						V$_{DD}$ = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode Note 5	f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 20 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 5.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				f$_{MX}$ = 10 MHz Note 2, V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = −40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				f$_{SUB}$ = 32.768 kHz Note 4 T$_A$ = +105°C	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                    2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = −40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode [Note 5]	f_{IH} = 32 MHz [Note 3]	Basic operation	V_{DD} = 5.0 V		2.3		mA
						V_{DD} = 3.0 V		2.3		mA
					Normal operation	V_{DD} = 5.0 V		5.2	9.2	mA
						V_{DD} = 3.0 V		5.2	9.2	mA
				f_{IH} = 24 MHz [Note 3]	Normal operation	V_{DD} = 5.0 V		4.1	7.0	mA
						V_{DD} = 3.0 V		4.1	7.0	mA
				f_{IH} = 16 MHz [Note 3]	Normal operation	V_{DD} = 5.0 V		3.0	5.0	mA
						V_{DD} = 3.0 V		3.0	5.0	mA
			HS (high-speed main) mode [Note 5]	f_{MX} = 20 MHz [Note 2], V_{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				f_{MX} = 20 MHz [Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				f_{MX} = 10 MHz [Note 2], V_{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
				f_{MX} = 10 MHz [Note 2], V_{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz [Note 4] T_A = −40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f_{SUB} = 32.768 kHz [Note 4] T_A = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f_{SUB} = 32.768 kHz [Note 4] T_A = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f_{SUB} = 32.768 kHz [Note 4] T_A = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f_{SUB} = 32.768 kHz [Note 4] T_A = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA
				f_{SUB} = 32.768 kHz [Note 4] T_A = +105°C	Normal operation	Square wave input		10.0	46.0	μA
						Resonator connection		10.0	46.0	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                                    2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T_A = −40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) [Note]	t_{SIK1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) [Note]	t_{KSI1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
Delay time from SCKp↓ to SOp output [Note]	t_{KSO1}	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	28/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	24/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	20/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	40/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	32/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	28/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	24/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V	24 MHz < f$_{MCK}$	96/f$_{MCK}$		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	72/f$_{MCK}$		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	64/f$_{MCK}$		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	52/f$_{MCK}$		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	32/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 4 MHz	20/f$_{MCK}$		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		t$_{KCY2}$/2 − 24		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		t$_{KCY2}$/2 − 36		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]		t$_{KCY2}$/2 − 100		ns
SIp setup time (to SCKp↑) [Note 2]	t$_{SIK2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V		1/f$_{MCK}$ + 40		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V		1/f$_{MCK}$ + 40		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V		1/f$_{MCK}$ + 60		ns
SIp hold time (from SCKp↑) [Note 3]	t$_{KSI2}$			1/f$_{MCK}$ + 62		ns
Delay time from SCKp↓ to SOp output [Note 4]	t$_{KSO2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ			2/f$_{MCK}$ + 240	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ			2/f$_{MCK}$ + 428	ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V C$_b$ = 30 pF, R$_b$ = 5.5 kΩ			2/f$_{MCK}$ + 1146	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI26	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		−

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage
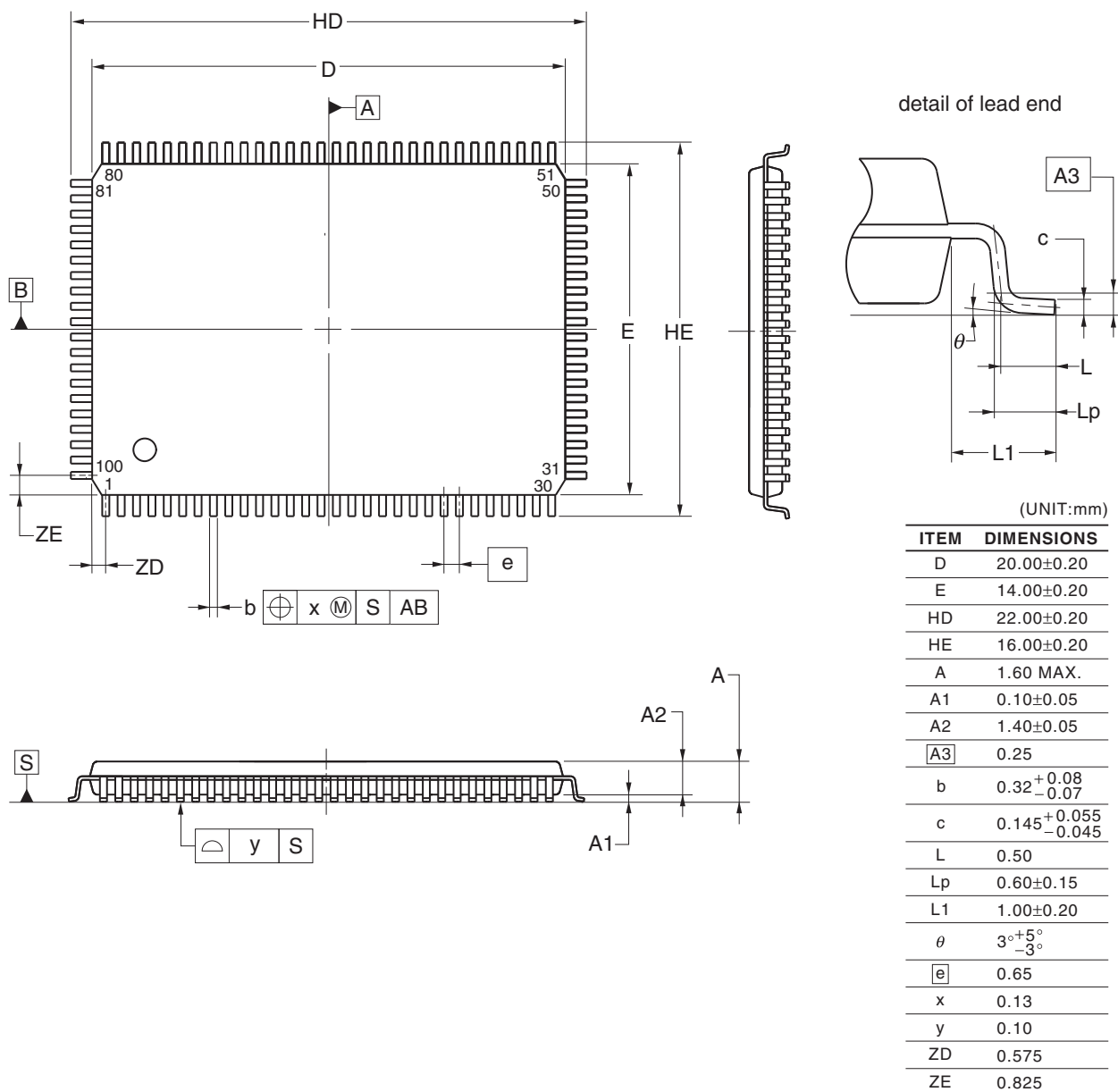
(T$_A$ = −40 to +105°C, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage output (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 4]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 4]		V

(**Notes** are listed on the next page.)

R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAFA, R5F100PKAFA, R5F100PLAFA
R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAFA, R5F101PKAFA, R5F101PLAFA
R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA
R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA
R5F100PFGFA, R5F100PGGFA, R5F100PHGFA, R5F100PJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92

detail of lead end

(UNIT:mm)

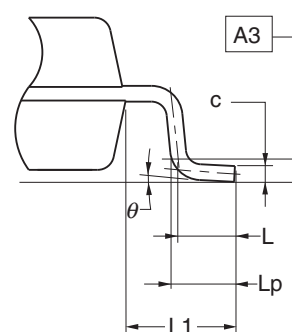| ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	$0.32^{+0.08}_{-0.07}$
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.65
x	0.13
y	0.10
ZD	0.575
ZE	0.825

4.14 128-pin Products

R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB
R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB
R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92
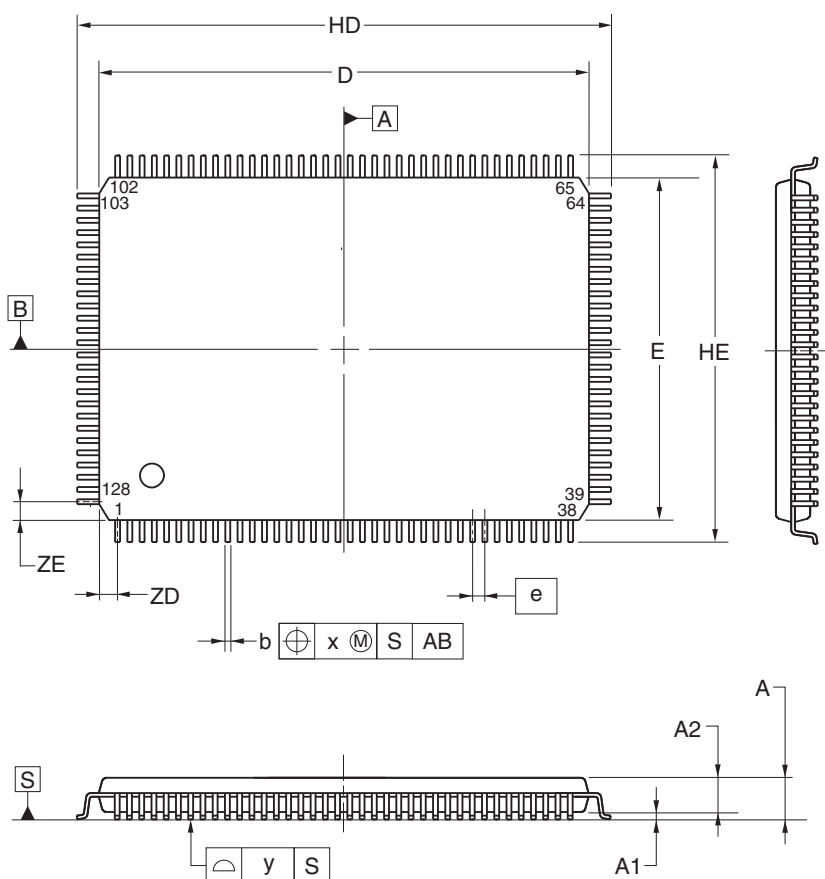
detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75