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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	21
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101addsp-v0

1.3.8　44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)
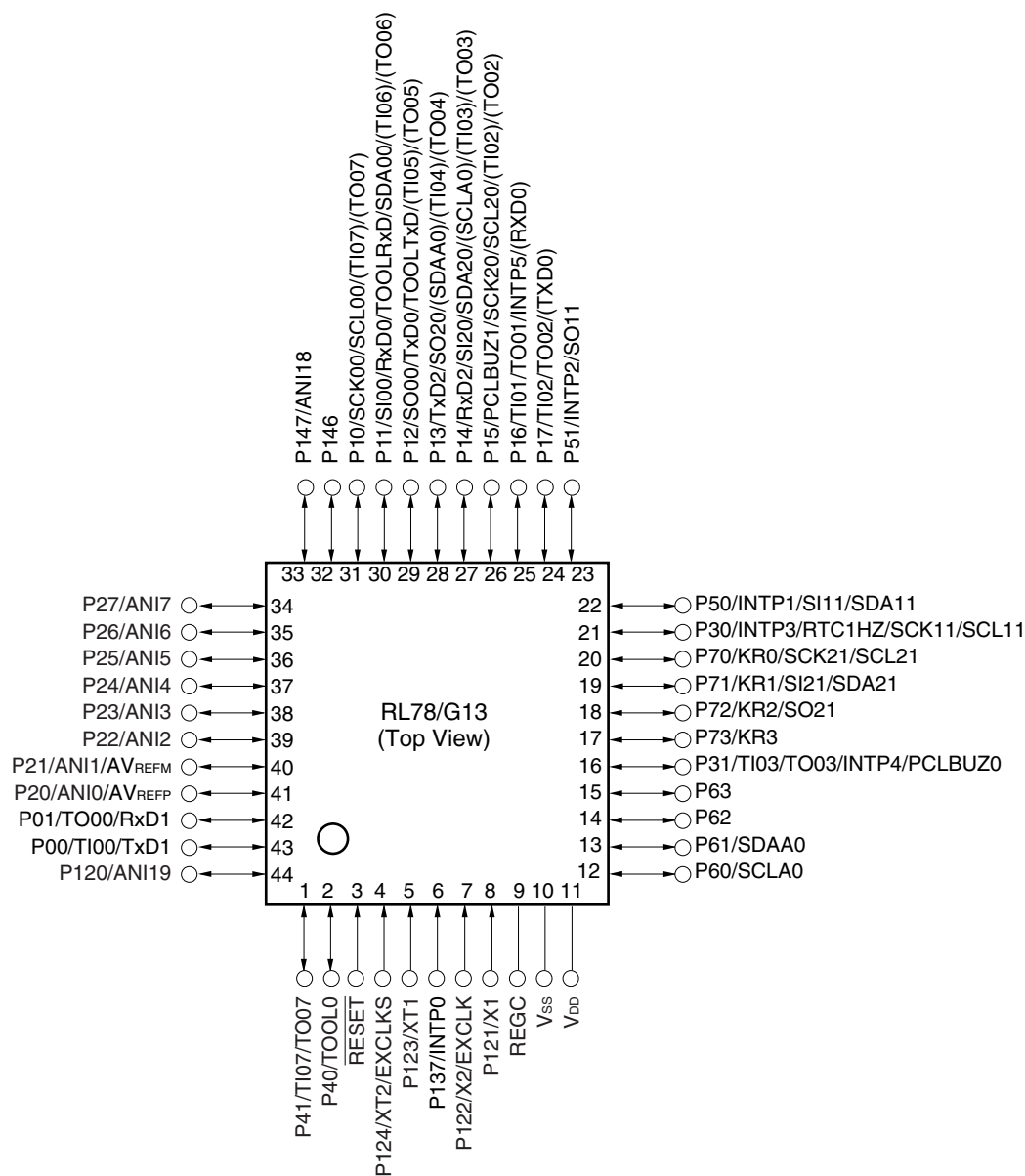
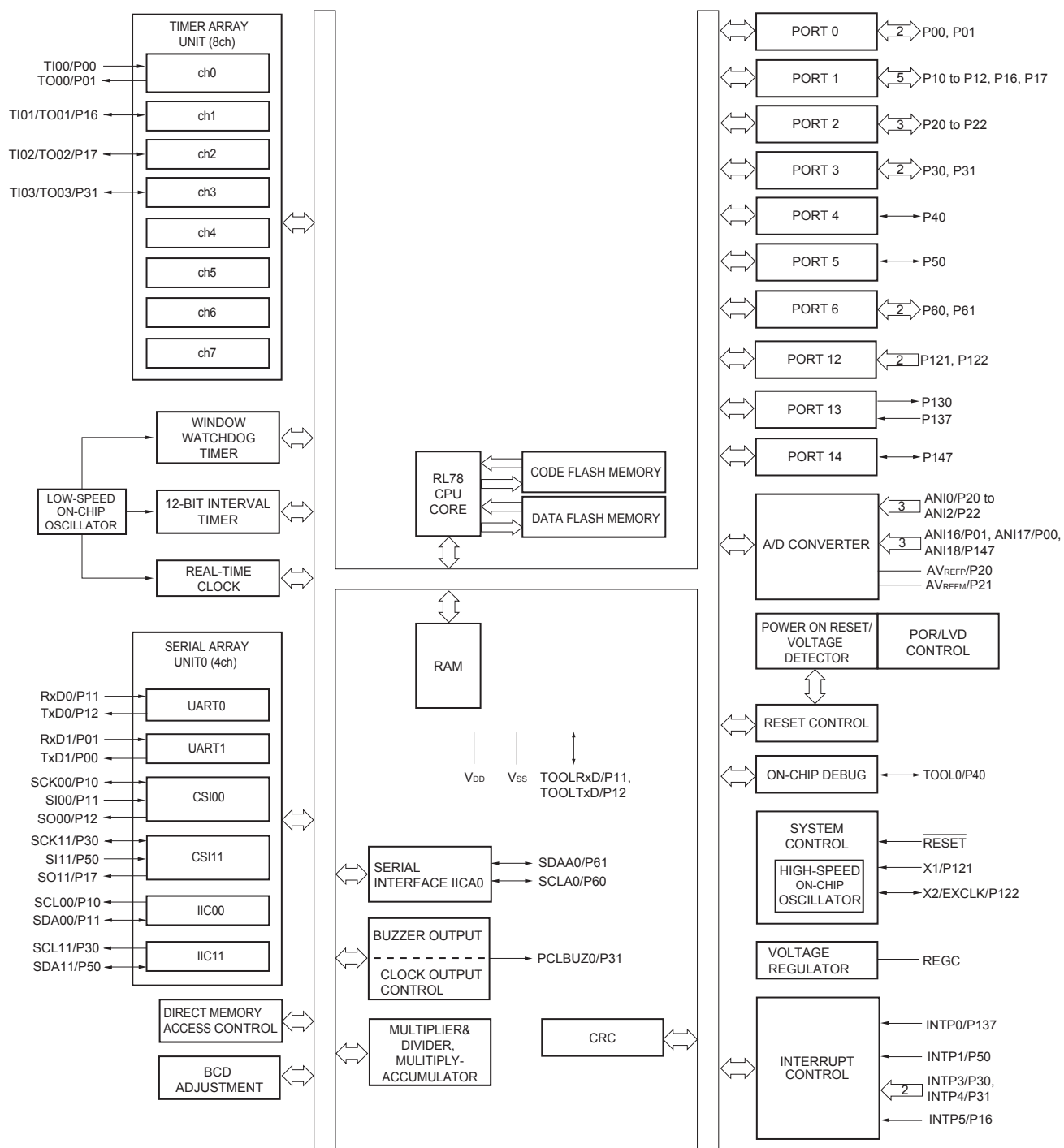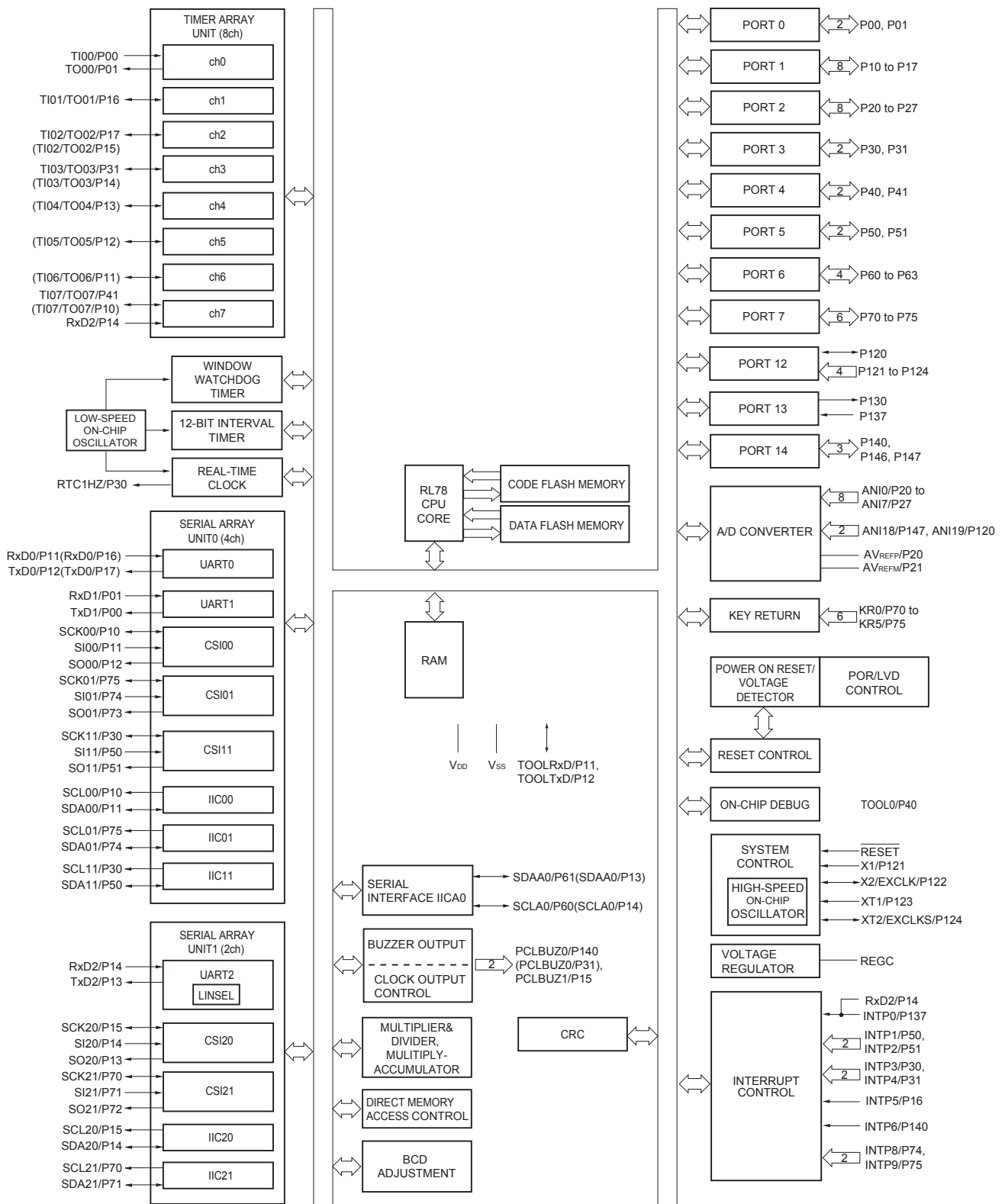**Caution　Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

Remarks 1. For pin identification, see **1.4　Pin Identification**.

　　　　　2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).　Refer to **Figure 4-8　Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
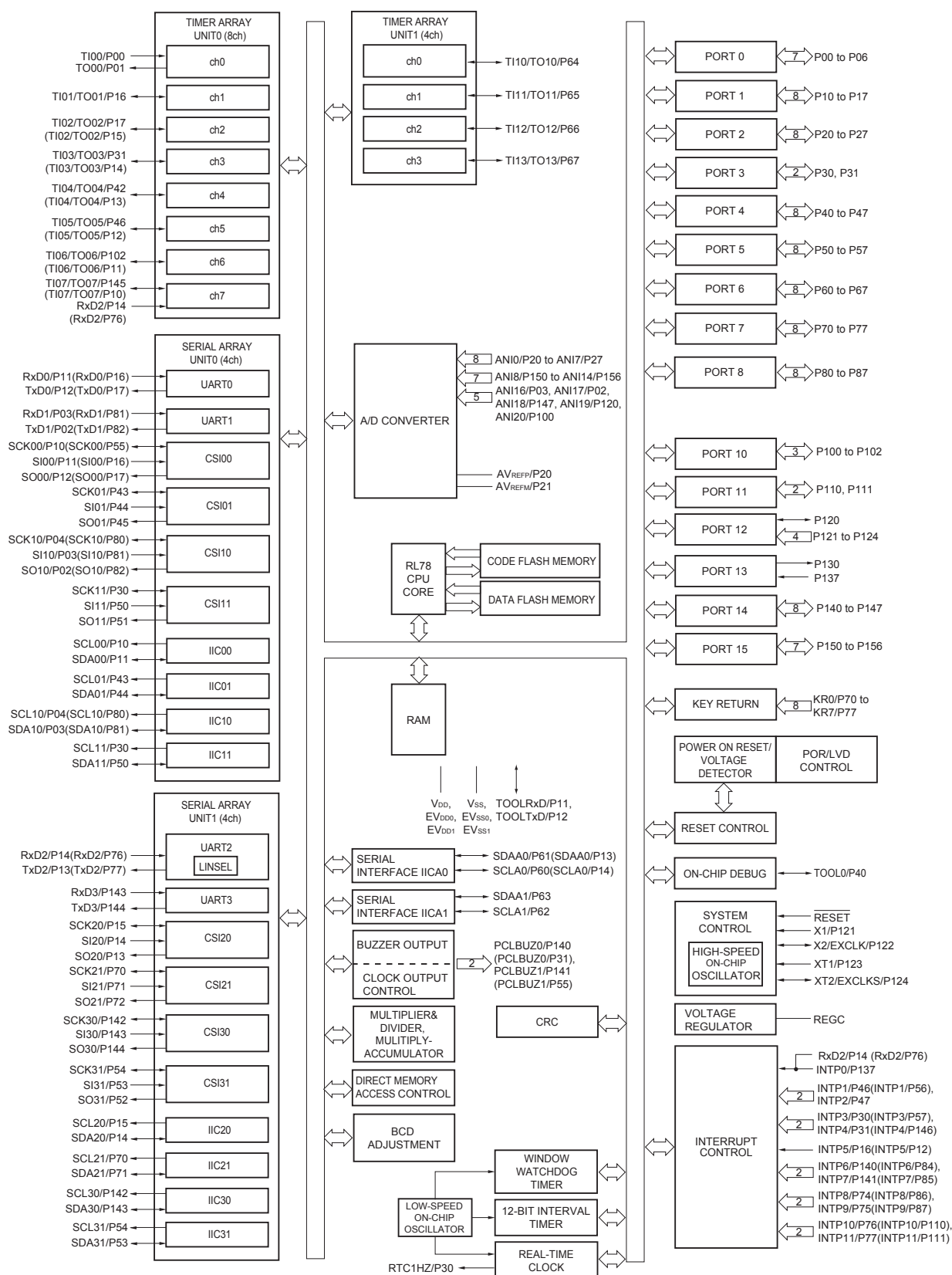
1.5.3 25-pin products

1.5.9 48-pin products

TIMER ARRAY UNIT (8ch)

- TI00/P00 — ch0 — TO00/P01
- TI01/TO01/P16 — ch1
- TI02/TO02/P17 (TI02/TO02/P15) — ch2
- TI03/TO03/P31 (TI03/TO03/P14) — ch3
- (TI04/TO04/P13) — ch4
- (TI05/TO05/P12) — ch5
- (TI06/TO06/P11) — ch6
- TI07/TO07/P41 (TI07/TO07/P10) — ch7
- RxD2/P14

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR → 12-BIT INTERVAL TIMER

RTC1HZ/P30 → REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

- RxD0/P11(RxD0/P16) — UART0
- TxD0/P12(TxD0/P17)
- RxD1/P01 — UART1
- TxD1/P00
- SCK00/P10 — CSI00
- SI00/P11
- SO00/P12
- SCK01/P75 — CSI01
- SI01/P74
- SO01/P73
- SCK11/P30 — CSI11
- SI11/P50
- SO11/P51
- SCL00/P10 — IIC00
- SDA00/P11
- SCL01/P75 — IIC01
- SDA01/P74
- SCL11/P30 — IIC11
- SDA11/P50

SERIAL ARRAY UNIT1 (2ch)

- RxD2/P14 — UART2 (LINSEL)
- TxD2/P13
- SCK20/P15 — CSI20
- SI20/P14
- SO20/P13
- SCK21/P70 — CSI21
- SI21/P71
- SO21/P72
- SCL20/P15 — IIC20
- SDA20/P14
- SCL21/P70 — IIC21
- SDA21/P71

RL78 CPU CORE — CODE FLASH MEMORY, DATA FLASH MEMORY

RAM

V_{DD}　V_{SS}　TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 → SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL → 2 → PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P15

MULTIPLIER & DIVIDER, MULTIPLY-ACCUMULATOR

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

CRC

PORT 0 — 2 — P00, P01
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 2 — P40, P41
PORT 5 — 2 — P50, P51
PORT 6 — 4 — P60 to P63
PORT 7 — 6 — P70 to P75
PORT 12 — P120, 4 — P121 to P124
PORT 13 — P130, P137
PORT 14 — 3 — P140, P146, P147

A/D CONVERTER
- 8 — ANI0/P20 to ANI7/P27
- 2 — ANI18/P147, ANI19/P120
- AV$_{REFP}$/P20
- AV$_{REFM}$/P21

KEY RETURN — 6 — KR0/P70 to KR5/P75

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL / HIGH-SPEED ON-CHIP OSCILLATOR
- RESET
- X1/P121
- X2/EXCLK/P122
- XT1/P123
- XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- RxD2/P14
- INTP0/P137
- 2 — INTP1/P50, INTP2/P51
- 2 — INTP3/P30, INTP4/P31
- INTP5/P16
- INTP6/P140
- 2 — INTP8/P74, INTP9/P75

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.13 100-pin products

TIMER ARRAY UNIT0 (8ch)
- TI00/P00, TO00/P01 — ch0
- TI01/TO01/P16 — ch1
- TI02/TO02/P17 (TI02/TO02/P15) — ch2
- TI03/TO03/P31 (TI03/TO03/P14) — ch3
- TI04/TO04/P42 (TI04/TO04/P13) — ch4
- TI05/TO05/P46 (TI05/TO05/P12) — ch5
- TI06/TO06/P102 (TI06/TO06/P11) — ch6
- TI07/TO07/P145 (TI07/TO07/P10) — ch7
- RxD2/P14 (RxD2/P76)

TIMER ARRAY UNIT1 (4ch)
- ch0 → TI10/TO10/P64
- ch1 → TI11/TO11/P65
- ch2 → TI12/TO12/P66
- ch3 → TI13/TO13/P67

SERIAL ARRAY UNIT0 (4ch)
- RxD0/P11(RxD0/P16), TxD0/P12(TxD0/P17) — UART0
- RxD1/P03(RxD1/P81), TxD1/P02(TxD1/P82) — UART1
- SCK00/P10(SCK00/P55), SI00/P11(SI00/P16), SO00/P12(SO00/P17) — CSI00
- SCK01/P43, SI01/P44, SO01/P45 — CSI01
- SCK10/P04(SCK10/P80), SI10/P03(SI10/P81), SO10/P02(SO10/P82) — CSI10
- SCK11/P30, SI11/P50, SO11/P51 — CSI11
- SCL00/P10, SDA00/P11 — IIC00
- SCL01/P43, SDA01/P44 — IIC01
- SCL10/P04(SCL10/P80), SDA10/P03(SDA10/P81) — IIC10
- SCL11/P30, SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (4ch)
- RxD2/P14(RxD2/P76), TxD2/P13(TxD2/P77) — UART2 (LINSEL)
- RxD3/P143, TxD3/P144 — UART3
- SCK20/P15, SI20/P14, SO20/P13 — CSI20
- SCK21/P70, SI21/P71, SO21/P72 — CSI21
- SCK30/P142, SI30/P143, SO30/P144 — CSI30
- SCK31/P54, SI31/P53, SO31/P52 — CSI31
- SCL20/P15, SDA20/P14 — IIC20
- SCL21/P70, SDA21/P71 — IIC21
- SCL30/P142, SDA30/P143 — IIC30
- SCL31/P54, SDA31/P53 — IIC31

A/D CONVERTER
- 8 ANI0/P20 to ANI7/P27
- 7 ANI8/P150 to ANI14/P156
- 5 ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120, ANI20/P100
- AV_{REFP}/P20
- AV_{REFM}/P21

RL78 CPU CORE
- CODE FLASH MEMORY
- DATA FLASH MEMORY

RAM

V_{DD}, EV_{DD0}, EV_{DD1}
V_{SS}, EV_{SS0}, EV_{SS1}
TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)
SERIAL INTERFACE IICA1 — SDAA1/P63, SCLA1/P62

BUZZER OUTPUT / CLOCK OUTPUT CONTROL — 2 PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P141 (PCLBUZ1/P55)

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

WINDOW WATCHDOG TIMER
12-BIT INTERVAL TIMER
LOW-SPEED ON-CHIP OSCILLATOR
REAL-TIME CLOCK — RTC1HZ/P30

PORT 0 — 7 P00 to P06
PORT 1 — 8 P10 to P17
PORT 2 — 8 P20 to P27
PORT 3 — 2 P30, P31
PORT 4 — 8 P40 to P47
PORT 5 — 8 P50 to P57
PORT 6 — 8 P60 to P67
PORT 7 — 8 P70 to P77
PORT 8 — 8 P80 to P87
PORT 10 — 3 P100 to P102
PORT 11 — 2 P110, P111
PORT 12 — P120, 4 P121 to P124
PORT 13 — P130, P137
PORT 14 — 8 P140 to P147
PORT 15 — 7 P150 to P156

KEY RETURN — 8 KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL / HIGH-SPEED ON-CHIP OSCILLATOR
- $\overline{RESET}$
- X1/P121
- X2/EXCLK/P122
- XT1/P123
- XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
- RxD2/P14 (RxD2/P76)
- INTP0/P137
- 2 INTP1/P46(INTP1/P56), INTP2/P47
- 2 INTP3/P30(INTP3/P57), INTP4/P31(INTP4/P146)
- INTP5/P16(INTP5/P12)
- 2 INTP6/P140(INTP6/P84), INTP7/P141(INTP7/P85)
- 2 INTP8/P74(INTP8/P86), INTP9/P75(INTP9/P87)
- 2 INTP10/P76(INTP10/P110), INTP11/P77(INTP11/P111)

Remark　Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[80-pin, 100-pin, 128-pin products]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Code flash memory (KB)		96 to 512		96 to 512		192 to 512	
Data flash memory (KB)		8	–	8	–	8	–
RAM (KB)		8 to 32 Note 1		8 to 32 Note 1		16 to 32 Note 1	
Address space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz					
Low-speed on-chip oscillator		15 kHz (TYP.)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)					
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)					
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.					
I/O port	Total	74		92		120	
	CMOS I/O	64 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 21)		82 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 24)		110 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 25)	
	CMOS input	5		5		5	
	CMOS output	1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	4		4		4	
Timer	16-bit timer	12 channels		12 channels		16 channels	
	Watchdog timer	1 channel		1 channel		1 channel	
	Real-time clock (RTC)	1 channel		1 channel		1 channel	
	12-bit interval timer (IT)	1 channel		1 channel		1 channel	
	Timer output	12 channels (PWM outputs: 10 Note 2)		12 channels (PWM outputs: 10 Note 2)		16 channels (PWM outputs: 14 Note 2)	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)					

Notes 1.   The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P):   Start address FAF00H

R5F100xL, R5F101xL (x = M, P, S):   Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944).**

(5) During communication at same potential (simplified I²C mode) (1/2)

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	—		1850		1850		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

UART mode bit width (during communication at different potential) (reference)
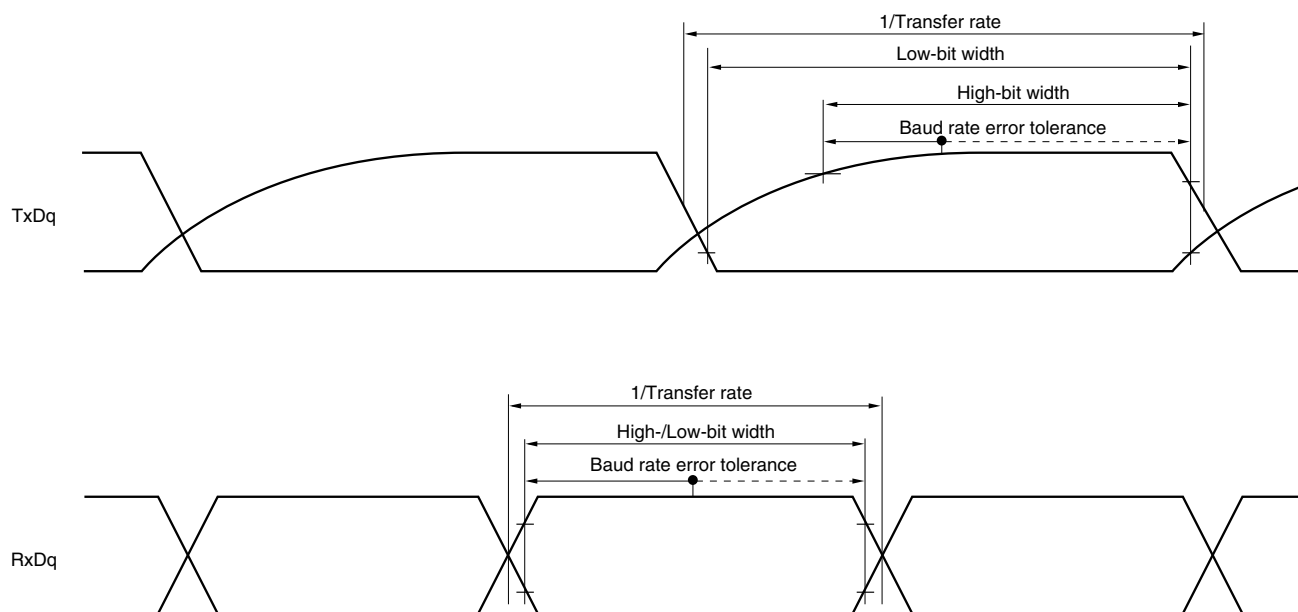
Remarks **1.** R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T$_A$ = –40 to +85°C, 2.7 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 2/f$_{CLK}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ	200		1150		1150		ns
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t$_{KH1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		t$_{KCY1}$/2 − 120		ns
SCKp low-level width	t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		t$_{KCY1}$/2 − 7		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		t$_{KCY1}$/2 − 10		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) [Note 1]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 20 pF, R$_b$ = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 20 pF, R$_b$ = 2.7 kΩ			130		130		130	ns

(**Notes, Caution,** and **Remarks** are listed on the next page.)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV$_{DD0}$		EV$_{DD0}$	V
	V$_{IH2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	2.2		EV$_{DD0}$	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	2.0		EV$_{DD0}$	V
			TTL input buffer 2.4 V ≤ EV$_{DD0}$ < 3.3 V	1.5		EV$_{DD0}$	V
	V$_{IH3}$	P20 to P27, P150 to P156		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P63		0.7EV$_{DD0}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV$_{DD0}$	V
	V$_{IL2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ EV$_{DD0}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P27, P150 to P156		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60 to P63		0		0.3EV$_{DD0}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V

Caution **The maximum value of V$_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV$_{DD0}$, even in the N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3) Peripheral Functions (Common to all products)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$ Note 1				0.20		μA
RTC operating current	I$_{RTC}$ Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I$_{IT}$ Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I$_{WDT}$ Notes 1, 2, 5	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ Notes 1, 6	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$ Note 1				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ Note 1				75.0		μA
LVD operating current	I$_{LVD}$ Notes 1, 7				0.08		μA
Self programming operating current	I$_{FSP}$ Notes 1, 9				2.50	12.20	mA
BGO operating current	I$_{BGO}$ Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Loe voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V$_{DD}$.

    2. When high speed on-chip oscillator and high-speed system clock are stopped.

    3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added. I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

    4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

    5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer operates.
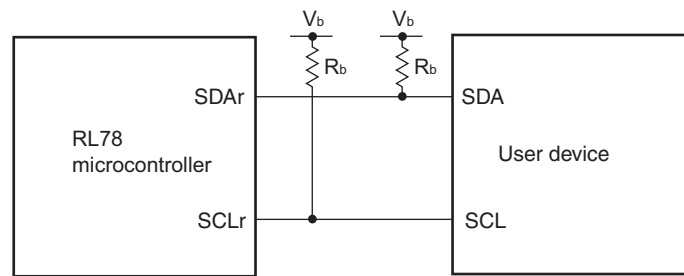
CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
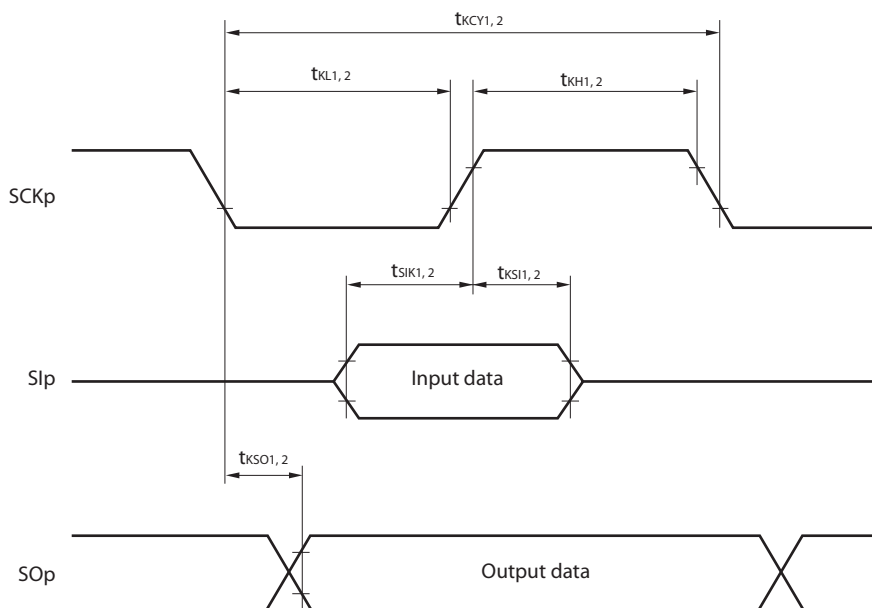
$t_{KCY1, 2}$

$t_{KL1, 2}$ $t_{KH1, 2}$

SCKp

$t_{SIK1, 2}$ $t_{KSI1, 2}$

SIp   Input data

$t_{KSO1, 2}$

SOp   Output data

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

$t_{KCY1, 2}$

$t_{KH1, 2}$ $t_{KL1, 2}$

SCKp

$t_{SIK1, 2}$ $t_{KSI1, 2}$

SIp   Input data

$t_{KSO1, 2}$

SOp   Output data
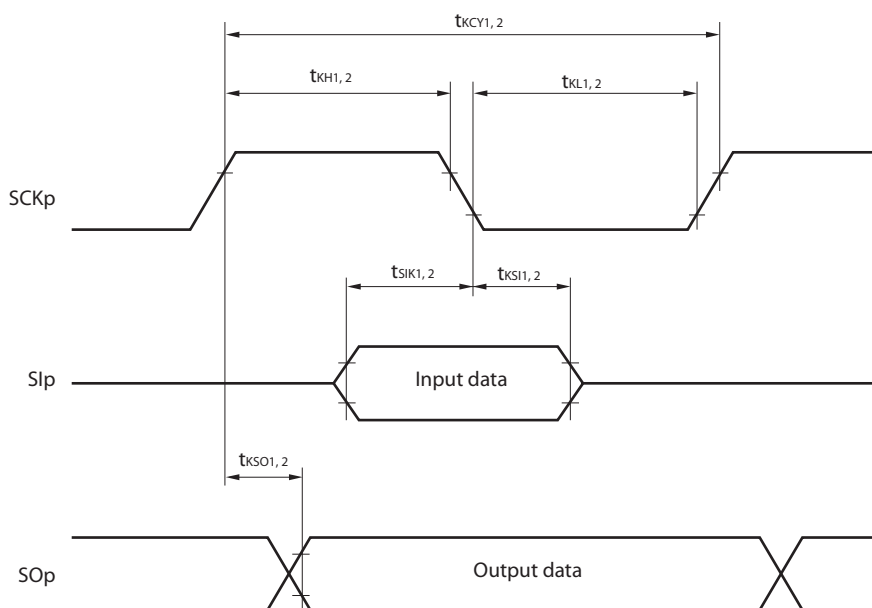
Remarks 1.   p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
2.   m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

Simplified I^{2}C mode connection diagram (during communication at different potential)

Simplified I^{2}C mode serial transfer timing (during communication at different potential)
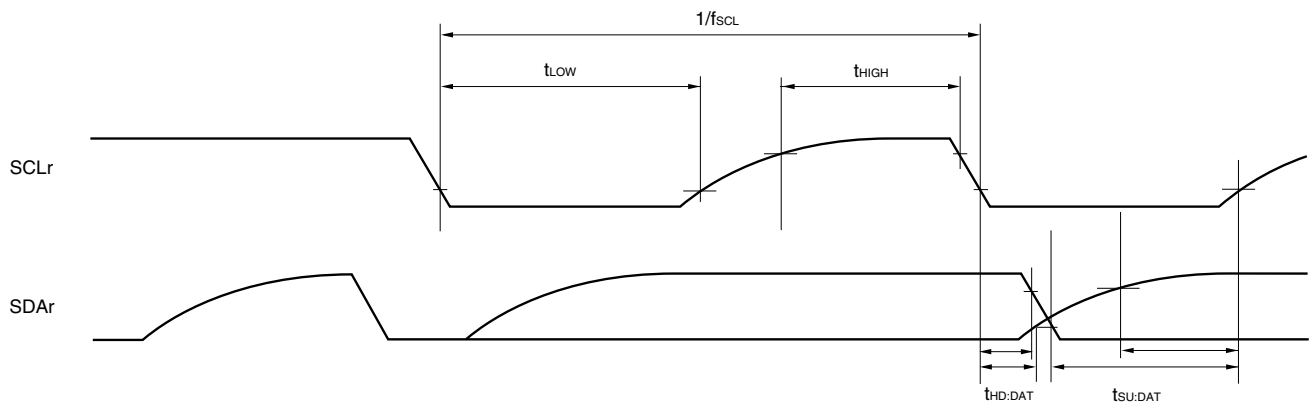
Caution   **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

Remarks **1.** R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

   2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

   3. f$_{MCK}$: Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

   n: Channel number (mn = 00, 01, 02, 10, 12, 13)

3.6.3 POR circuit characteristics

(T$_A$ = –40 to +105°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.45	1.51	1.57	V
	V$_{PDR}$	Power supply fall time	1.44	1.50	1.56	V
Minimum pulse width	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time
required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is
entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock
operation status control register (CSC).
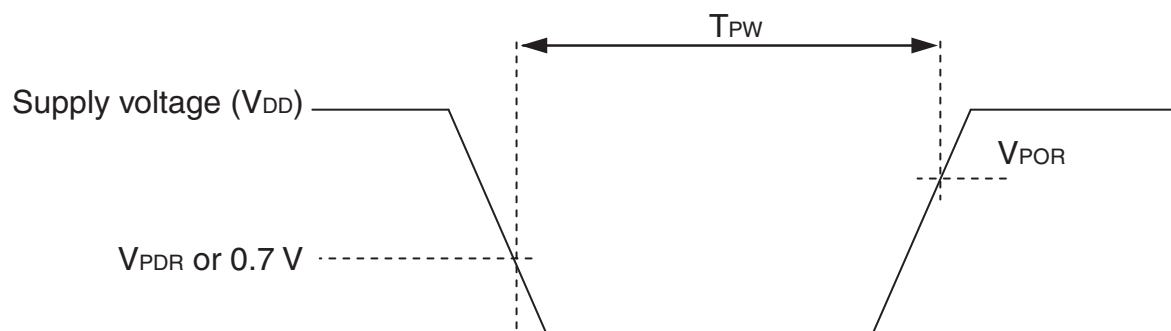
4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP
R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP
R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP
R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12

detail of lead end

NOTE

Each lead centerline is located within 0.13 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	$0.24^{+0.08}_{-0.07}$
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	$3°^{+5°}_{-3°}$
T	0.25
U	0.6±0.15
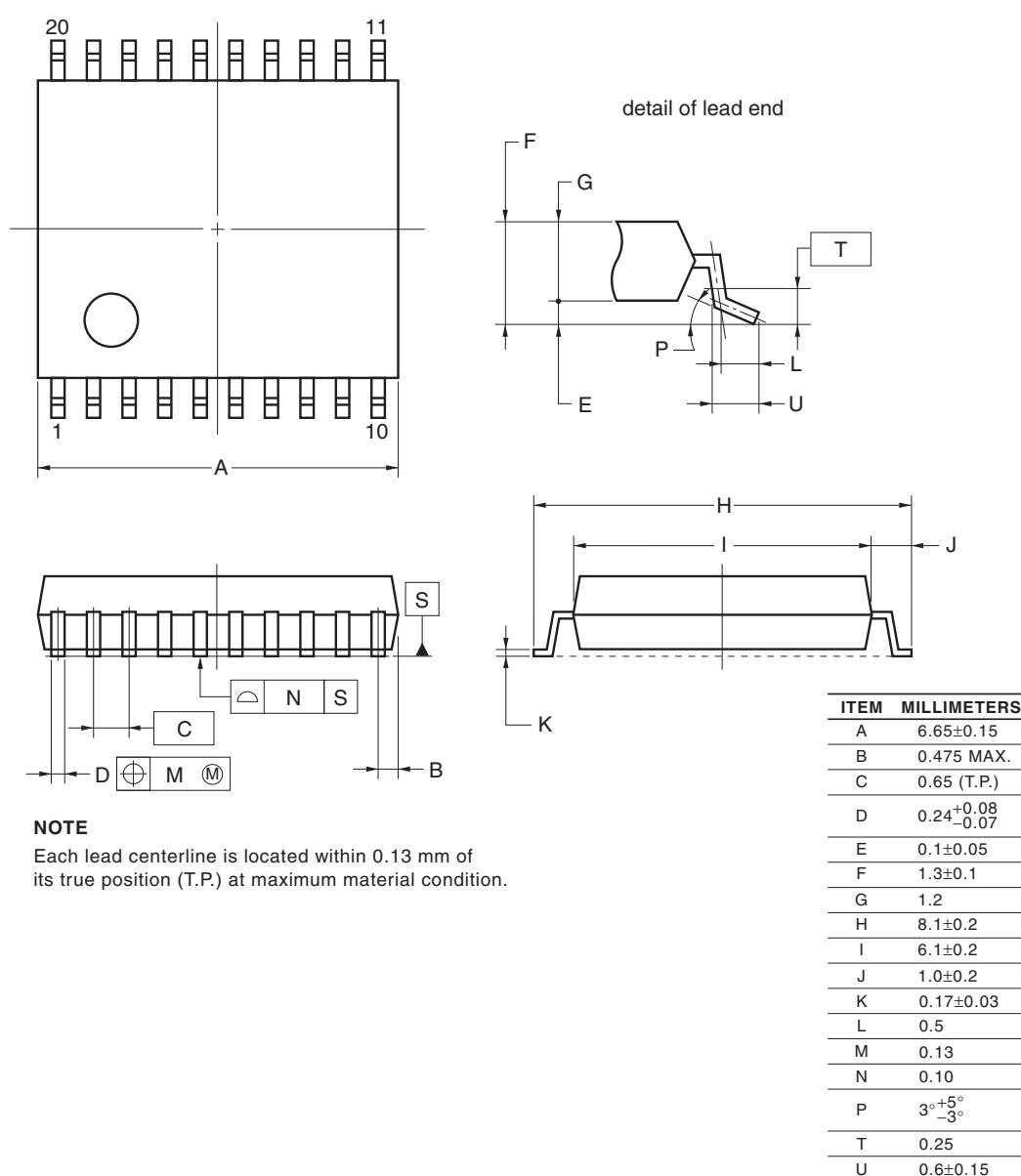
4.2 24-pin Products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
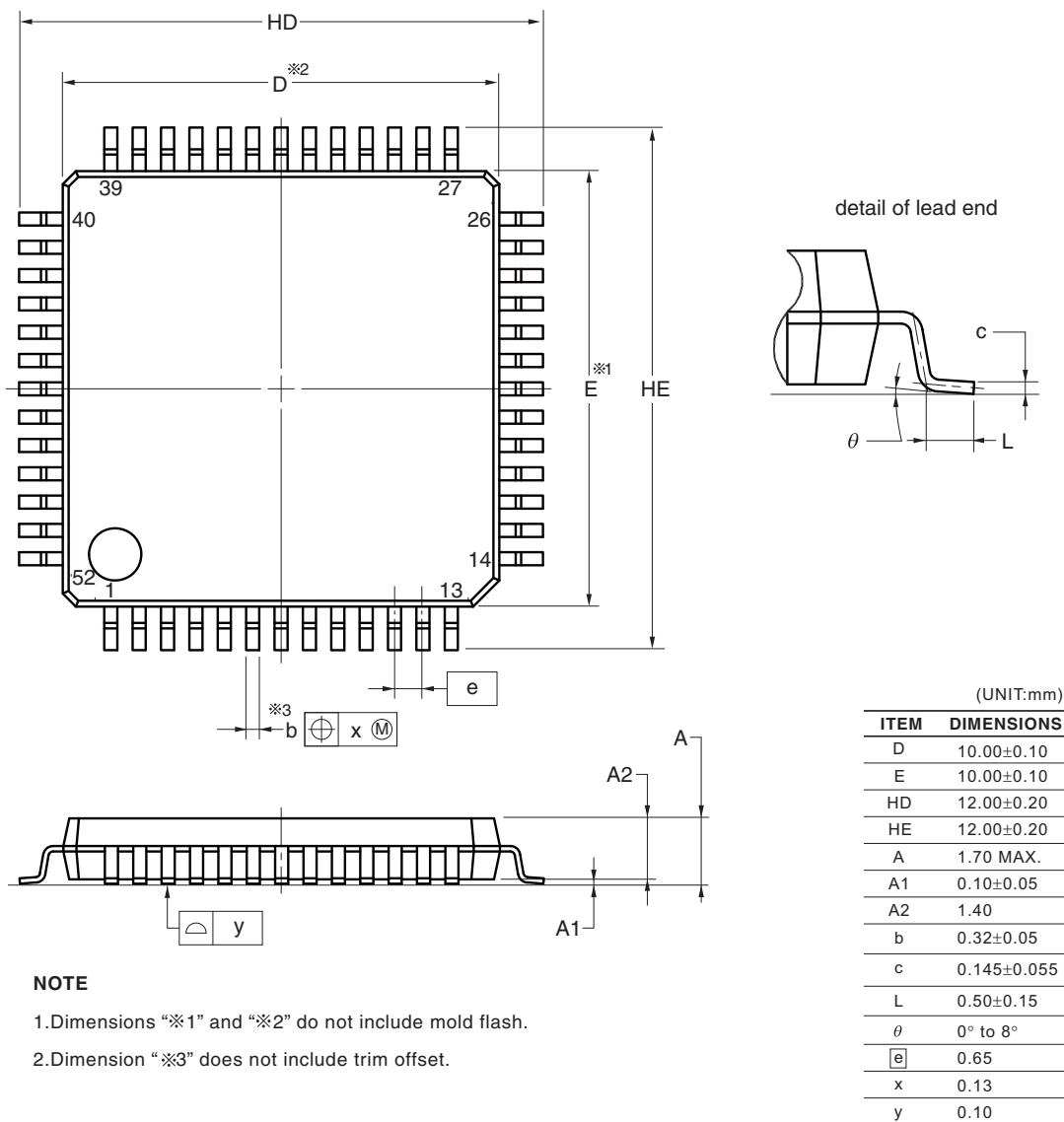R5F1007AGNA, R5F1007CGNA, R5F1007DGNA, R5F1007EGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-3	0.04

DETAIL OF Ⓐ PART

INDEX AREA

EXPOSED DIE PAD

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.95	4.00	4.05
E	3.95	4.00	4.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
ⓔ	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	2.50	—
E_2	—	2.50	—
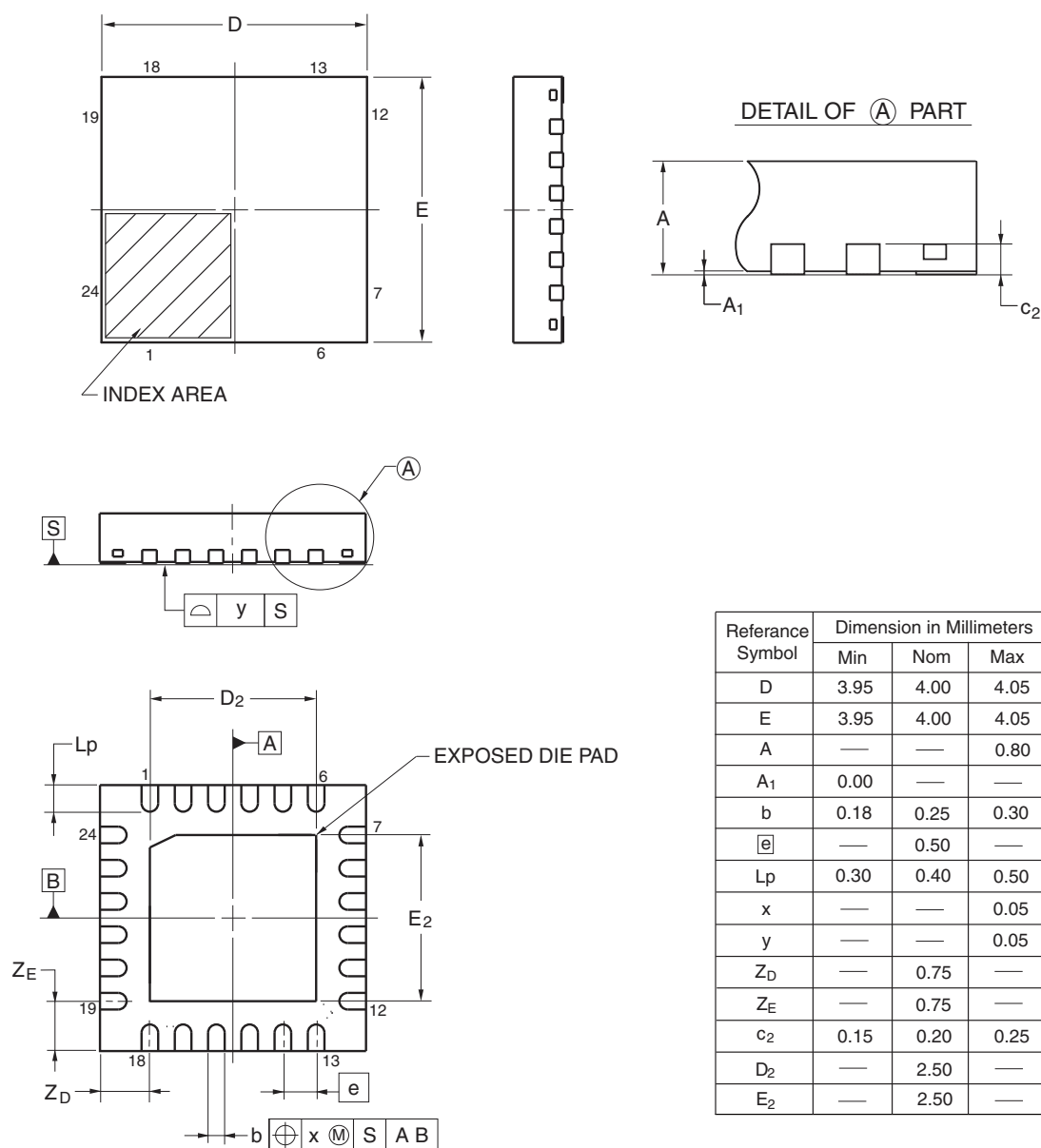
4.10 52-pin Products

R5F100JCAFA, R5F100JDAFA, R5F100JEAFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJAFA, R5F100JKAFA, R5F100JLAFA

R5F101JCAFA, R5F101JDAFA, R5F101JEAFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJAFA, R5F101JKAFA, R5F101JLAFA

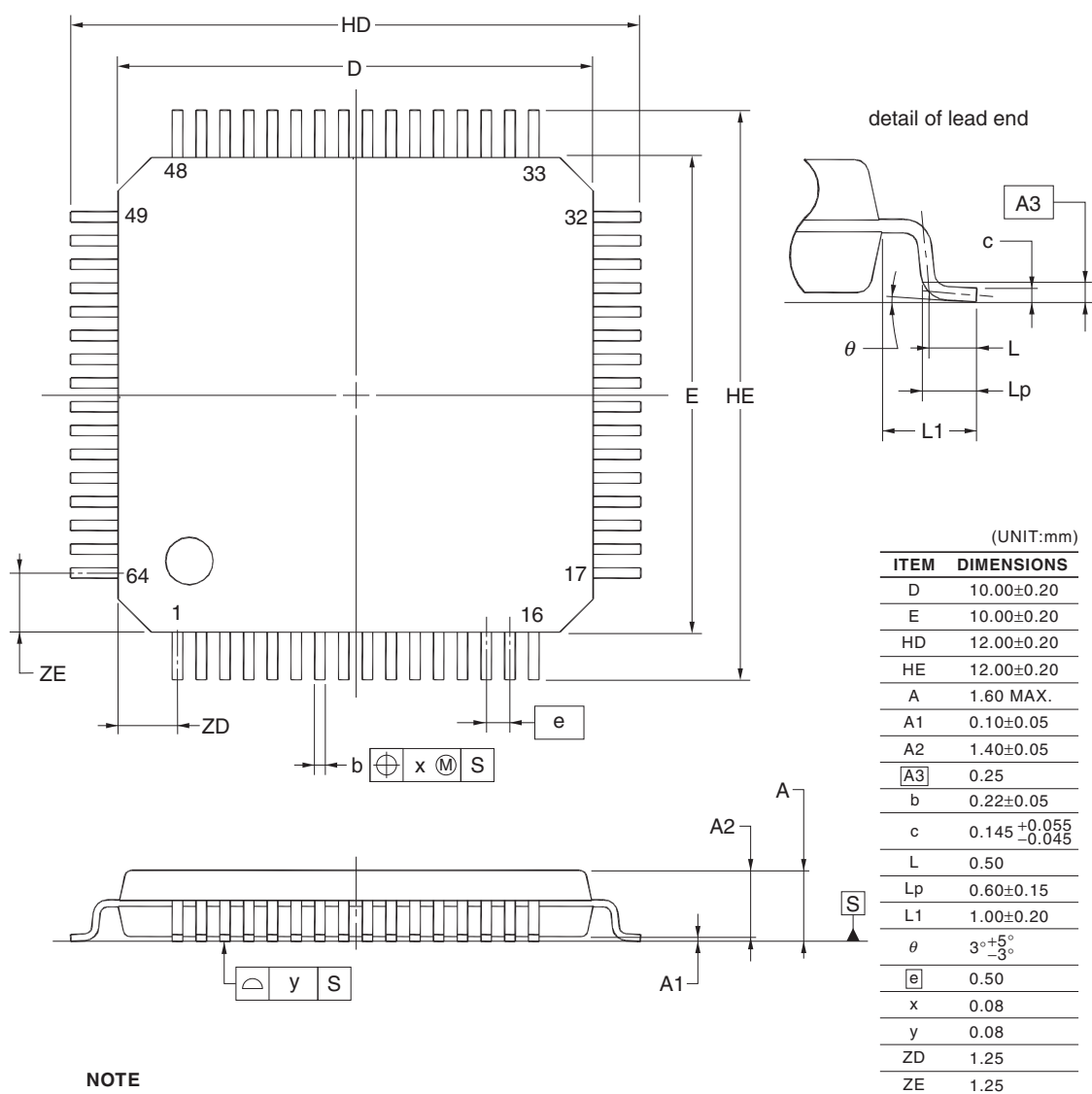R5F100JCDFA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDFA, R5F100JJDFA, R5F100JKDFA, R5F100JLDFA

R5F101JCDFA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDFA, R5F101JJDFA, R5F101JKDFA, R5F101JLDFA

R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,
R5F100LKAFB, R5F100LLAFB

R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB,
R5F101LJAFB, R5F101LKAFB, R5F101LLAFB

R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,
R5F100LKDFB, R5F100LLDFB

R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB,
R5F101LJDFB, R5F101LKDFB, R5F101LLDFB

R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB,
R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 \, ^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° \, ^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB
R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB
R5F100MFDFB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
R5F101MFDFB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB
R5F100MFGFB, R5F100MGGFB, R5F100MHGFB, R5F100MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.

		Description		
Rev.	**Date**	**Page**	**Summary**	
1.00	Feb 29, 2012	-	First Edition issued	
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.	
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.	
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.	
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.	
		59, 63, 67	Descriptions of Note 8 in a table corrected.	
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.	
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.	
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.	
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.	
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.	
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.	
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.	
3.00	Aug 02, 2013	1	Modification of 1.1 Features	
		3	Modification of 1.2 List of Part Numbers	
		4 to 15	Modification of Table 1-1. List of Ordering Part Numbers, note, and caution	
		16 to 32	Modification of package type in 1.3.1 to 1.3.14	
		33	Modification of description in 1.4 Pin Identification	
		48, 50, 52	Modification of caution, table, and note in 1.6 Outline of Functions	
		55	Modification of description in table of Absolute Maximum Ratings (T$_A$ = 25°C)	
		57	Modification of table, note, caution, and remark in 2.2.1 X1, XT1 oscillator characteristics	
		57	Modification of table in 2.2.2 On-chip oscillator characteristics	
		58	Modification of note 3 of table (1/5) in 2.3.1 Pin characteristics	
		59	Modification of note 3 of table (2/5) in 2.3.1 Pin characteristics	
		63	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		64	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		65	Modification of table in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		66	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products	
		68	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products	
		70	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products	
		72	Modification of notes 1 and 4 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products	
		74	Modification of notes 1, 5, and 6 in (3) Flash ROM: 384 to 512 KB of 44- to 100-pin products	
		75	Modification of (4) Peripheral Functions (Common to all products)	
		77	Modification of table in 2.4 AC Characteristics	
		78, 79	Addition of Minimum Instruction Execution Time during Main System Clock Operation	
		80	Modification of figures of AC Timing Test Points and External System Clock Timing	

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction.   If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction.   Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction.   CMOS devices behave differently than Bipolar or NMOS devices.   Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry.   Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin.   All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation.   Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate.   When it is dry, a humidifier should be used.   It is recommended to avoid using insulators that easily build up static electricity.   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material.   All test and measurement tools including work benches and floors should be grounded.   The operator should be grounded using a wrist strap.   Semiconductor devices must not be touched with bare hands.   Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device.   Immediately after the power source is turned ON, devices with reset functions have not yet been initialized.   Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers.   A device is not initialized until the reset signal is received.   A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply.   When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply.   Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.   The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE :   Do not input signals or an I/O pull-up power supply while the device is not powered.   The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.   Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.