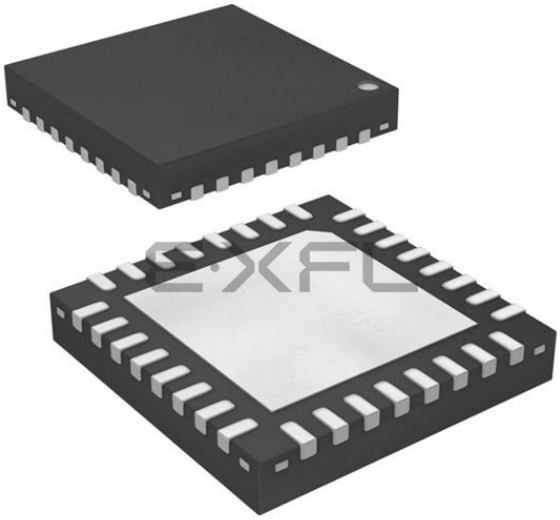
Renesas Electronics America Inc - R5F101BCDNA#U0 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-WFQFN Exposed Pad
Supplier Device Package	32-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101bcdna-u0

Table 1-1. List of Ordering Part Numbers

(12/12)

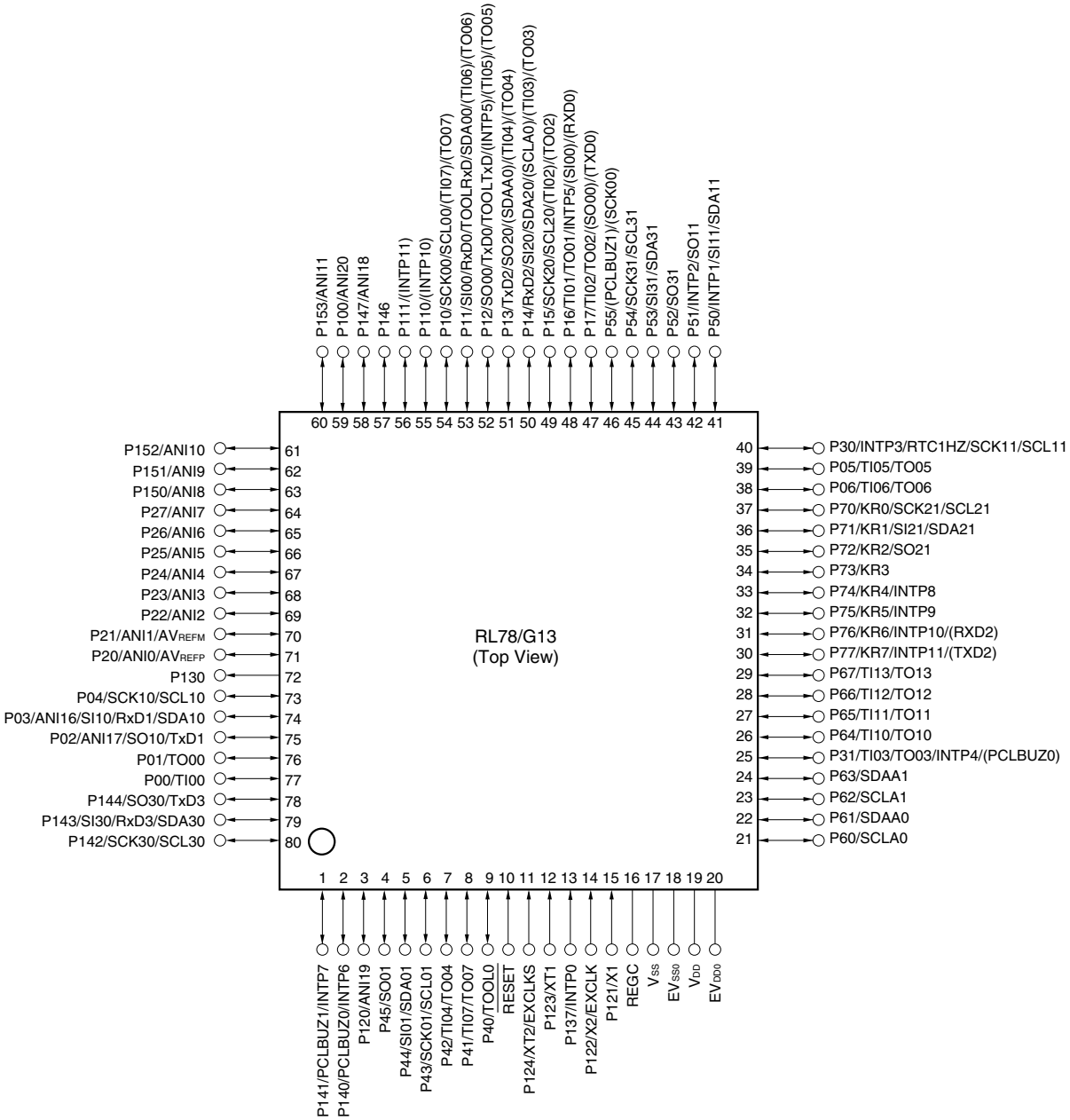
Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
128 pins	128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)	Mounted	A	R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0
			D	R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0
		Not mounted	A	R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0
			D	R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

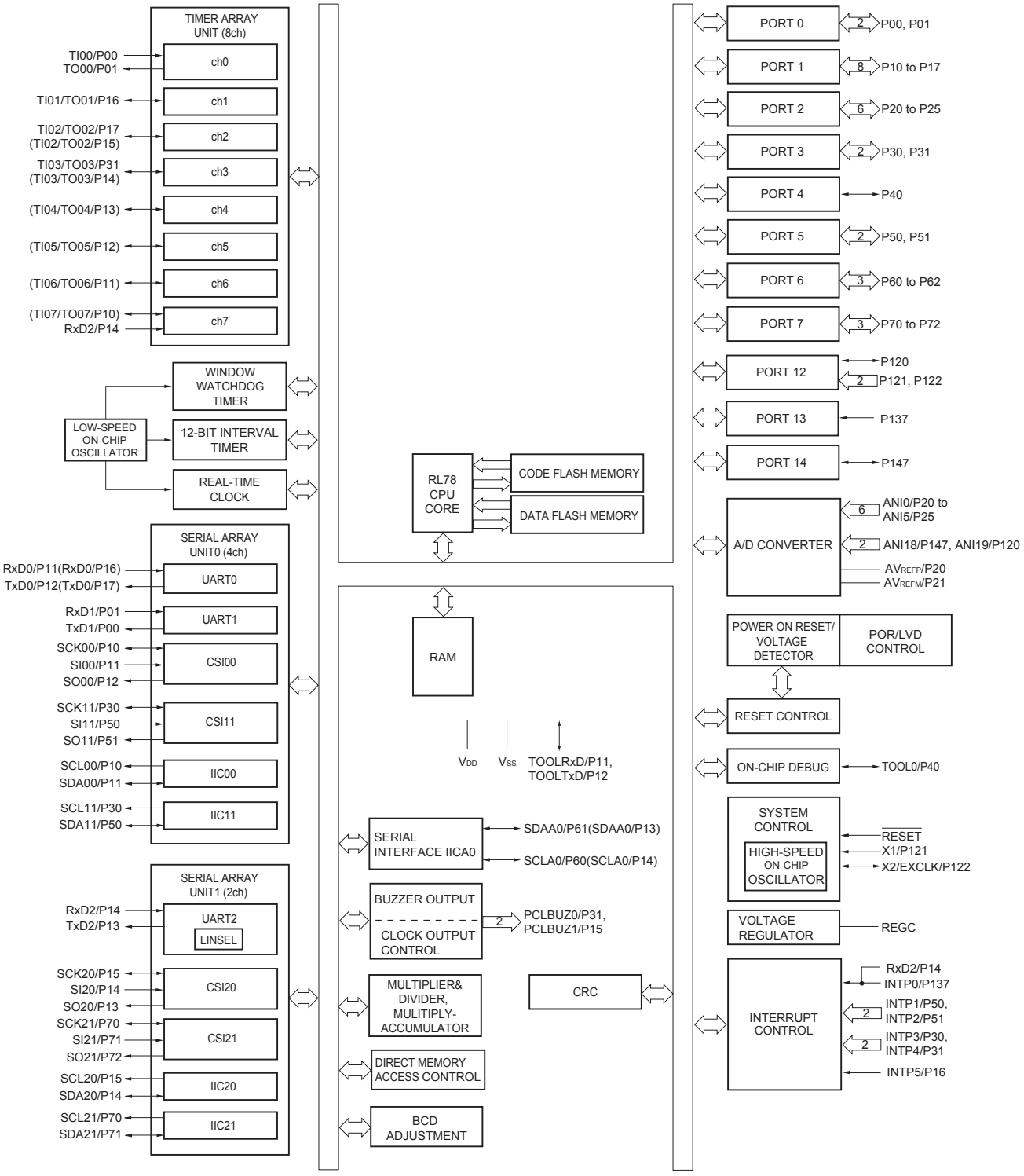
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

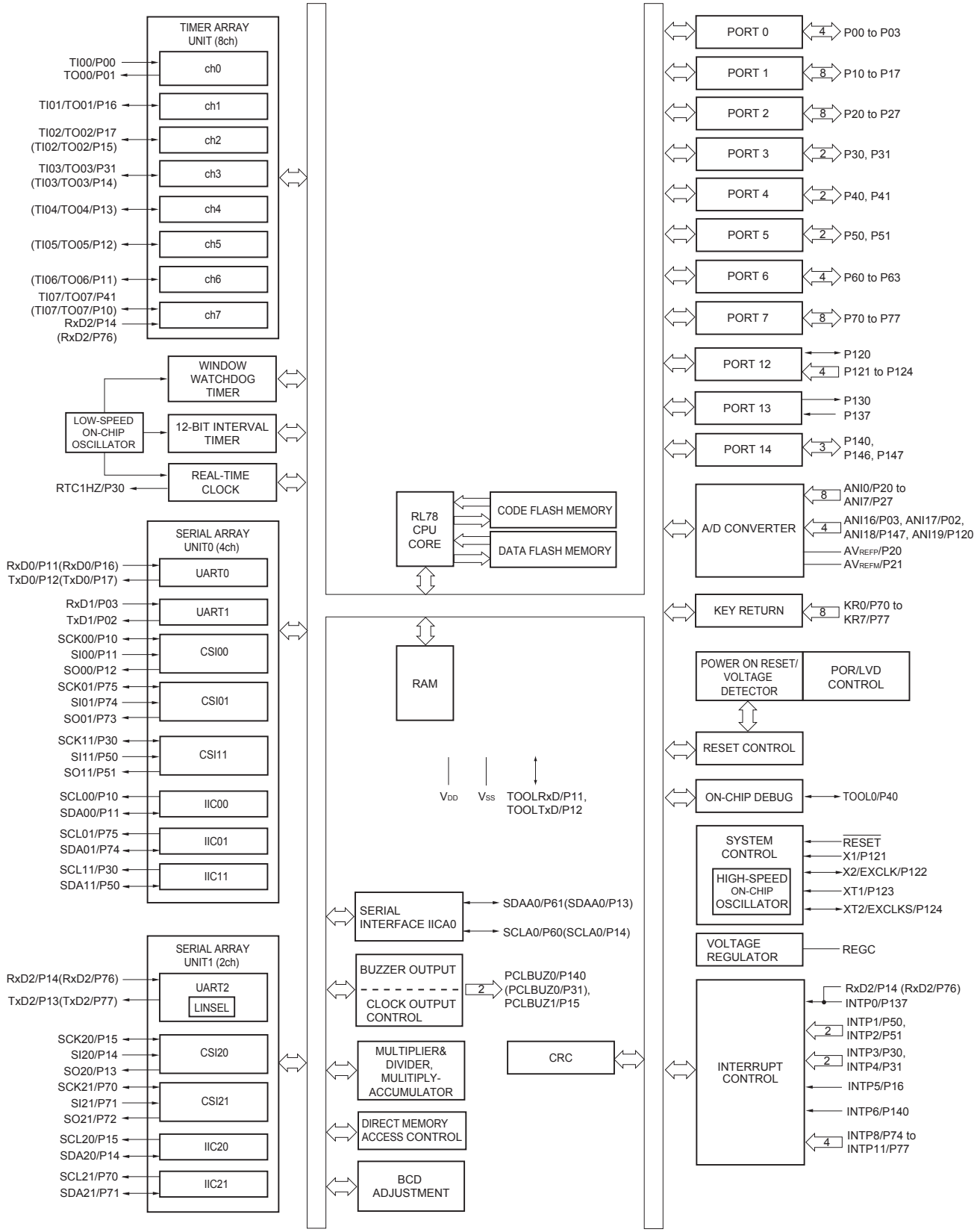
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.6 36-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.10 52-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output		–		1		1		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)											
8/10-bit resolution A/D converter		6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface		[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
	I^2C bus	–		1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller		2 channels											
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt		–											
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function		Provided											
<R> Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)											
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)											

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512	
Data flash memory (KB)		4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 16[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]		2 to 32[Note1]	
Address space		1 MB									
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)									
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz									
Low-speed on-chip oscillator		15 kHz (TYP.)									
General-purpose registers		(8-bit register × 8) × 4 banks									
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)									
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)									
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.									
I/O port	Total	36		40		44		48		58	
	CMOS I/O	28 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		31 (N-ch O.D. I/O [V_{DD} withstand voltage]: 10)		34 (N-ch O.D. I/O [V_{DD} withstand voltage]: 11)		38 (N-ch O.D. I/O [V_{DD} withstand voltage]: 13)		48 (N-ch O.D. I/O [V_{DD} withstand voltage]: 15)	
	CMOS input	5		5		5		5		5	
	CMOS output	–		–		1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	3		4		4		4		4	
Timer	16-bit timer	8 channels									
	Watchdog timer	1 channel									
	Real-time clock (RTC)	1 channel									
	12-bit interval timer (IT)	1 channel									
	Timer output	4 channels (PWM outputs: 3[Note2], 8 channels (PWM outputs: 7[Note2])[Note3]		5 channels (PWM outputs: 4[Note2], 8 channels (PWM outputs: 7[Note2])[Note3]						8 channels (PWM outputs: 7[Note2])	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)									

Notes 1. The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xD, R5F101xD (x = E to G, J, L): Start address FF300H
R5F100xE, R5F101xE (x = E to G, J, L): Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L): Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

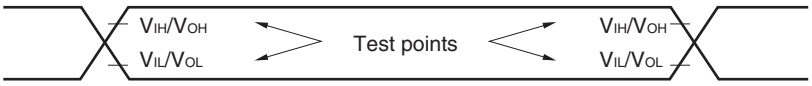
(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

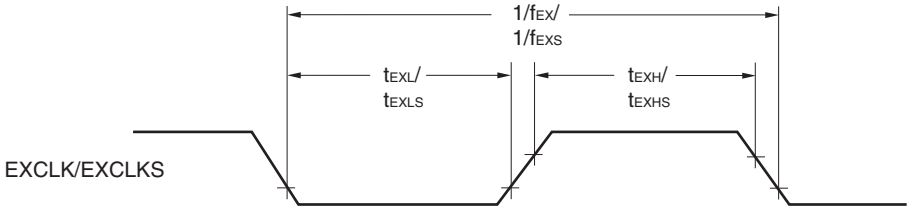
Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.6		mA
						V_{DD} = 3.0 V		2.6		mA
					Normal operation	V_{DD} = 5.0 V		6.1	9.5	mA
						V_{DD} = 3.0 V		6.1	9.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		4.8	7.4	mA
						V_{DD} = 3.0 V		4.8	7.4	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.5	5.3	mA
						V_{DD} = 3.0 V		3.5	5.3	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.3	mA
						V_{DD} = 2.0 V		1.5	2.3	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.5	2.0	mA
						V_{DD} = 2.0 V		1.5	2.0	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.9	6.1	mA
						Resonator connection		4.1	6.3	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.9	6.1	mA
						Resonator connection		4.1	6.3	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		2.5	3.7	mA
						Resonator connection		2.5	3.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		2.5	3.7	mA
						Resonator connection		2.5	3.7	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.2	mA
						Resonator connection		1.4	2.2	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.2	mA
						Resonator connection		1.4	2.2	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		5.4	6.5	μA
						Resonator connection		5.5	6.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		5.5	6.5	μA
						Resonator connection		5.6	6.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		5.6	9.4	μA
						Resonator connection		5.7	9.5	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		5.9	12.0	μA
						Resonator connection		6.0	12.1	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		6.6	16.3	μA
						Resonator connection		6.7	16.4	μA

(**Notes** and **Remarks** are listed on the next page.)

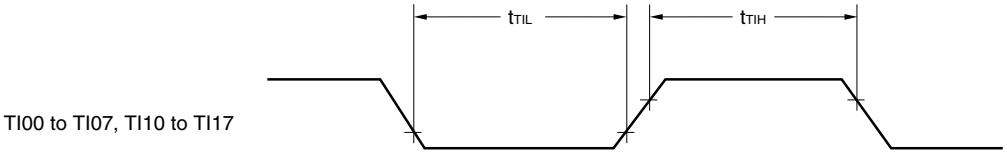
AC Timing Test Points

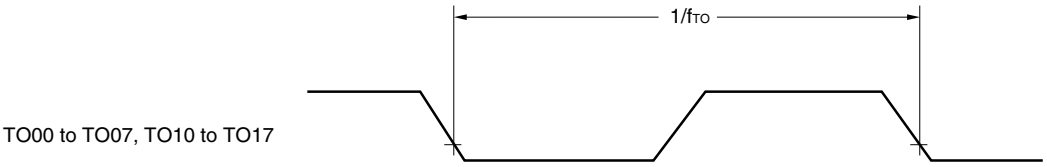


External System Clock Timing

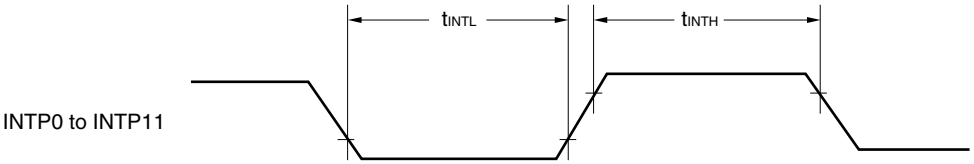


TI/TO Timing

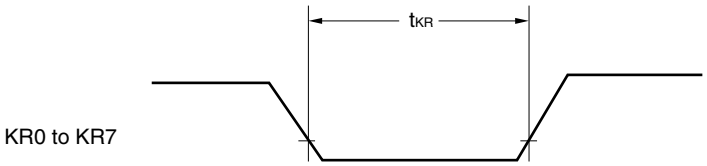




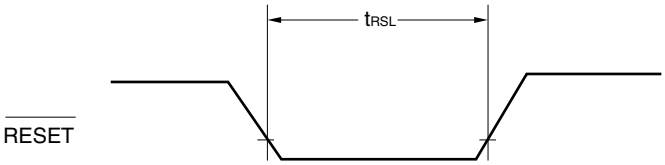
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

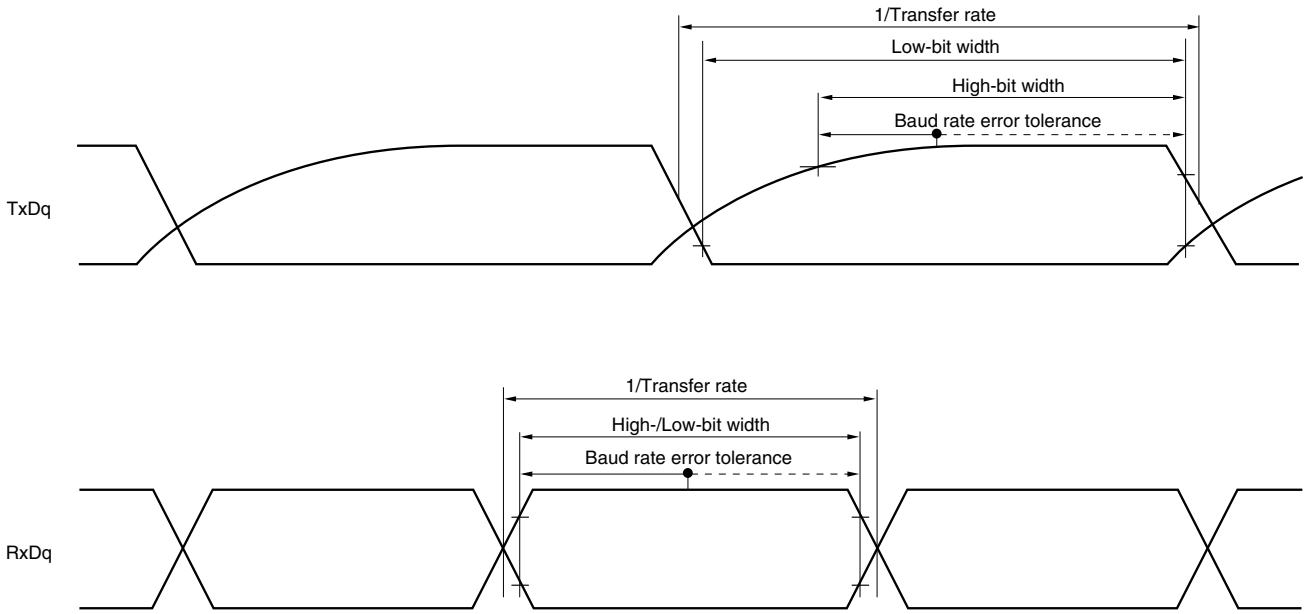
(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V	20 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 20 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V	16 MHz < f_{MCK}	8/f_{MCK}		—		—		ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}		6/f_{MCK}		6/f_{MCK}		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 500		6/f_{MCK} and 500		6/f_{MCK} and 500		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 750		6/f_{MCK} and 750		6/f_{MCK} and 750		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		6/f_{MCK} and 1500		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		6/f_{MCK} and 1500		6/f_{MCK} and 1500		ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		t_{KCY2}/2 – 7		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		t_{KCY2}/2 – 8		ns
		1.8 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		t_{KCY2}/2 – 18		ns
		1.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns
		1.6 V ≤ EV_{DD0} ≤ 5.5 V		—		t_{KCY2}/2 – 66		t_{KCY2}/2 – 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

UART mode bit width (during communication at different potential) (reference)



Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (1/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	t_{KCY1} ≥ 4/f_{CLK}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		t_{KCY1}/2 – 75		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		t_{KCY1}/2 – 170		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		t_{KCY1}/2 – 458		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		t_{KCY1}/2 – 12		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		t_{KCY1}/2 – 18		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note], C_b = 30 pF, R_b = 5.5 kΩ		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		t_{KCY1}/2 – 50		ns

Note Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed two pages after the next page.)

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

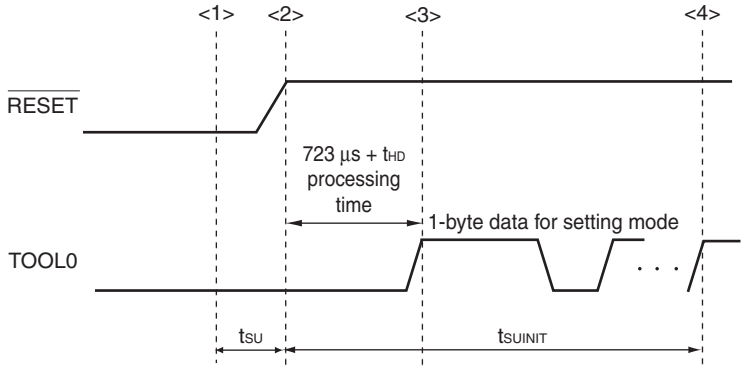
4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.10 Timing of Entry to Flash Memory Programming Modes

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time to complete the communication for the initial setting after the external reset is released	t_{SUINIT}	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	t_{SU}	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must be released before the external reset is released.	1			ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset is released (POR and LVD reset must be released before the external reset is released.).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark t_{SUINIT}: Communication for the initial setting must be completed within 100 ms after the external reset is released during this period.

t_{SU}: Time to release the external reset after the TOOL0 pin is set to the low level

t_{HD}: Time to hold the TOOL0 pin at the low level after the external reset is released (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T_A = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T_A = –40 to +105°C
R5F100xxGxx

Cautions 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2. With products not provided with an EV_{DD0}, EV_{DD1}, EV_{SS0}, or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD}, or replace EV_{SS0} and EV_{SS1} with V_{SS}.

3. The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.

4. Please contact Renesas Electronics sales office for derating of operation under T_A = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G13 is used in the range of T_A = –40 to +85°C, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS (T_A = –40 to +85°C)**.

There are following differences between the products "G: Industrial applications (T_A = –40 to +105°C)" and the products “A: Consumer applications, and D: Industrial applications”.

Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	T_A = -40 to +85°C	T_A = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V_{DD} ≤ 5.5 V ±1.0%@ T_A = -20 to +85°C ±1.5%@ T_A = -40 to -20°C 1.6 V ≤ V_{DD} < 1.8 V ±5.0%@ T_A = -20 to +85°C ±5.5%@ T_A = -40 to -20°C	2.4 V ≤ V_{DD} ≤ 5.5 V ±2.0%@ T_A = +85 to +105°C ±1.0%@ T_A = -20 to +85°C ±1.5%@ T_A = -40 to -20°C
Serial array unit	UART CSI: f_{CLK}/2 (supporting 16 Mbps), f_{CLK}/4 Simplified I^2C communication	UART CSI: f_{CLK}/4 Simplified I^2C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(**Remark** is listed on the next page.)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −3.0 mA	EV_{DD0} − 0.7			V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −2.0 mA	EV_{DD0} − 0.6			V
			2.4 V ≤ EV_{DD0} ≤ 5.5 V, I_{OH1} = −1.5 mA	EV_{DD0} − 0.5			V
	V_{OH2}	P20 to P27, P150 to P156	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = −100 μA	V_{DD} − 0.5			V
Output voltage, low	V_{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL1} = 0.6 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P156	2.4 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 15.0 mA			2.0	V
			4.0 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 5.0 mA			0.4	V
			2.7 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 3.0 mA			0.4	V
			2.4 V ≤ EV_{DD0} ≤ 5.5 V, I_{OL3} = 2.0 mA			0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz

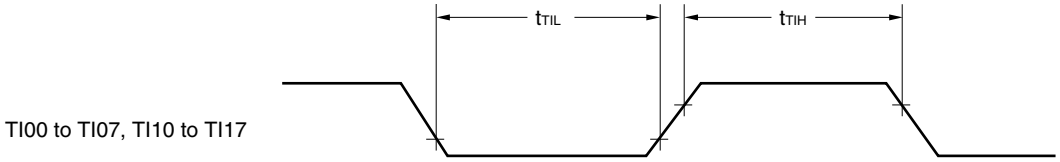
Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

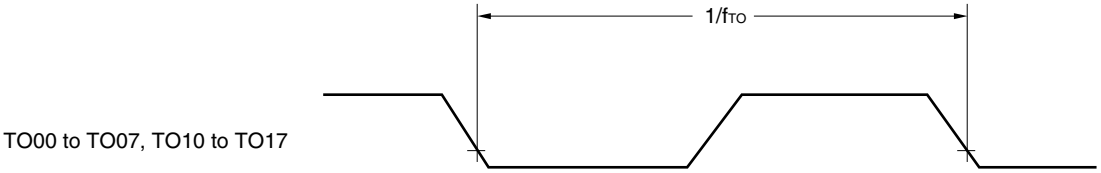
2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

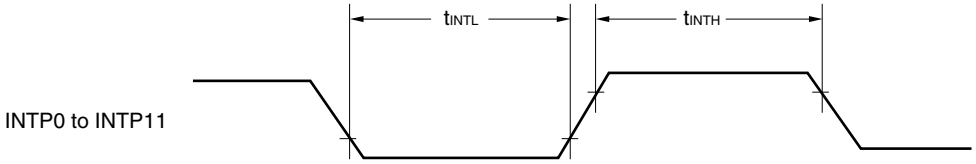
4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

TI/TO Timing

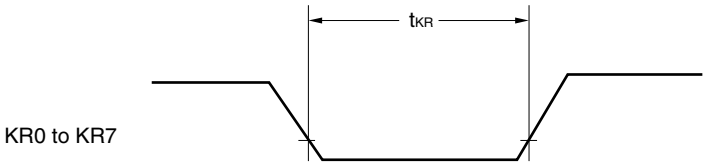




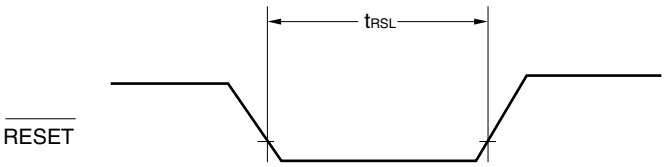
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V	250		ns
			2.4 V ≤ EV_{DD0} ≤ 5.5 V	500		ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 24		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 36		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		t_{KCY1}/2 – 76		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.7 V ≤ EV_{DD0} ≤ 5.5 V		66		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V		113		ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			38		ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4			50	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		400 Note1	kHz
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		100 Note1	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1200		ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	4600		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 220 Note2		ns
		2.4 V ≤ EV_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 580 Note2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV_{DD0} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

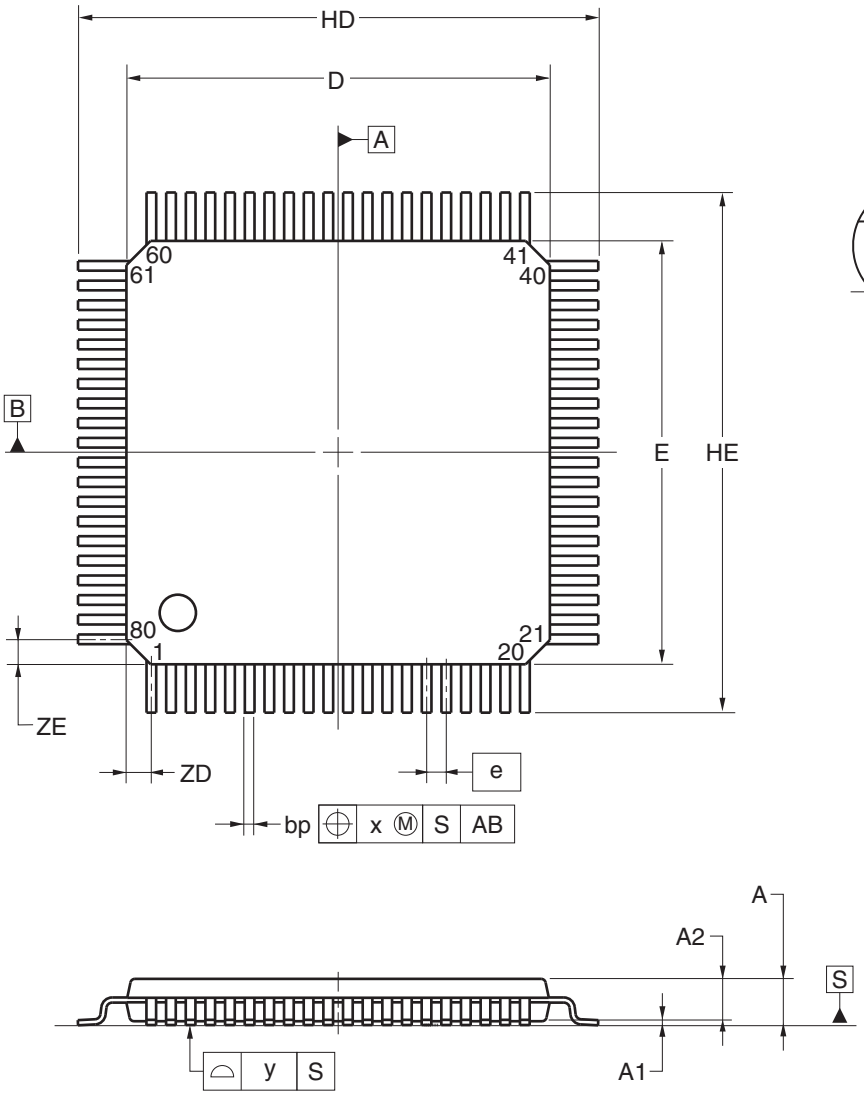
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

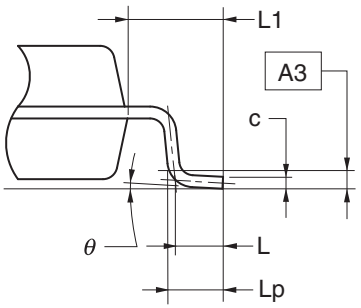
4.12 80-pin Products

R5F100MFAFA, R5F100MGAFA, R5F100MHAFA, R5F100MJAFA, R5F100MKAFA, R5F100MLAFA
R5F101MFAFA, R5F101MGAFA, R5F101MHAFA, R5F101MJAFA, R5F101MKAFA, R5F101MLAFA
R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA
R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



detail of lead end



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
θ	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—