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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

XFI

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101eddna-u0

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1-1.	List of	Ordering	Part	Numbers
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				(5/12)
Pin	Package	Data	Fields of	Ordering Part Number
count		flash	Application	
			Note	
48 pins	48-pin plastic	Mounted	А	R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0,
	LFQFP (7 \times 7 mm,			R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0,
	0.5 mm pitch)			R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0,
				R5F100GLAFB#V0
				R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0,
				R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0,
				R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0,
				R5F100GLAFB#X0
			D	R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0,
				R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0,
				R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0,
				R5F100GLDFB#V0
				R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0,
				R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0,
				R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0,
				R5F100GLDFB#X0
			G	R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0,
				R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0,
				R5F100GHGFB#V0, R5F100GJGFB#V0
				R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0,
				R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0,
				R5F100GHGFB#X0, R5F100GJGFB#X0
		Not	А	R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0,
		mounted		R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0,
				R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0,
				R5F101GLAFB#V0
				R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0,
				R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0,
				R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0,
				R5F101GLAFB#X0
			D	R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0,
				R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0,
				R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0,
				R5F101GLDFB#V0
				R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0,
				R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0,
				R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0,
		1		R5F101GLDFB#X0

Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.



1.3 Pin Configuration (Top View)

1.3.1 20-pin products

• 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remark For pin identification, see 1.4 Pin Identification.



1.3.10 52-pin products

• 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)





Remarks 1. For pin identification, see 1.4 Pin Identification.

Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.



1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Cautions 1. Make EVsso pin the same potential as Vss pin.

- 2. Make VDD pin the potential that is higher than EVDD0 pin.
- 3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).
- Remarks 1. For pin identification, see 1.4 Pin Identification.
 - 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 - **3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.



1.3.12 80-pin products

- 80-pin plastic LQFP (14 \times 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Cautions 1. Make EVsso pin the same potential as Vss pin.

- 2. Make VDD pin the potential that is higher than EVDD0 pin.
- 3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).
- Remarks 1. For pin identification, see 1.4 Pin Identification.
 - 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 - **3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G13 User's Manual.



Parameter	Symbols		Conditions	Ratings	Unit
Output current, high	Іон1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins –170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	Іон2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Output current, low	IoL1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient	Та	In normal operati	on mode	-40 to +85	°C
temperature		In flash memory	programming mode		
Storage temperature	Tstg			-65 to +150	°C

Absolute Maximum Ratings (TA = 25°C) (2/2)

- Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.
- **Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.



- **Notes 1.** Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. During HALT instruction execution by flash memory.
 - 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 4. When high-speed system clock and subsystem clock are stopped.
 - When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 - 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: 2.7 V \leq V_{DD} \leq 5.5 V@1 MHz to 32 MHz
 - 2.4 V \leq V_{DD} \leq 5.5 V@1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8 \text{ V} \le V_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 8 MHz
 - LV (low-voltage main) mode: 1.6 V \leq V_{DD} \leq 5.5 V@1 MHz to 4 MHz
 - 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - **3.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C



- **Notes 1.** Total current flowing into VDD, EVDDO, and EVDD1, including the input leakage current flowing when the level of the input pin is fixed to VDD, EVDDO, and EVDD1, or Vss, EVSSO, and EVSS1. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 - 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 - 3. When high-speed system clock and subsystem clock are stopped.
 - 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
 - **5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V} @ 1 \text{ MHz}$ to 32 MHz
 - 2.4 V \leq V_{DD} \leq 5.5 V@1 MHz to 16 MHz
 - LS (low-speed main) mode: $~~1.8~V \leq V_{\text{DD}} \leq 5.5~V~$ @1 MHz to 8 MHz
 - LV (low-voltage main) mode: 1.6 V \leq V_DD \leq 5.5 V@1 MHz to 4 MHz
- Remarks 1. fmx: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 - 2. fin: High-speed on-chip oscillator clock frequency
 - **3.** fsub: Subsystem clock frequency (XT1 clock oscillation frequency)
 - 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^{\circ}C$



2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V \leq EVDD0 = EVDD1 \leq VDD \leq 5.5 V, Vss = EVss0 = EVss1 = 0 V)

Items	Symbol		Conditions	3	MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum Tcy Main HS (HS (high-	$2.7~V{\leq}V_{\text{DD}}{\leq}5.5~V$	0.03125		1	μS	
instruction execution time)		system clock (fmain)	speed main) mode	$2.4 \text{ V} \le \text{V}_{DD} < 2.7 \text{ V}$	0.0625		1	μs
		operation	LS (low-speed main) mode	$1.8 V \le V_{DD} \le 5.5 V$	0.125		1	μS
			LV (low- voltage main) mode	$1.6~V \le V_{DD} \le 5.5~V$	0.25		1	μs
		Subsystem of	clock (fsua)	$1.8V\!\le\!V_{DD}\!\le\!5.5V$	28.5	30.5	31.3	μS
		operation	[
		In the self	HS (high-	$2.7 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$	0.03125		1	μS
		mode	mode	$2.4 V \le V_{DD} < 2.7 V$	0.0625		1	μS
			LS (low-speed main) mode	$1.8V\!\leq\!V_{DD}\!\leq\!5.5V$	0.125		1	μS
			LV (low- voltage main) mode	$1.8 \text{ V} \le \text{V}_{\text{DD}} \le 5.5 \text{ V}$	0.25		1	μS
External system clock	fex	$2.7 \text{ V} \leq \text{V}_{\text{DD}}$	≤ 5.5 V	I	1.0		20.0	MHz
frequency		$2.4 V \le V_{DD}$	< 2.7 V		1.0		16.0	MHz
		$1.8 V \le V_{DD}$	< 2.4 V		1.0		8.0	MHz
		$1.6 \text{ V} \leq \text{V}_{\text{DD}} < 1.8 \text{ V}$			1.0		4.0	MHz
	fexs				32		35	kHz
External system clock input	texh, texl	$2.7 \ V \le V_{DD}$	24			ns		
high-level width, low-level width		$2.4 \text{ V} \leq \text{V}_{\text{DD}} < 2.7 \text{ V}$			30			ns
		$1.8 V \le V_{DD}$	< 2.4 V		60			ns
		$1.6 V \le V_{DD}$	$1.6 \text{ V} \leq \text{V}_{\text{DD}} < 1.8 \text{ V}$					ns
	texhs, texls				13.7			μS
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	tтıн, tтı∟				1/fмск+10			ns ^{Note}
TO00 to TO07, TO10 to TO17	fтo	HS (high-spe	eed 4.0 V	$\leq EV_{DD0} \leq 5.5 V$			16	MHz
output frequency		main) mode	2.7 V	$\leq EV_{DD0} < 4.0 V$			8	MHz
			1.8 V	$\leq EV_{DD0} < 2.7 V$			4	MHz
			1.6 V	\leq EV _{DD0} < 1.8 V			2	MHz
		LS (low-spee	ed 1.8 V	$\leq EV_{DD0} \leq 5.5 V$			4	MHz
			1.6 V	$\leq EV_{DD0} < 1.8 V$			2	MHz
		LV (low-volta main) mode	age 1.6 V	$\leq EV$ DD0 $\leq 5.5 V$			2	MHz
PCLBUZ0, PCLBUZ1 output	f PCL	HS (high-spe	eed 4.0 V	$\leq EV_{DD0} \leq 5.5 V$			16	MHz
nequency		main) mode	2.7 V	$\leq EV_{DD0} < 4.0 V$			8	MHz
			1.8 V	$\leq EV_{DD0} < 2.7 V$			4	MHz
		10 //	1.6 V	\leq EV _{DD0} < 1.8 V			2	MHz
		LS (IOW-Spee main) mode	ea 1.8 V	$\leq EVDD0 \leq 5.5 V$			4	MIHZ
			1.6 V	$\leq EVDD0 < 1.8 V$			2	
		main) mode	1.8 V	$\geq EVDD0 \leq 5.5 V$			4	IVIHZ M⊔⇒
Interrupt input high-lovel width	tiniti i		1.0 V		1		2	IVII⊓∠ ./e
low-level width	tINTL		1.0 V	< EVDD < 5.5 V	1			μs
Key interrupt input low-level	tkB	KB0 to KR7	1.0 V	$\leq \mathrm{EV}_{\mathrm{DD0}} \leq 5.5 \mathrm{V}$	250			μο ne
width			1.6 V	< EV _{DD0} < 1.8 V	1		<u> </u>	<i>u</i> s
RESET low-level width	trsl				10			μs

(Note and Remark are listed on the next page.)



Parameter	Parameter Symbol Conditions		HS (hig main)	h-speed Mode	LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fsc∟	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ $C_b = 50 \text{ pF}, \text{ R}_b = 2.7 \text{ k}\Omega$		1000 Note 1		400 Note 1		400 Note 1	kHz
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 3 \text{ k}\Omega$		400 Note 1		400 Note 1		400 Note 1	kHz
		$\label{eq:linear} \begin{array}{l} 1.8 \mbox{ V} \leq EV_{\mbox{DD0}} < 2.7 \mbox{ V}, \\ C_{\mbox{b}} = 100 \mbox{ pF}, \mbox{ R}_{\mbox{b}} = 5 k\Omega \end{array}$		300 Note 1		300 Note 1		300 Note 1	kHz
		$1.7 \text{ V} \leq \text{EV}_{\text{DD0}} < 1.8 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 5 \text{ k}\Omega$		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV _{DD0} < 1.8 V, C₀ = 100 pF, R₀ = 5 kΩ		_		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	tLow	$2.7 \text{ V} \le \text{EV}_{\text{DD0}} \le 5.5 \text{ V},$ $C_{\text{b}} = 50 \text{ pF}, \text{ R}_{\text{b}} = 2.7 \text{ k}\Omega$	475		1150		1150		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 3 \text{ k}\Omega$	1150		1150		1150		ns
		1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		$1.7 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 5 \text{ k}\Omega$	1850		1850		1850		ns
		$1.6 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 5 \text{ k}\Omega$			1850		1850		ns
Hold time when SCLr = "H"	tніgн	$\begin{array}{l} 2.7 \ \text{V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \ \text{V}, \\ \text{C}_{\text{b}} = 50 \ \text{pF}, \ \text{R}_{\text{b}} = 2.7 \ \text{k}\Omega \end{array}$	475		1150		1150		ns
		$1.8 \text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 3 \text{ k}\Omega$	1150		1150		1150		ns
		1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		$1.7 \text{ V} \le \text{EV}_{\text{DD0}} < 1.8 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 5 \text{ k}\Omega$	1850		1850		1850		ns
		$1.6 \text{ V} \leq \text{EV}_{\text{DD0}} < 1.8 \text{ V},$ $C_{\text{b}} = 100 \text{ pF}, \text{ R}_{\text{b}} = 5 \text{ k}\Omega$	_		1850		1850		ns

(5) During communication at same potential (simplified I²C mode) (1/2)

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)







- **2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- **3.** fMCK: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
- **4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.



(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

Parameter	Symbol	Conditions	HS (higl main)	h-speed Mode	LS (low main)	r-speed Mode	LV (low main)	LV (low-voltage main) Mode	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) ^{Note 1}	tsikı	$\begin{array}{l} 4.0 \ V \leq EV_{\text{DD0}} \leq 5.5 \ V, \\ 2.7 \ V \leq V_b \leq 4.0 \ V, \end{array}$	44		110		110		ns
		$C_b = 30 \text{ pF}, \text{ R}_b = 1.4 \text{ k}\Omega$							
		$\begin{array}{l} 2.7 \ V \leq EV_{\text{DD0}} < 4.0 \ V, \\ 2.3 \ V \leq V_{\text{b}} \leq 2.7 \ V, \end{array}$	44		110		110		ns
		$C_{b}=30 \text{ pF}, \text{ R}_{b}=2.7 \text{ k}\Omega$							
		$ \begin{split} 1.8 \ V &\leq EV_{\text{DD0}} < 3.3 \ V, \\ 1.6 \ V &\leq V_b \leq 2.0 \ V^{\text{Note 2}}, \end{split} $	110		110		110		ns
		C_b = 30 pF, R_b = 5.5 k Ω							
SIp hold time (from SCKp↓) ^{№ te 1}	tksi1	$\label{eq:linear_states} \begin{array}{l} 4.0 \ V \leq EV_{\text{DD0}} \leq 5.5 \ V, \\ 2.7 \ V \leq V_{\text{b}} \leq 4.0 \ V, \end{array}$	19		19		19		ns
		C_b = 30 pF, R_b = 1.4 k Ω							
		$\begin{array}{l} 2.7 \ V \leq EV_{\text{DD0}} < 4.0 \ V, \\ 2.3 \ V \leq V_{b} \leq 2.7 \ V, \end{array}$	19		19		19		ns
		C_b = 30 pF, R_b = 2.7 k Ω							
		$ \begin{aligned} 1.8 \ V &\leq EV_{\text{DD0}} < 3.3 \ V, \\ 1.6 \ V &\leq V_{\text{b}} \leq 2.0 \ V^{\text{Note 2}}, \end{aligned} $	19		19		19		ns
		$C_{b}=30 \text{ pF}, \text{R}_{b}=5.5 \text{k}\Omega$							
Delay time from SCKp↑ to	tkso1			25		25		25	ns
SOp output Note 1		C_b = 30 pF, R_b = 1.4 k Ω							
		$\begin{array}{l} 2.7 \ V \leq EV_{DD0} < 4.0 \ V, \\ 2.3 \ V \leq V_b \leq 2.7 \ V, \end{array}$		25		25		25	ns
		C_b = 30 pF, R_b = 2.7 k Ω							
		$\label{eq:linear} \begin{split} 1.8 \ V &\leq E V_{\text{DD0}} < 3.3 \ V, \\ 1.6 \ V &\leq V_b \leq 2.0 \ V^{\text{Note 2}}, \end{split}$		25		25		25	ns
		C_b = 30 pF, R_b = 5.5 k Ω							

1	$(T_A = -40 \text{ to } +85^{\circ}\text{C} + 1.8 \text{ V} \le \text{EV}_{DD} = \text{EV}_{D1} \le \text{V}_{D2} \le 5.5$	5 V	$V_{SS} = FV_{SS0} = FV_{SS1} = 0 V$
١.	$(1A = -40 10 + 05 0, 1.0 4 \le 24000 = 24001 \le 400 \le 5.5$, v ;	$, v_{33} - \Box v_{330} - \Box v_{331} - O v_{j}$

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. Use it with $EV_{DD0} \ge V_b$.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (When 20- to 52-pin products)/EVDD tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)



CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential) (When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,

n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.



2.6.5 Power supply voltage rising slope characteristics

$(T_A = -40 \text{ to } +85^{\circ}C, V_{SS} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

$(T_A = -40 \text{ to } +85^{\circ}\text{C}, \text{Vss} = 0 \text{ V})$

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.







CSI mode serial transfer timing (during communication at same potential) (When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)





Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)



Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	fsc∟	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V,$		400 ^{Note1}	kHz
		$C_b = 50 \text{ pF}, \text{ R}_b = 2.7 \text{ k}\Omega$			
		$2.4~V \leq EV_{\text{DD0}} \leq 5.5~V,$		100 ^{Note1}	kHz
		$C_b = 100 \text{ pF}, \text{ R}_b = 3 \text{ k}\Omega$			
Hold time when SCLr = "L"	t∟ow	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V,$	1200		ns
		$C_b = 50 \text{ pF}, \text{ R}_b = 2.7 \text{ k}\Omega$			
		$2.4~V \leq EV_{\text{DD0}} \leq 5.5~V,$	4600		ns
		$C_b = 100 \text{ pF}, \text{ R}_b = 3 \text{ k}\Omega$			
Hold time when SCLr = "H"	tніgн	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V,$	1200		ns
		$C_b = 50 \text{ pF}, \text{ R}_b = 2.7 \text{ k}\Omega$			
		$2.4~V \leq EV_{\text{DD0}} \leq 5.5~V,$	4600		ns
		$C_b = 100 \text{ pF}, R_b = 3 \text{ k}\Omega$			
Data setup time (reception)	tsu:dat	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V,$	1/fмск + 220		ns
		$C_b = 50 \text{ pF}, \text{R}_b = 2.7 \text{ k}\Omega$	Note2		
		$2.4~V \leq EV_{\text{DD}} \leq 5.5~V,$	1/fмск + 580		ns
		$C_b = 100 \text{ pF}, R_b = 3 \text{ k}\Omega$	Note2		
Data hold time (transmission)	thd:dat	$2.7~V \leq EV_{\text{DD0}} \leq 5.5~V,$	0	770	ns
		$C_b = 50 \text{ pF}, \text{ R}_b = 2.7 \text{ k}\Omega$			
		$2.4~V \leq EV_{\text{DD0}} \leq 5.5~V,$	0	1420	ns
		$C_b = 100 \text{ pF}, R_b = 3 \text{ k}\Omega$			

(4) During communication at same potential (simplified I²C mode)

 $(T_A = -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{DD0} = \text{EV}_{DD1} \le \text{V}_{DD} \le 5.5 \text{ V}, \text{ V}_{SS} = \text{EV}_{SS0} = \text{EV}_{SS1} = 0 \text{ V})$

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

- 2. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".
- Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)



Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



- **Remarks 1.** R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
 h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - 3. fmck: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m

= 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)



Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	tsu:dat		1/fмск + 340 Note 2		ns
		$\label{eq:VDD} \begin{array}{l} 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ 2.3 \; V \leq V_b \leq 2.7 \; V, \\ C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{array}$	1/fмск + 340 Note 2		ns
			1/f _{MCK} + 760 _{Note 2}		ns
		$\label{eq:2.7} \begin{split} & 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ & 2.3 \; V \leq V_b \leq 2.7 \; V, \\ & C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$	1/fмск + 760 Note 2		ns
		$\label{eq:2.4} \begin{split} & 2.4 \; V \leq EV_{DD0} < 3.3 \; V, \\ & 1.6 \; V \leq V_b \leq 2.0 \; V, \\ & C_b = 100 \; pF, \; R_b = 5.5 \; k\Omega \end{split}$	1/fмск + 570 Note 2		ns
Data hold time (transmission)) thd:dat		0	770	ns
		$\label{eq:2.7} \begin{split} & 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ & 2.3 \; V \leq V_b \leq 2.7 \; V, \\ & C_b = 50 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$	0	770	ns
			0	1420	ns
		$\label{eq:2.7} \begin{split} & 2.7 \; V \leq EV_{DD0} < 4.0 \; V, \\ & 2.3 \; V \leq V_b \leq 2.7 \; V, \\ & C_b = 100 \; pF, \; R_b = 2.7 \; k\Omega \end{split}$	0	1420	ns
		$\label{eq:2.4} \begin{split} 2.4 \; V &\leq EV_{DD0} < 3.3 \; V, \\ 1.6 \; V &\leq V_b \leq 2.0 \; V, \\ C_b &= 100 \; pF, \; R_b = 5.5 \; k\Omega \end{split}$	0	1215	ns

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2) (T_A = -40 to +105°C, 2.4 V \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 V, Vss = EV_{SS0} = EV_{SS1} = 0 V)

Notes 1. The value must also be equal to or less than $f_{MCK}/4$.

2. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)



(3) When reference voltage (+) = VDD (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = Vss (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T ₄	$= -40 \text{ to } +105^{\circ}\text{C}, 2.4 \text{ V} \le \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \le \text{V}_{\text{DD}} \le 5.$	5.5 V, Vss = EVsso = EVss1 = 0 V, Reference voltage (+)	=
Vdd,	, Reference voltage (–) = Vss)		

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$		1.2	±7.0	LSB
Conversion time too	tconv	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	$3.6~V \leq V \text{DD} \leq 5.5~V$	2.125		39	μs
			$2.7~V \leq V \text{DD} \leq 5.5~V$	3.1875		39	μS
			$2.4~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS	$3.6~V \leq V \text{DD} \leq 5.5~V$	2.375		39	μs
			$2.7~V \leq V \text{DD} \leq 5.5~V$	3.5625		39	μs
			$2.4~V \leq V \text{DD} \leq 5.5~V$	17		39	μs
(high-speed main) n		(high-speed main) mode)					
Zero-scale error ^{Notes 1, 2}	Ezs	10-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±0.60	%FSR
Full-scale error ^{Notes 1, 2}	Ers	10-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±0.60	%FSR
Integral linearity errorNote 1	ILE	10-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±4.0	LSB
Differential linearity error	DLE	10-bit resolution	$2.4~V \leq V \text{DD} \leq 5.5~V$			±2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI14		0		Vdd	V
ANI16 to ANI26			0		EVDD0	V	
		Internal reference voltage output		VBGR Note 3			V
		$\label{eq:constraint} \begin{array}{l} (2.4 \ V \leq V \mbox{DD} \leq 5.5 \ V, \mbox{HS} \ (high-speed \ main) \ mode) \\ \\ \hline Temperature \ sensor \ output \ voltage \\ (2.4 \ V \leq V \mbox{DD} \leq 5.5 \ V, \ HS \ (high-speed \ main) \ mode) \end{array}$					
					VTMPS25 Note 3		

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

- $\ensuremath{\textbf{2.}}$ This value is indicated as a ratio (%FSR) to the full-scale value.
- 3. Refer to 3.6.2 Temperature sensor/internal reference voltage characteristics.



		Description		
Rev.	Date	Page	Summary	
3.00	Aug 02, 2013	118	Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics	
		118	Modification of table and note in 2.6.3 POR circuit characteristics	
		119	Modification of table in 2.6.4 LVD circuit characteristics	
		120	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode	
		120	Renamed to 2.6.5 Power supply voltage rising slope characteristics	
		122	Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes	
		123	Modification of caution 1 and description	
		124	Modification of table and remark 3 in Absolute Maximum Ratings (T _A = 25°C)	
		126	Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics	
		126	Modification of table in 3.2.2 On-chip oscillator characteristics	
		127	Modification of note 3 in 3.3.1 Pin characteristics (1/5)	
		128	Modification of note 3 in 3.3.1 Pin characteristics (2/5)	
		133	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2)	
		135	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64- pin products (2/2)	
		137	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100- pin products (1/2)	
		139	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2)	
		140	Modification of (3) Peripheral Functions (Common to all products)	
		142	Modification of table in 3.4 AC Characteristics	
		143	Addition of Minimum Instruction Execution Time during Main System Clock Operation	
		143	Modification of figure of AC Timing Test Points	
		143	Modification of figure of External System Clock Timing	
		145	Modification of figure of AC Timing Test Points	
		145	Modification of description, note 1, and caution in (1) During communication at same potential (UART mode)	
		146	Modification of description in (2) During communication at same potential (CSI mode)	
		147	Modification of description in (3) During communication at same potential (CSI mode)	
		149	Modification of table, note 1, and caution in (4) During communication at same potential (simplified I ² C mode)	
		151	Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)	
		152 to 154	Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)	
		155	Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)	
		156	Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)	
		157, 158	Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)	
		160, 161	Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)	