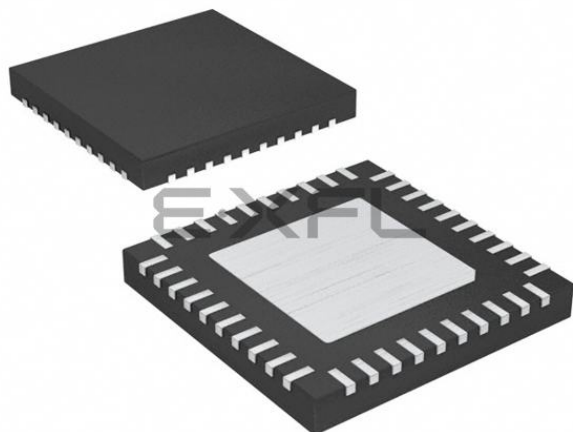




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101eeana-u0

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G13					
			20 pins	24 pins	25 pins	30 pins	32 pins	36 pins
128 KB	8 KB	12 KB	–	–	–	R5F100AG	R5F100BG	R5F100CG
	–		–	–	–	R5F101AG	R5F101BG	R5F101CG
96 KB	8 KB	8 KB	–	–	–	R5F100AF	R5F100BF	R5F100CF
	–		–	–	–	R5F101AF	R5F101BF	R5F101CF
64 KB	4 KB	4 KB Note	R5F1006E	R5F1007E	R5F1008E	R5F100AE	R5F100BE	R5F100CE
	–		R5F1016E	R5F1017E	R5F1018E	R5F101AE	R5F101BE	R5F101CE
48 KB	4 KB	3 KB Note	R5F1006D	R5F1007D	R5F1008D	R5F100AD	R5F100BD	R5F100CD
	–		R5F1016D	R5F1017D	R5F1018D	R5F101AD	R5F101BD	R5F101CD
32 KB	4 KB	2 KB	R5F1006C	R5F1007C	R5F1008C	R5F100AC	R5F100BC	R5F100CC
	–		R5F1016C	R5F1017C	R5F1018C	R5F101AC	R5F101BC	R5F101CC
16 KB	4 KB	2 KB	R5F1006A	R5F1007A	R5F1008A	R5F100AA	R5F100BA	R5F100CA
	–		R5F1016A	R5F1017A	R5F1018A	R5F101AA	R5F101BA	R5F101CA

Flash ROM	Data flash	RAM	RL78/G13							
			40 pins	44 pins	48 pins	52 pins	64 pins	80 pins	100 pins	128 pins
512 KB	8 KB	32 KB Note	–	R5F100FL	R5F100GL	R5F100JL	R5F100LL	R5F100ML	R5F100PL	R5F100SL
	–		–	R5F101FL	R5F101GL	R5F101JL	R5F101LL	R5F101ML	R5F101PL	R5F101SL
384 KB	8 KB	24 KB	–	R5F100FK	R5F100GK	R5F100JK	R5F100LK	R5F100MK	R5F100PK	R5F100SK
	–		–	R5F101FK	R5F101GK	R5F101JK	R5F101LK	R5F101MK	R5F101PK	R5F101SK
256 KB	8 KB	20 KB Note	–	R5F100FJ	R5F100GJ	R5F100JJ	R5F100LJ	R5F100MJ	R5F100PJ	R5F100SJ
	–		–	R5F101FJ	R5F101GJ	R5F101JJ	R5F101LJ	R5F101MJ	R5F101PJ	R5F101SJ
192 KB	8 KB	16 KB	R5F100EH	R5F100FH	R5F100GH	R5F100JH	R5F100LH	R5F100MH	R5F100PH	R5F100SH
	–		R5F101EH	R5F101FH	R5F101GH	R5F101JH	R5F101LH	R5F101MH	R5F101PH	R5F101SH
128 KB	8 KB	12 KB	R5F100EG	R5F100FG	R5F100GG	R5F100JG	R5F100LG	R5F100MG	R5F100PG	–
	–		R5F101EG	R5F101FG	R5F101GG	R5F101JG	R5F101LG	R5F101MG	R5F101PG	–
96 KB	8 KB	8 KB	R5F100EF	R5F100FF	R5F100GF	R5F100JF	R5F100LF	R5F100MF	R5F100PF	–
	–		R5F101EF	R5F101FF	R5F101GF	R5F101JF	R5F101LF	R5F101MF	R5F101PF	–
64 KB	4 KB	4 KB Note	R5F100EE	R5F100FE	R5F100GE	R5F100JE	R5F100LE	–	–	–
	–		R5F101EE	R5F101FE	R5F101GE	R5F101JE	R5F101LE	–	–	–
48 KB	4 KB	3 KB Note	R5F100ED	R5F100FD	R5F100GD	R5F100JD	R5F100LD	–	–	–
	–		R5F101ED	R5F101FD	R5F101GD	R5F101JD	R5F101LD	–	–	–
32 KB	4 KB	2 KB	R5F100EC	R5F100FC	R5F100GC	R5F100JC	R5F100LC	–	–	–
	–		R5F101EC	R5F101FC	R5F101GC	R5F101JC	R5F101LC	–	–	–
16 KB	4 KB	2 KB	R5F100EA	R5F100FA	R5F100GA	–	–	–	–	–
	–		R5F101EA	R5F101FA	R5F101GA	–	–	–	–	–

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C, E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = 6 to 8, A to C, E to G, J, L): Start address FEF00H

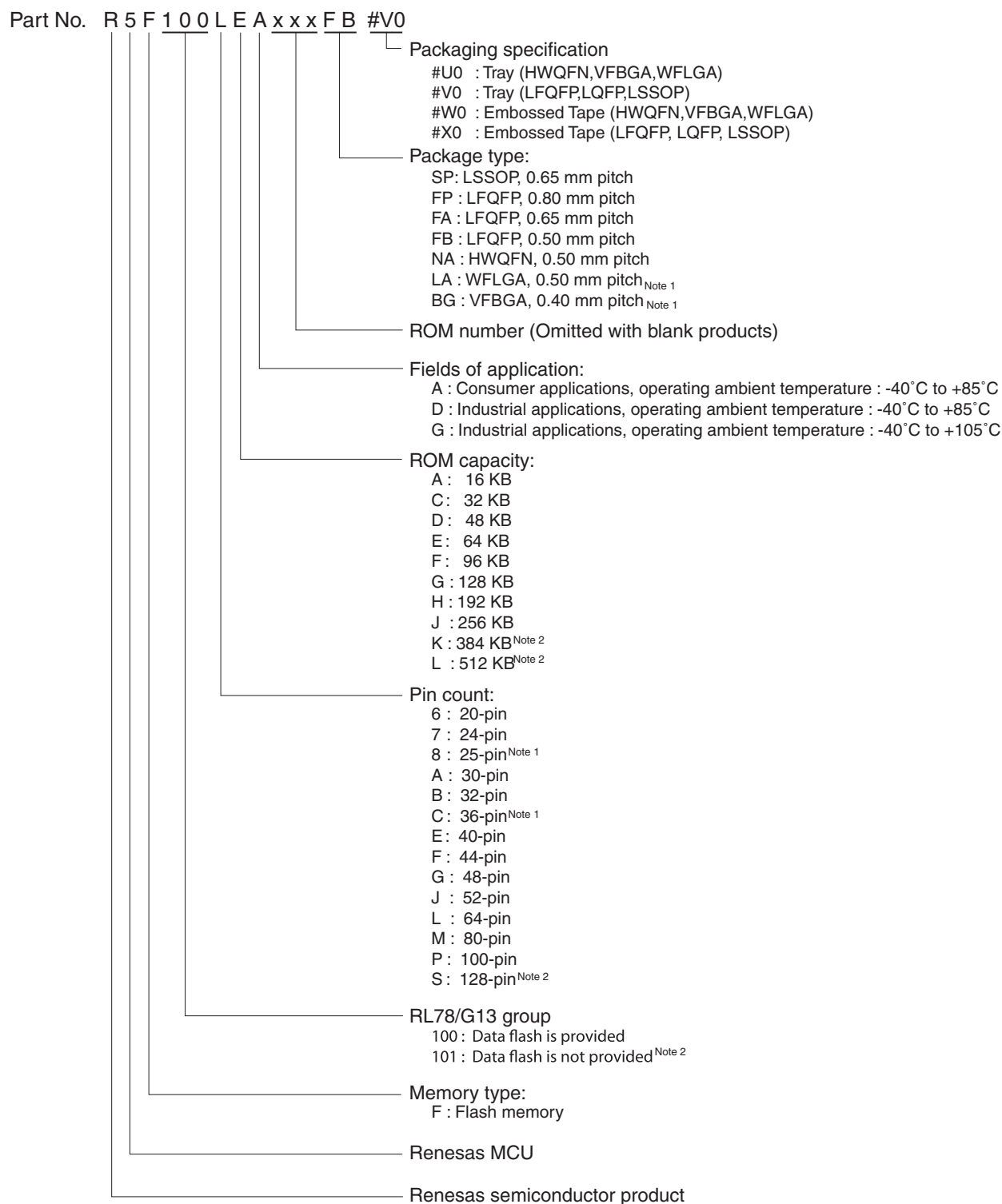
R5F100xJ, R5F101xJ (x = F, G, J, L, M, P): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L, M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 List of Part Numbers

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13



- Notes**
1. Products only for "A: Consumer applications ($T_A = -40$ to $+85^\circ\text{C}$)", and "G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$)"
 2. Products only for "A: Consumer applications ($T_A = -40$ to $+85^\circ\text{C}$)", and "D: Industrial applications ($T_A = -40$ to $+85^\circ\text{C}$)"

3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
4. When setting to PIOR = 1

(2/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Clock output/buzzer output		—		1		1		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)											
8/10-bit resolution A/D converter		6 channels		6 channels		6 channels		8 channels		8 channels		8 channels	
Serial interface		[20-pin, 24-pin, 25-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel [30-pin, 32-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I ² C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I ² C: 2 channels/UART (UART supporting LIN-bus): 1 channel											
		I ² C bus	—		1 channel		1 channel		1 channel		1 channel		1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)											
DMA controller		2 channels											
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt		—											
Reset		• Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access											
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)											
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)											
On-chip debug function		Provided											
Power supply voltage		V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)											
Operating ambient temperature		T _A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T _A = 40 to +105°C (G: Industrial applications)											

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I _{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I _{OH2}	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
	Output current, low	I _{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
I _{OL2}		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		T _A	In normal operation mode		−40 to +85
	In flash memory programming mode				
Storage temperature	T _{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit				
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.1		mA			
						V _{DD} = 3.0 V		2.1		mA			
					Normal operation	V _{DD} = 5.0 V		4.6	7.0	mA			
						V _{DD} = 3.0 V		4.6	7.0	mA			
					f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.7	5.5	mA		
							V _{DD} = 3.0 V		3.7	5.5	mA		
				f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		2.7	4.0	mA			
						V _{DD} = 3.0 V		2.7	4.0	mA			
				LS (low-speed main) mode Note 5	f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.2	1.8	mA		
							V _{DD} = 2.0 V		1.2	1.8	mA		
				LV (low-voltage main) mode Note 5	f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.2	1.7	mA		
							V _{DD} = 2.0 V		1.2	1.7	mA		
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2 , V _{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA			
						Resonator connection		3.2	4.8	mA			
					f _{MX} = 20 MHz Note 2 , V _{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA		
							Resonator connection		3.2	4.8	mA		
					f _{MX} = 10 MHz Note 2 , V _{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA		
							Resonator connection		1.9	2.7	mA		
					f _{MX} = 10 MHz Note 2 , V _{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA		
							Resonator connection		1.9	2.7	mA		
					LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2 , V _{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA	
								Resonator connection		1.1	1.7	mA	
							f _{MX} = 8 MHz Note 2 , V _{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
									Resonator connection		1.1	1.7	mA
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 T _A = −40°C	Normal operation	Square wave input		4.1	4.9	μA				
					Resonator connection		4.2	5.0	μA				
			f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation	Square wave input		4.1	4.9	μA				
					Resonator connection		4.2	5.0	μA				
			f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation	Square wave input		4.2	5.5	μA				
					Resonator connection		4.3	5.6	μA				
			f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		4.3	6.3	μA				
					Resonator connection		4.4	6.4	μA				
			f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		4.6	7.7	μA				
					Resonator connection		4.7	7.8	μA				

(Notes and Remarks are listed on the next page.)

(5) During communication at same potential (simplified I²C mode) (2/2)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		1/f _{MCK} + 145 Note2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		1/f _{MCK} + 230 Note2		ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1/f _{MCK} + 290 Note2		1/f _{MCK} + 290 Note2		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(2/3)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note 1}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) ^{Note 1}	t _{KSH1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output ^{Note 1}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ		483		483		483	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. Use it with EV_{DD0} ≥ V_b.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

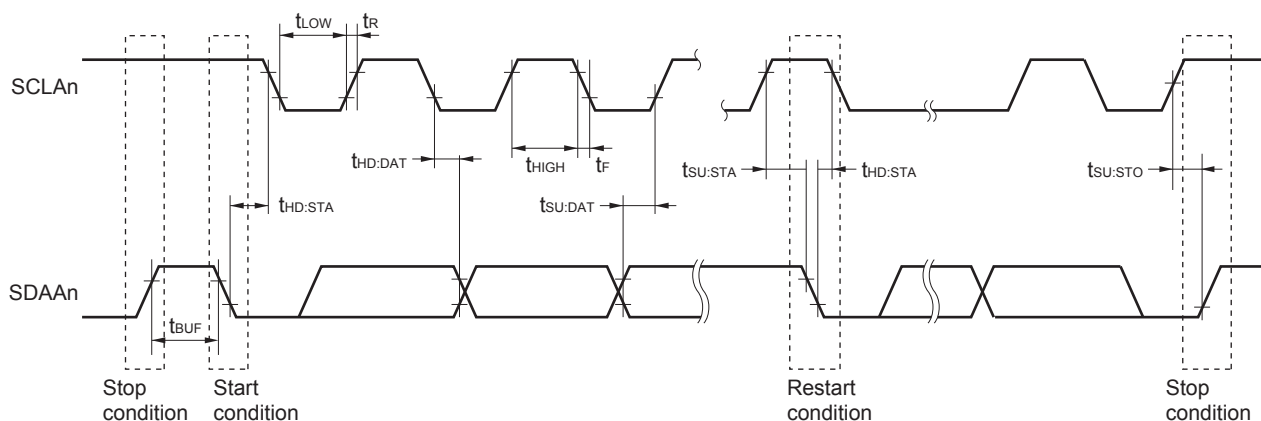
(3) I²C fast mode plus(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0	0.45	—	—	—	—	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.<R> 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ**I²C serial transfer timing****Remark** n = 0, 1

(3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V_{SS} (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (–) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
Conversion time	t _{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI14	0			V _{DD}	V
		ANI16 to ANI26	0			EV _{DD0}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{BGR} ^{Note 4}				V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)	V _{TMPS25} ^{Note 4}				V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

4. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +85°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V		
			Power supply fall time	2.60	2.65	2.70	V		
		V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V		
			Power supply fall time	2.50	2.55	2.60	V		
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V		
			Power supply fall time	2.40	2.45	2.50	V		
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V		
			Power supply fall time	2.00	2.04	2.08	V		
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V		
			Power supply fall time	1.90	1.94	1.98	V		
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V		
			Power supply fall time	1.80	1.84	1.87	V		
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V		
			Power supply fall time	1.70	1.73	1.77	V		
		V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V		
			Power supply fall time	1.60	1.63	1.66	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time						300	μs

2.8 Flash Memory Programming Characteristics

(T_A = -40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	1.8 V ≤ V _{DD} ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years T _A = 85°C	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 years T _A = 25°C		1,000,000		
		Retained for 5 years T _A = 85°C	100,000			
		Retained for 20 years T _A = 85°C	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

(3) Peripheral Functions (Common to all products)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.20		μA
RTC operating current	I_{RTC} Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	$f_{\text{IL}} = 15\text{ kHz}$			0.22		μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$		1.3	1.7	mA
			Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF} Note 1				75.0		μA
Temperature sensor operating current	I_{TMPS} Note 1				75.0		μA
LVD operating current	I_{LVD} Notes 1, 7				0.08		μA
Self programming operating current	I_{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I_{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ} Note 1	ADC operation	The mode is performed ^{Note 10}		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

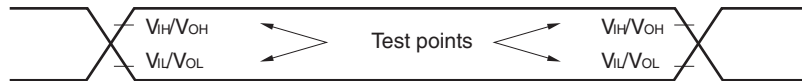
Notes 1. Current flowing to the V_{DD} .

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. $I_{\text{DD}2}$ subsystem clock operation includes the operational current of the real-time clock.4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{IT} , when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{WDT} when the watchdog timer operates.

3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq E_{VDD0} = E_{VDD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{VSS0} = E_{VSS1} = 0\text{ V}$)

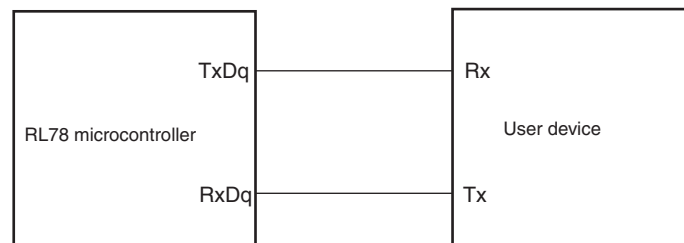
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate ^{Note 1}		Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$		$f_{MCK}/12$ ^{Note 2}	bps
				2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

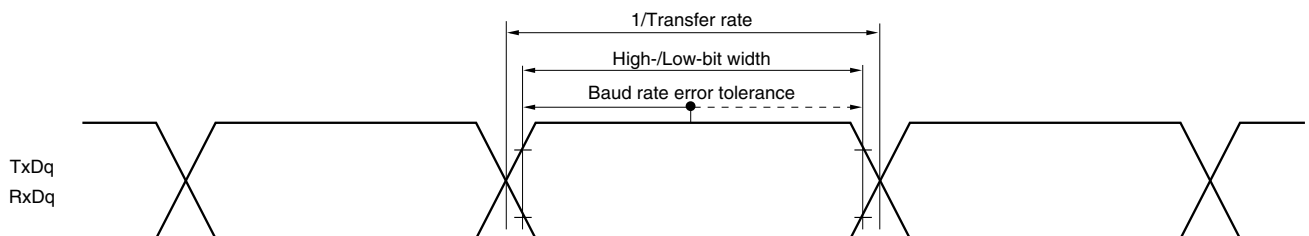
2. The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$.
 $2.4\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



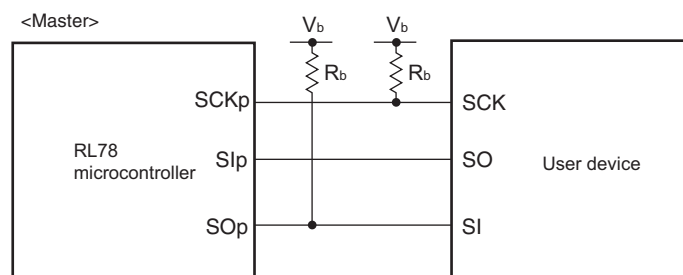
UART mode bit width (during communication at same potential) (reference)



Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at different potential)

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

3.5.2 Serial interface IICA

(T_A = -40 to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = “L”	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = “H”	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

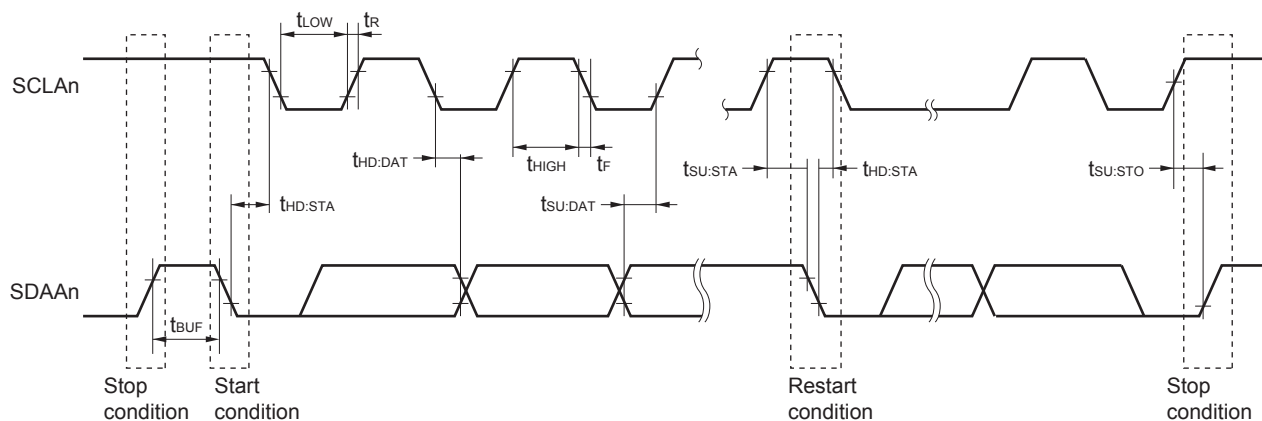
<R> 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩFast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing

**Remark** n = 0, 1

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP} Reference voltage (-) = AV_{REFM}	Reference voltage (+) = V_{DD} Reference voltage (-) = V_{SS}	Reference voltage (+) = V_{BGR} Reference voltage (-) = AV_{REFM}
ANI0 to ANI14	Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI26	Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 3.6.1 (1).		—

(1) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

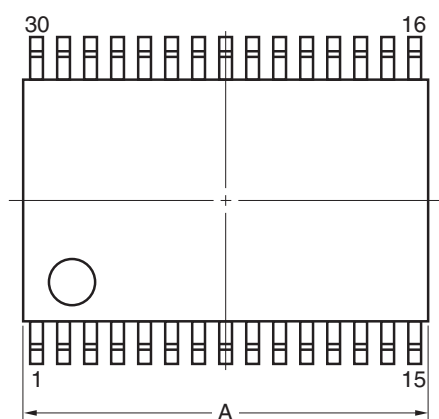
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 3.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin: ANI2 to ANI14	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.375	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.5625	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.25	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$ ^{Note 3}	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 1.5	LSB
Analog input voltage	V_{AIN}	ANI2 to ANI14	0		AV_{REFP}	V
		Internal reference voltage output ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{BGR} ^{Note 4}			V
		Temperature sensor output voltage ($2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode)	V_{TMPS25} ^{Note 4}			V

(Notes are listed on the next page.)

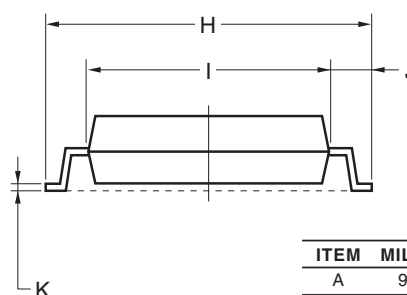
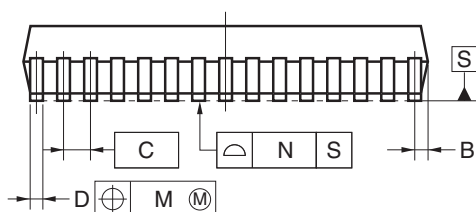
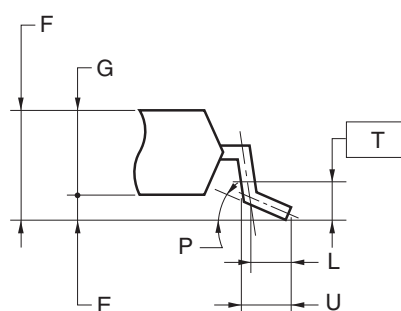
4.4 30-pin Products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
 R5F100AAGSP, R5F100ACGSP, R5F100ADGSP, R5F100AEGSP, R5F100AFGSP, R5F100AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



detail of lead end

**NOTE**

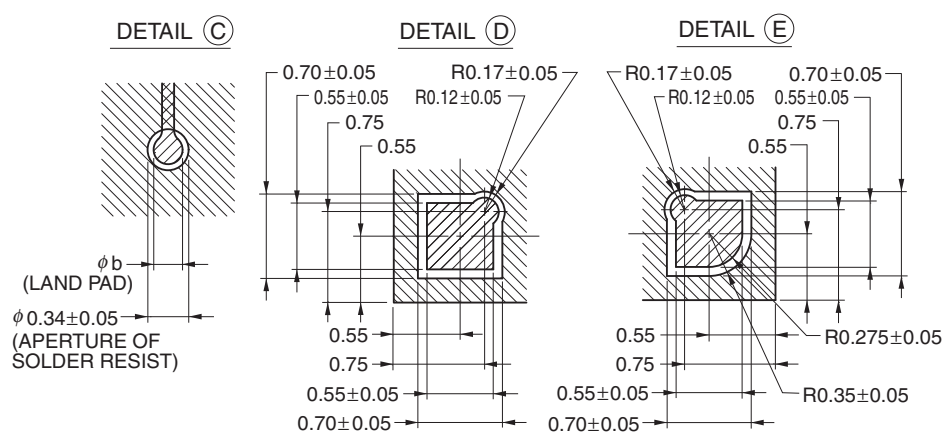
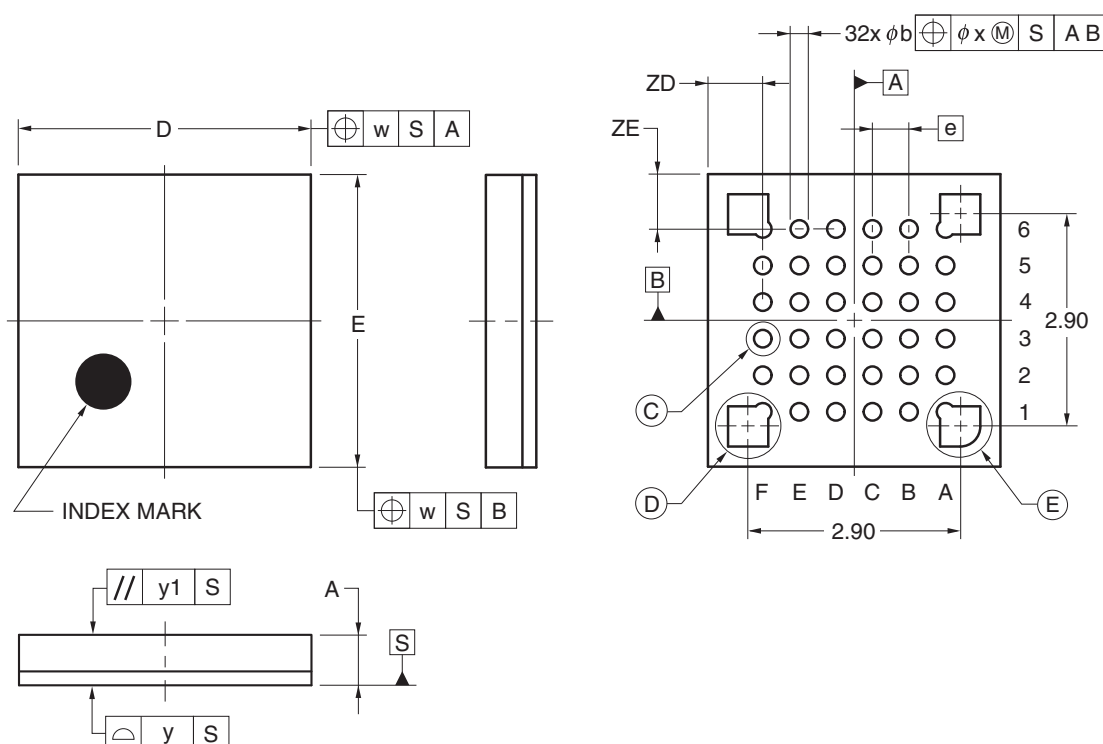
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
 R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
 R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023



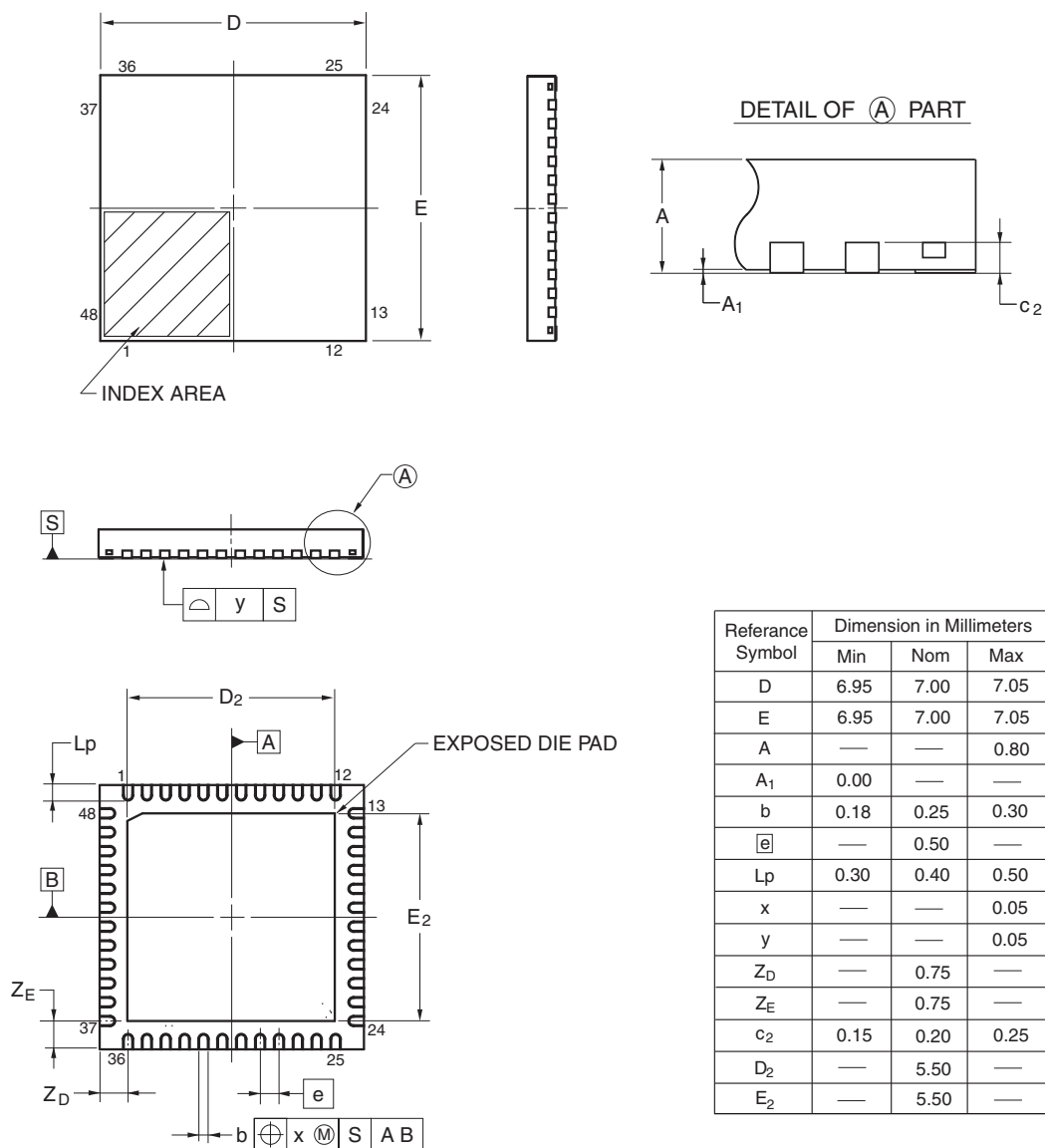
(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

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R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
 R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
 R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

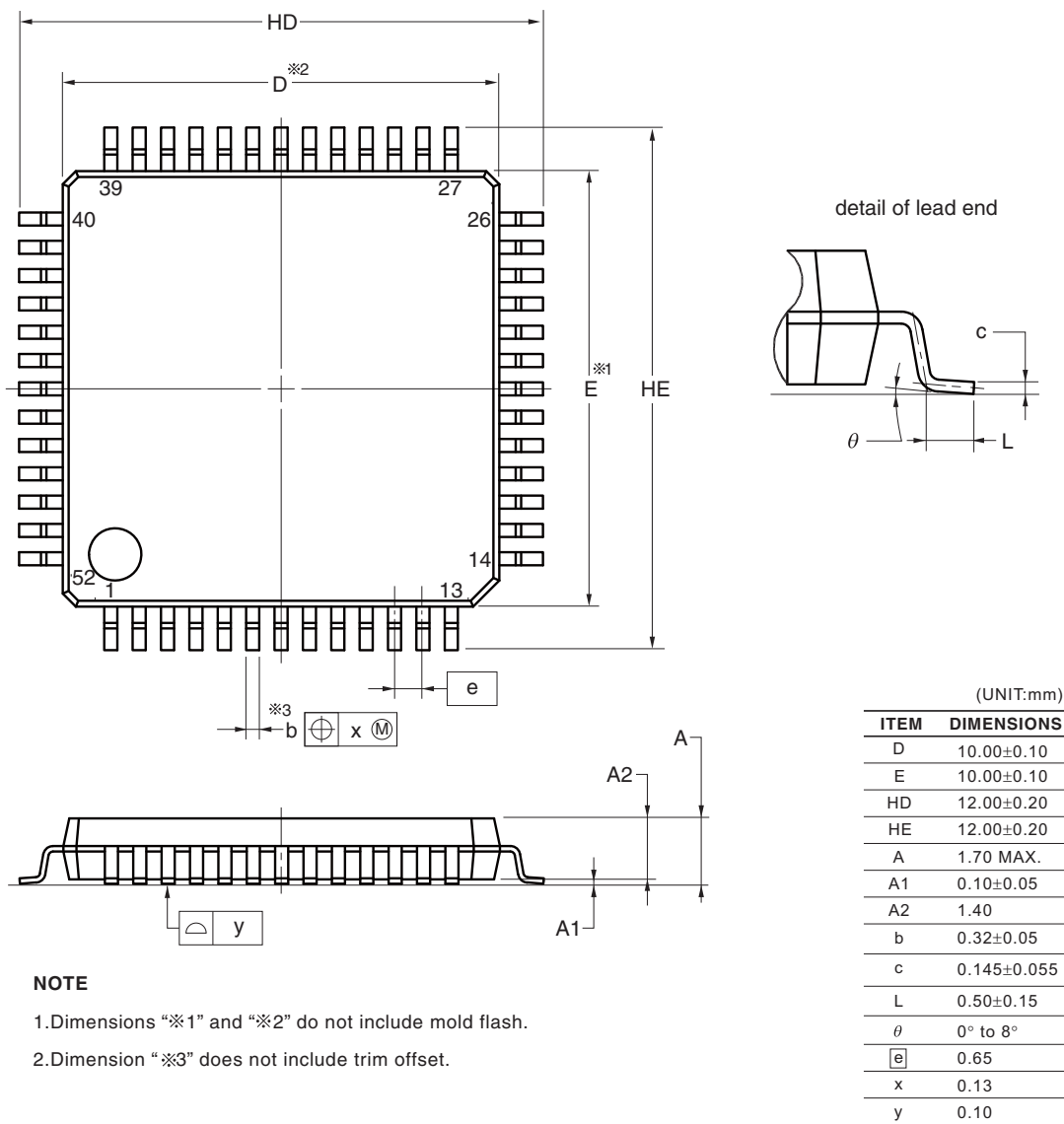


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4.10 52-pin Products

R5F100JCAFA, R5F100JDFA, R5F100JEFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFA, R5F100JKFA, R5F100JLAFA
 R5F101JCAFA, R5F101JDFA, R5F101JEFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFA, R5F101JKFA, R5F101JLAFA
 R5F100JCDA, R5F100JDDA, R5F100JEDA, R5F100JFDA, R5F100JGDA, R5F100JHDA, R5F100JJDA, R5F100JKDA, R5F100JLDA
 R5F101JCDA, R5F101JDDA, R5F101JEDA, R5F101JFDA, R5F101JGDA, R5F101JHDA, R5F101JJDA, R5F101JKDA, R5F101JLDA
 R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



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