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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I <sup>2</sup> C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	28
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 9x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-WFQFN Exposed Pad
Supplier Device Package	40-HWQFN (6x6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101egdna-u0">https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101egdna-u0</a>

## ○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G13					
			20 pins	24 pins	25 pins	30 pins	32 pins	36 pins
128 KB	8 KB	12 KB	–	–	–	R5F100AG	R5F100BG	R5F100CG
	–		–	–	–	R5F101AG	R5F101BG	R5F101CG
96 KB	8 KB	8 KB	–	–	–	R5F100AF	R5F100BF	R5F100CF
	–		–	–	–	R5F101AF	R5F101BF	R5F101CF
64 KB	4 KB	4 KB Note	R5F1006E	R5F1007E	R5F1008E	R5F100AE	R5F100BE	R5F100CE
	–		R5F1016E	R5F1017E	R5F1018E	R5F101AE	R5F101BE	R5F101CE
48 KB	4 KB	3 KB Note	R5F1006D	R5F1007D	R5F1008D	R5F100AD	R5F100BD	R5F100CD
	–		R5F1016D	R5F1017D	R5F1018D	R5F101AD	R5F101BD	R5F101CD
32 KB	4 KB	2 KB	R5F1006C	R5F1007C	R5F1008C	R5F100AC	R5F100BC	R5F100CC
	–		R5F1016C	R5F1017C	R5F1018C	R5F101AC	R5F101BC	R5F101CC
16 KB	4 KB	2 KB	R5F1006A	R5F1007A	R5F1008A	R5F100AA	R5F100BA	R5F100CA
	–		R5F1016A	R5F1017A	R5F1018A	R5F101AA	R5F101BA	R5F101CA

Flash ROM	Data flash	RAM	RL78/G13							
			40 pins	44 pins	48 pins	52 pins	64 pins	80 pins	100 pins	128 pins
512 KB	8 KB	32 KB Note	–	R5F100FL	R5F100GL	R5F100JL	R5F100LL	R5F100ML	R5F100PL	R5F100SL
	–		–	R5F101FL	R5F101GL	R5F101JL	R5F101LL	R5F101ML	R5F101PL	R5F101SL
384 KB	8 KB	24 KB	–	R5F100FK	R5F100GK	R5F100JK	R5F100LK	R5F100MK	R5F100PK	R5F100SK
	–		–	R5F101FK	R5F101GK	R5F101JK	R5F101LK	R5F101MK	R5F101PK	R5F101SK
256 KB	8 KB	20 KB Note	–	R5F100FJ	R5F100GJ	R5F100JJ	R5F100LJ	R5F100MJ	R5F100PJ	R5F100SJ
	–		–	R5F101FJ	R5F101GJ	R5F101JJ	R5F101LJ	R5F101MJ	R5F101PJ	R5F101SJ
192 KB	8 KB	16 KB	R5F100EH	R5F100FH	R5F100GH	R5F100JH	R5F100LH	R5F100MH	R5F100PH	R5F100SH
	–		R5F101EH	R5F101FH	R5F101GH	R5F101JH	R5F101LH	R5F101MH	R5F101PH	R5F101SH
128 KB	8 KB	12 KB	R5F100EG	R5F100FG	R5F100GG	R5F100JG	R5F100LG	R5F100MG	R5F100PG	–
	–		R5F101EG	R5F101FG	R5F101GG	R5F101JG	R5F101LG	R5F101MG	R5F101PG	–
96 KB	8 KB	8 KB	R5F100EF	R5F100FF	R5F100GF	R5F100JF	R5F100LF	R5F100MF	R5F100PF	–
	–		R5F101EF	R5F101FF	R5F101GF	R5F101JF	R5F101LF	R5F101MF	R5F101PF	–
64 KB	4 KB	4 KB Note	R5F100EE	R5F100FE	R5F100GE	R5F100JE	R5F100LE	–	–	–
	–		R5F101EE	R5F101FE	R5F101GE	R5F101JE	R5F101LE	–	–	–
48 KB	4 KB	3 KB Note	R5F100ED	R5F100FD	R5F100GD	R5F100JD	R5F100LD	–	–	–
	–		R5F101ED	R5F101FD	R5F101GD	R5F101JD	R5F101LD	–	–	–
32 KB	4 KB	2 KB	R5F100EC	R5F100FC	R5F100GC	R5F100JC	R5F100LC	–	–	–
	–		R5F101EC	R5F101FC	R5F101GC	R5F101JC	R5F101LC	–	–	–
16 KB	4 KB	2 KB	R5F100EA	R5F100FA	R5F100GA	–	–	–	–	–
	–		R5F101EA	R5F101FA	R5F101GA	–	–	–	–	–

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C, E to G, J, L): Start address FF300H

R5F100xE, R5F101xE (x = 6 to 8, A to C, E to G, J, L): Start address FEF00H

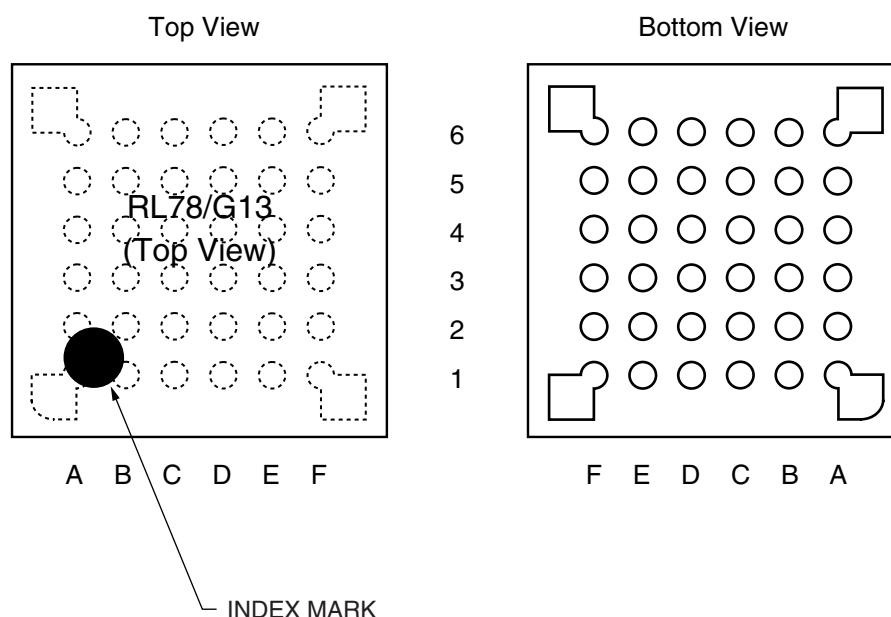
R5F100xJ, R5F101xJ (x = F, G, J, L, M, P): Start address FAF00H

R5F100xL, R5F101xL (x = F, G, J, L, M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	P60/SCLA0	V <sub>DD</sub>	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V <sub>SS</sub>	REGC	RESET	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV <sub>REFP</sub>	P21/ANI1/ AV <sub>REFM</sub>	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

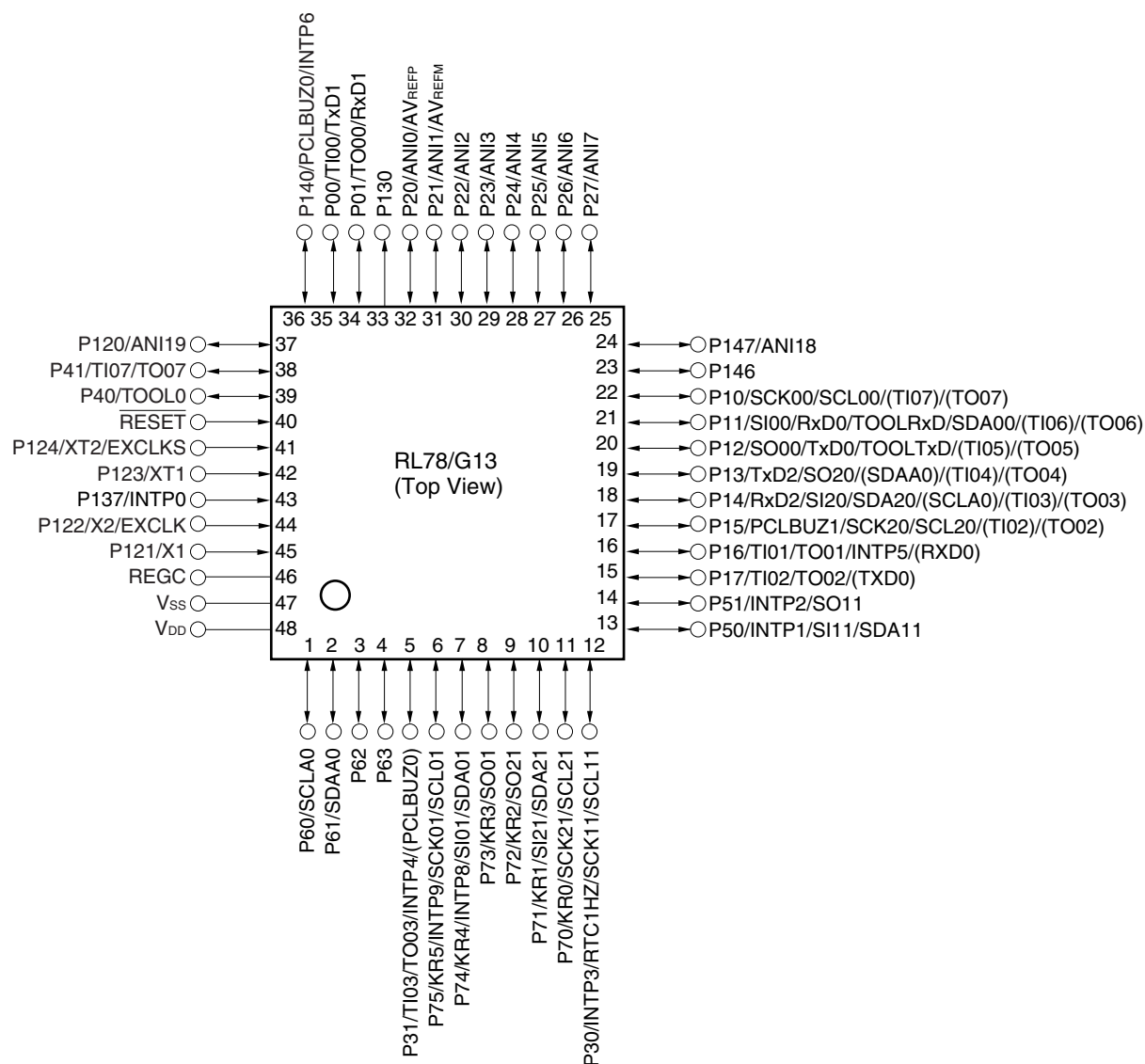
**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.3.9 48-pin products

- 48-pin plastic LQFP (7 × 7 mm, 0.5 mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F).

**Remarks 1.** For pin identification, see 1.4 Pin Identification.

- Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

**Caution** This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
		R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)		4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)		2 to 4 <sup>Note1</sup>		2 to 4 <sup>Note1</sup>		2 to 4 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>		2 to 12 <sup>Note1</sup>	
Address space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V <sub>DD</sub> = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V <sub>DD</sub> = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V <sub>DD</sub> = 1.6 to 5.5 V)											
Subsystem clock		–											
Low-speed on-chip oscillator		15 kHz (TYP.)											
General-purpose registers		(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f <sub>IH</sub> = 32 MHz operation)											
		0.05 μs (High-speed system clock: f <sub>MX</sub> = 20 MHz operation)											
Instruction set		<ul style="list-style-type: none"><li>• Data transfer (8/16 bits)</li><li>• Adder and subtractor/logical operation (8/16 bits)</li><li>• Multiplication (8 bits × 8 bits)</li><li>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.</li></ul>											
I/O port	Total	16	20	21	26	28	32						
	CMOS I/O	13 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 5)	15 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 6)	15 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 6)	21 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 9)	22 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 9)	26 (N-ch O.D. I/O [V <sub>DD</sub> withstand voltage]: 10)						
	CMOS input	3	3	3	3	3	3						
	CMOS output	–	–	1	–	–	–						
	N-ch O.D. I/O (withstand voltage: 6 V)	–	2	2	2	3	3						
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel <sup>Note 2</sup>											
	12-bit interval timer (IT)	1 channel											
	Timer output	3 channels (PWM outputs: 2 <sup>Note 3</sup> )	4 channels (PWM outputs: 3 <sup>Note 3</sup> )				4 channels (PWM outputs: 3 <sup>Note 3</sup> ), 8 channels (PWM outputs: 7 <sup>Note 3</sup> ) <sup>Note 4</sup>						
	RTC output	–											

- Notes**
- The flash library uses RAM in self-programming and rewriting of the data flash memory. The target products and start address of the RAM areas used by the flash library are shown below.  
R5F100xD, R5F101xD (x = 6 to 8, A to C): Start address FF300H  
R5F100xE, R5F101xE (x = 6 to 8, A to C): Start address FEF00H  
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.
  - Only the constant-period interrupt function when the low-speed on-chip oscillator clock (f<sub>IL</sub>) is selected

- The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).
- When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Lx	R5F101Lx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		<ul style="list-style-type: none"><li>2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f<sub>MAIN</sub> = 20 MHz operation)</li><li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f<sub>SUB</sub> = 32.768 kHz operation)</li></ul>									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] <ul style="list-style-type: none"><li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li><li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li></ul> [48-pin, 52-pin products] <ul style="list-style-type: none"><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 1 channel/simplified I<sup>2</sup>C: 1 channel/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li></ul> [64-pin products] <ul style="list-style-type: none"><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART: 1 channel</li><li>CSI: 2 channels/simplified I<sup>2</sup>C: 2 channels/UART (UART supporting LIN-bus): 1 channel</li></ul>									
		I <sup>2</sup> C bus	1 channel		1 channel		1 channel		1 channel		1 channel
Multiplier and divider/multiply-accumulator		<ul style="list-style-type: none"><li>16 bits × 16 bits = 32 bits (Unsigned or signed)</li><li>32 bits ÷ 32 bits = 32 bits (Unsigned)</li><li>16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)</li></ul>									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		<ul style="list-style-type: none"><li>Reset by <math>\overline{\text{RESET}}</math> pin</li><li>Internal reset by watchdog timer</li><li>Internal reset by power-on-reset</li><li>Internal reset by voltage detector</li><li>Internal reset by illegal instruction execution <sup>Note</sup></li><li>Internal reset by RAM parity error</li><li>Internal reset by illegal-memory access</li></ul>									
Power-on-reset circuit		<ul style="list-style-type: none"><li>Power-on-reset: 1.51 V (TYP.)</li><li>Power-down-reset: 1.50 V (TYP.)</li></ul>									
Voltage detector		<ul style="list-style-type: none"><li>Rising edge : 1.67 V to 4.06 V (14 stages)</li><li>Falling edge : 1.63 V to 3.98 V (14 stages)</li></ul>									
On-chip debug function		Provided									
Power supply voltage		V <sub>DD</sub> = 1.6 to 5.5 V (T <sub>A</sub> = -40 to +85°C) V <sub>DD</sub> = 2.4 to 5.5 V (T <sub>A</sub> = -40 to +105°C)									
Operating ambient temperature		T <sub>A</sub> = 40 to +85°C (A: Consumer applications, D: Industrial applications) T <sub>A</sub> = 40 to +105°C (G: Industrial applications)									

**Note** The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

&lt;R&gt;

## 2.3 DC Characteristics

## 2.3.1 Pin characteristics

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high <sup>Note 1</sup>	I <sub>OH1</sub>	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-10.0 <sup>Note 2</sup>	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-55.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-10.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		-5.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% <sup>Note 3</sup> )	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-80.0	mA
			2.7 V ≤ EV <sub>DD0</sub> < 4.0 V		-19.0	mA
			1.8 V ≤ EV <sub>DD0</sub> < 2.7 V		-10.0	mA
			1.6 V ≤ EV <sub>DD0</sub> < 1.8 V		-5.0	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ EV <sub>DD0</sub> ≤ 5.5 V		-135.0 <sup>Note 4</sup>	mA
	I <sub>OH2</sub>	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		-0.1 <sup>Note 2</sup>	mA
		Total of all pins (When duty ≤ 70% <sup>Note 3</sup> )	1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V		-1.5	mA

**Notes** 1. Value of current at which the device operation is guaranteed even if the current flows from the EV<sub>DD0</sub>, EV<sub>DD1</sub>, V<sub>DD</sub> pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I<sub>OH</sub> × 0.7)/(n × 0.01)

<Example> Where n = 80% and I<sub>OH</sub> = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \cong -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is -100 mA.

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products****(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V) (2/2)**

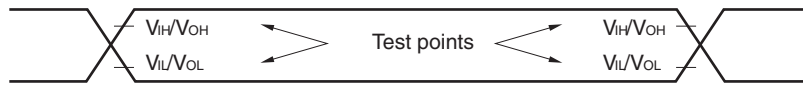
Parameter	Symbol				Conditions	MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I <sub>DD2</sub> Note 2	HALT mode	HS (high-speed main) mode Note 7	f <sub>IH</sub> = 32 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.62	1.89	mA	
					V <sub>DD</sub> = 3.0 V		0.62	1.89	mA	
				f <sub>IH</sub> = 24 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.50	1.48	mA	
					V <sub>DD</sub> = 3.0 V		0.50	1.48	mA	
				f <sub>IH</sub> = 16 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 5.0 V		0.44	1.12	mA	
					V <sub>DD</sub> = 3.0 V		0.44	1.12	mA	
			LS (low-speed main) mode Note 7	f <sub>IH</sub> = 8 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		290	620	μA	
					V <sub>DD</sub> = 2.0 V		290	620	μA	
			LV (low-voltage main) mode Note 7	f <sub>IH</sub> = 4 MHz <sup>Note 4</sup>	V <sub>DD</sub> = 3.0 V		460	700	μA	
					V <sub>DD</sub> = 2.0 V		460	700	μA	
			HS (high-speed main) mode Note 7	f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f <sub>MX</sub> = 20 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.31	1.14	mA	
					Resonator connection		0.48	1.34	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 5.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
				f <sub>MX</sub> = 10 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		0.21	0.68	mA	
					Resonator connection		0.28	0.76	mA	
			LS (low-speed main) mode Note 7	f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 3.0 V	Square wave input		110	390	μA	
					Resonator connection		160	450	μA	
				f <sub>MX</sub> = 8 MHz <sup>Note 3</sup> , V <sub>DD</sub> = 2.0 V	Square wave input		110	390	μA	
					Resonator connection		160	450	μA	
			Subsystem clock operation	f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = −40°C	Square wave input		0.31	0.66	μA	
					Resonator connection		0.50	0.85	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +25°C	Square wave input		0.38	0.66	μA	
					Resonator connection		0.57	0.85	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +50°C	Square wave input		0.47	3.49	μA	
					Resonator connection		0.66	3.68	μA	
				f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +70°C	Square wave input		0.80	6.10	μA	
					Resonator connection		0.99	6.29	μA	
			f <sub>SUB</sub> = 32.768 kHz <sup>Note 5</sup> T <sub>A</sub> = +85°C	Square wave input		1.52	10.46	μA		
				Resonator connection		1.71	10.65	μA		
	I <sub>DD3</sub> <sup>Note 6</sup>	STOP mode <sup>Note 8</sup>	T <sub>A</sub> = −40°C					0.19	0.54	μA
			T <sub>A</sub> = +25°C					0.26	0.54	μA
			T <sub>A</sub> = +50°C					0.35	3.37	μA
			T <sub>A</sub> = +70°C					0.68	5.98	μA
			T <sub>A</sub> = +85°C					1.40	10.34	μA

(Notes and Remarks are listed on the next page.)



## 2.5 Peripheral Functions Characteristics

### AC Timing Test Points



### 2.5.1 Serial array unit

#### (1) During communication at same potential (UART mode)

(T<sub>A</sub> = -40 to +85°C, 1.6 V ≤ E<sub>VDD0</sub> = E<sub>VDD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = E<sub>VSS0</sub> = E<sub>VSS1</sub> = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate <sup>Note 1</sup>		2.4 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		f <sub>MCK</sub> /6 <sup>Note 2</sup>		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 3</sup>		5.3		1.3		0.6	Mbps
		1.8 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		f <sub>MCK</sub> /6 <sup>Note 2</sup>		f <sub>MCK</sub> /6		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 3</sup>		5.3		1.3		0.6	Mbps
		1.7 V ≤ E <sub>VDD0</sub> ≤ 5.5 V		f <sub>MCK</sub> /6 <sup>Note 2</sup>		f <sub>MCK</sub> /6 <sup>Note 2</sup>		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 3</sup>		5.3		1.3		0.6	Mbps
		1.6 V ≤ E <sub>VDD0</sub> ≤ 5.5 V	—			f <sub>MCK</sub> /6 <sup>Note 2</sup>		f <sub>MCK</sub> /6	bps
		Theoretical value of the maximum transfer rate f <sub>MCK</sub> = f <sub>CLK</sub> <sup>Note 3</sup>	—			1.3		0.6	Mbps

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

**2.** The following conditions are required for low voltage interface when E<sub>VDD0</sub> < V<sub>DD</sub>.

2.4 V ≤ E<sub>VDD0</sub> < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ E<sub>VDD0</sub> < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ E<sub>VDD0</sub> < 1.8 V : MAX. 0.6 Mbps

**3.** The maximum operating frequencies of the CPU/peripheral hardware clock (f<sub>CLK</sub>) are:

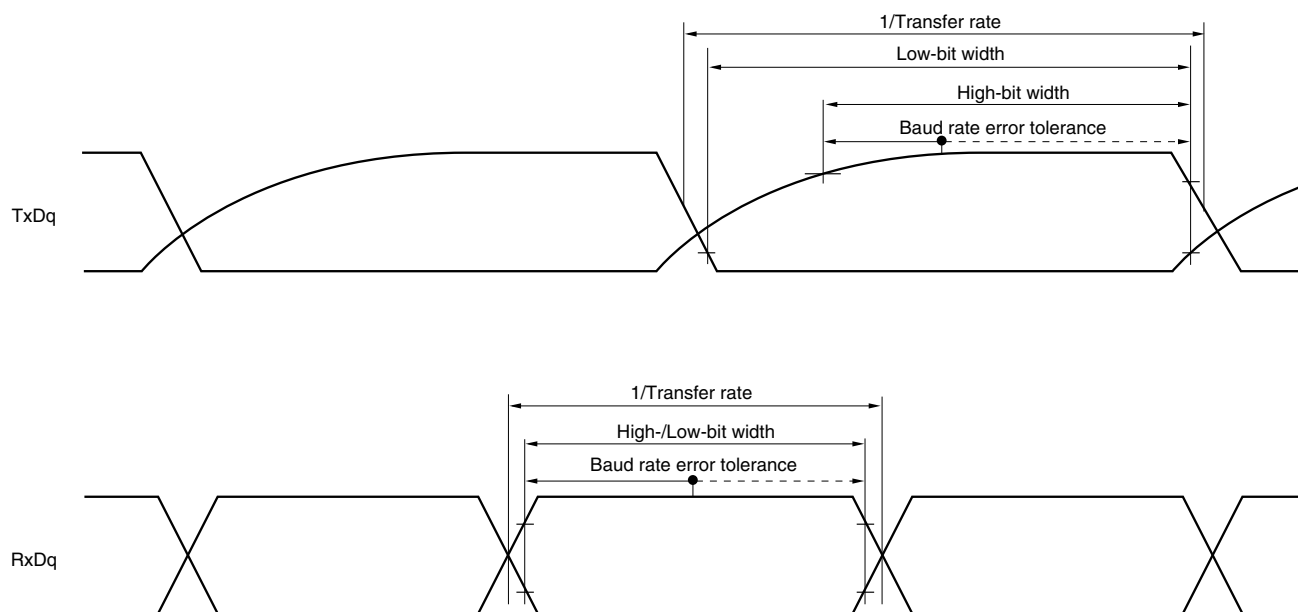
HS (high-speed main) mode: 32 MHz (2.7 V ≤ V<sub>DD</sub> ≤ 5.5 V)

16 MHz (2.4 V ≤ V<sub>DD</sub> ≤ 5.5 V)

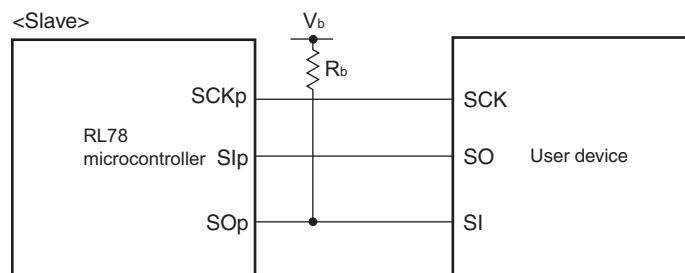
LS (low-speed main) mode: 8 MHz (1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V)

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**UART mode bit width (during communication at different potential) (reference)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  
 $C_b[\text{F}]$ : Communication line (TxDq) load capacitance,  $V_b[\text{V}]$ : Communication line voltage
  2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
  3.  $f_{\text{MCK}}$ : Serial array unit operation clock frequency  
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
  4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage
  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKS<sub>mn</sub> bit of serial mode register mn (SMR<sub>mn</sub>).  
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I<sup>2</sup>C mode) (2/2)****(T<sub>A</sub> = -40 to +85°C, 1.8 V ≤ EV<sub>DD0</sub> = EV<sub>DD1</sub> ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = EV<sub>SS0</sub> = EV<sub>SS1</sub> = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t <sub>SU:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 135 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		1/f <sub>MCK</sub> + 190 <sup>Note 3</sup>		kHz
Data hold time (transmission)	t <sub>HD:DAT</sub>	4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV <sub>DD0</sub> ≤ 5.5 V, 2.7 V ≤ V <sub>b</sub> ≤ 4.0 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV <sub>DD0</sub> < 4.0 V, 2.3 V ≤ V <sub>b</sub> ≤ 2.7 V, C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV <sub>DD0</sub> < 3.3 V, 1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> , C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ	0	405	0	405	0	405	ns

**Notes** 1. The value must also be equal to or less than f<sub>MCK</sub>/4.2. Use it with EV<sub>DD0</sub> ≥ V<sub>b</sub>.3. Set the f<sub>MCK</sub> value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution** Select the TTL input buffer and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V<sub>DD</sub> tolerance (for the 20- to 52-pin products)/EV<sub>DD</sub> tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

&lt;R&gt;

- Notes**
1. The first clock pulse is generated after this period when the start/restart condition is detected.
  2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ

**( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$ ) (4/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	$\text{V}_{\text{OH1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -3.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.7$		V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -2.0\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.6$		V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH1}} = -1.5\text{ mA}$	$\text{EV}_{\text{DD0}} - 0.5$		V
	$\text{V}_{\text{OH2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OH2}} = -100\text{ }\mu\text{A}$	$\text{V}_{\text{DD}} - 0.5$		V
Output voltage, low	$\text{V}_{\text{OL1}}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 8.5\text{ mA}$		0.7	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 3.0\text{ mA}$		0.6	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 1.5\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL1}} = 0.6\text{ mA}$		0.4	V
	$\text{V}_{\text{OL2}}$	P20 to P27, P150 to P156	$2.4\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL2}} = 400\text{ }\mu\text{A}$		0.4	V
	$\text{V}_{\text{OL3}}$	P60 to P63	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 15.0\text{ mA}$		2.0	V
			$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 5.0\text{ mA}$		0.4	V
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 3.0\text{ mA}$		0.4	V
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$ , $\text{I}_{\text{OL3}} = 2.0\text{ mA}$		0.4	V

**Caution** P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ ) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I <sub>DD1</sub>	Operating mode	HS (high-speed main) mode Note 5	$f_{\text{IH}} = 32\text{ MHz}$ Note 3	Basic operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		2.3		mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		2.3		mA
					Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		5.2	9.2	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		5.2	9.2	mA
				$f_{\text{IH}} = 24\text{ MHz}$ Note 3	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		4.1	7.0	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		4.1	7.0	mA
				$f_{\text{IH}} = 16\text{ MHz}$ Note 3	Normal operation	$\text{V}_{\text{DD}} = 5.0\text{ V}$		3.0	5.0	mA
						$\text{V}_{\text{DD}} = 3.0\text{ V}$		3.0	5.0	mA
			HS (high-speed main) mode Note 5	$f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				$f_{\text{MX}} = 20\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		3.4	5.9	mA
						Resonator connection		3.6	6.0	mA
				$f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 5.0\text{ V}$	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
				$f_{\text{MX}} = 10\text{ MHz}$ Note 2, $\text{V}_{\text{DD}} = 3.0\text{ V}$	Normal operation	Square wave input		2.1	3.5	mA
						Resonator connection		2.1	3.5	mA
		Subsystem clock operation		$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = -40^\circ\text{C}$	Normal operation	Square wave input		4.8	5.9	$\mu\text{A}$
						Resonator connection		4.9	6.0	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +25^\circ\text{C}$	Normal operation	Square wave input		4.9	5.9	$\mu\text{A}$
						Resonator connection		5.0	6.0	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +50^\circ\text{C}$	Normal operation	Square wave input		5.0	7.6	$\mu\text{A}$
						Resonator connection		5.1	7.7	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +70^\circ\text{C}$	Normal operation	Square wave input		5.2	9.3	$\mu\text{A}$
						Resonator connection		5.3	9.4	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +85^\circ\text{C}$	Normal operation	Square wave input		5.7	13.3	$\mu\text{A}$
						Resonator connection		5.8	13.4	$\mu\text{A}$
				$f_{\text{SUB}} = 32.768\text{ kHz}$ Note 4 $T_A = +105^\circ\text{C}$	Normal operation	Square wave input		10.0	46.0	$\mu\text{A}$
						Resonator connection		10.0	46.0	$\mu\text{A}$

(Notes and Remarks are listed on the next page.)

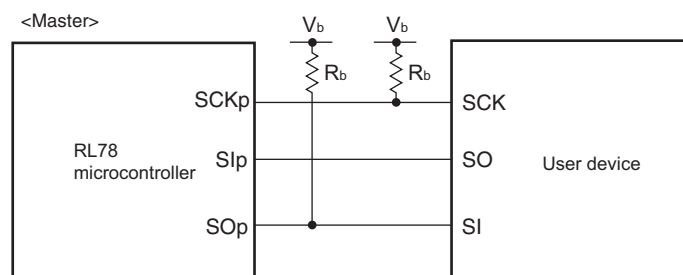
- Notes**
1. Total current flowing into  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , including the input leakage current flowing when the level of the input pin is fixed to  $V_{DD}$ ,  $EV_{DD0}$ , and  $EV_{DD1}$ , or  $V_{SS}$ ,  $EV_{SS0}$ , and  $EV_{SS1}$ . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
  2. When high-speed on-chip oscillator and subsystem clock are stopped.
  3. When high-speed system clock and subsystem clock are stopped.
  4. When high-speed on-chip oscillator and high-speed system clock are stopped. When  $AMPHS1 = 1$  (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
  5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:  $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$

$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

- Remarks**
1.  $f_{MX}$ : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
  2.  $f_{IH}$ : High-speed on-chip oscillator clock frequency
  3.  $f_{SUB}$ : Subsystem clock frequency (XT1 clock oscillation frequency)
  4. Except subsystem clock operation, temperature condition of the TYP. value is  $T_A = 25^{\circ}\text{C}$



**CSI mode connection diagram (during communication at different potential)**

- Remarks**
1.  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage
  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
  3.  $f_{MCK}$ : Serial array unit operation clock frequency  
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).  
m: Unit number, n: Channel number (mn = 00))
  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.  
Use other CSI for communication at different potential.

## 3.5.2 Serial interface IICA

(T<sub>A</sub> =  $-40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$ ,  $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$ )

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f <sub>SCL</sub>	Fast mode: f <sub>CLK</sub> ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f <sub>CLK</sub> ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t <sub>SU:STA</sub>		4.7		0.6		μs
Hold time <sup>Note 1</sup>	t <sub>HD:STA</sub>		4.0		0.6		μs
Hold time when SCLA0 = “L”	t <sub>LOW</sub>		4.7		1.3		μs
Hold time when SCLA0 = “H”	t <sub>HIGH</sub>		4.0		0.6		μs
Data setup time (reception)	t <sub>SU:DAT</sub>		250		100		ns
Data hold time (transmission) <sup>Note 2</sup>	t <sub>HD:DAT</sub>		0	3.45	0	0.9	μs
Setup time of stop condition	t <sub>SU:STO</sub>		4.0		0.6		μs
Bus-free time	t <sub>BUF</sub>		4.7		1.3		μs

**Notes** 1. The first clock pulse is generated after this period when the start/restart condition is detected.

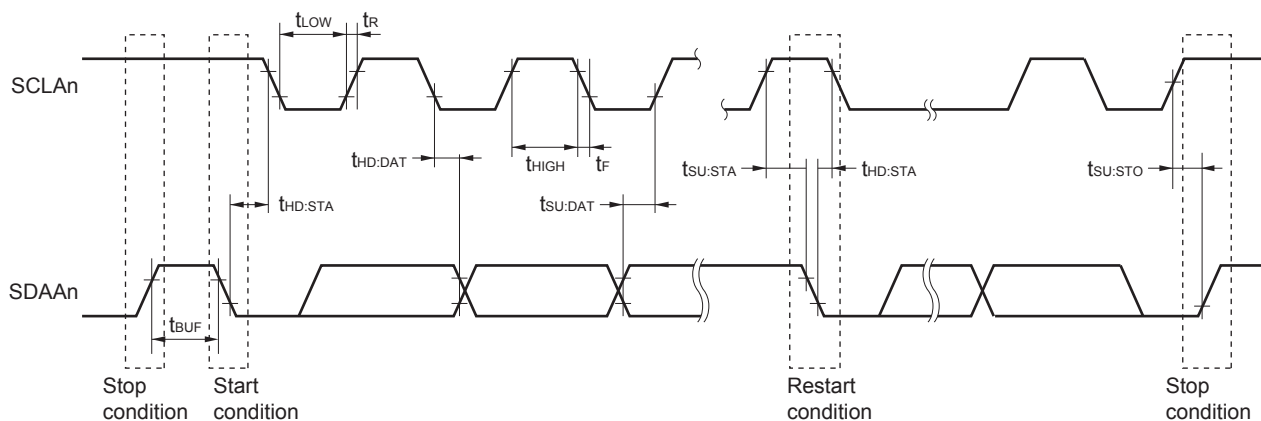
<R> 2. The maximum value (MAX.) of t<sub>HD:DAT</sub> is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

**Caution** The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of C<sub>b</sub> (communication line capacitance) and the value of R<sub>b</sub> (communication line pull-up resistor) at that time in each mode are as follows.

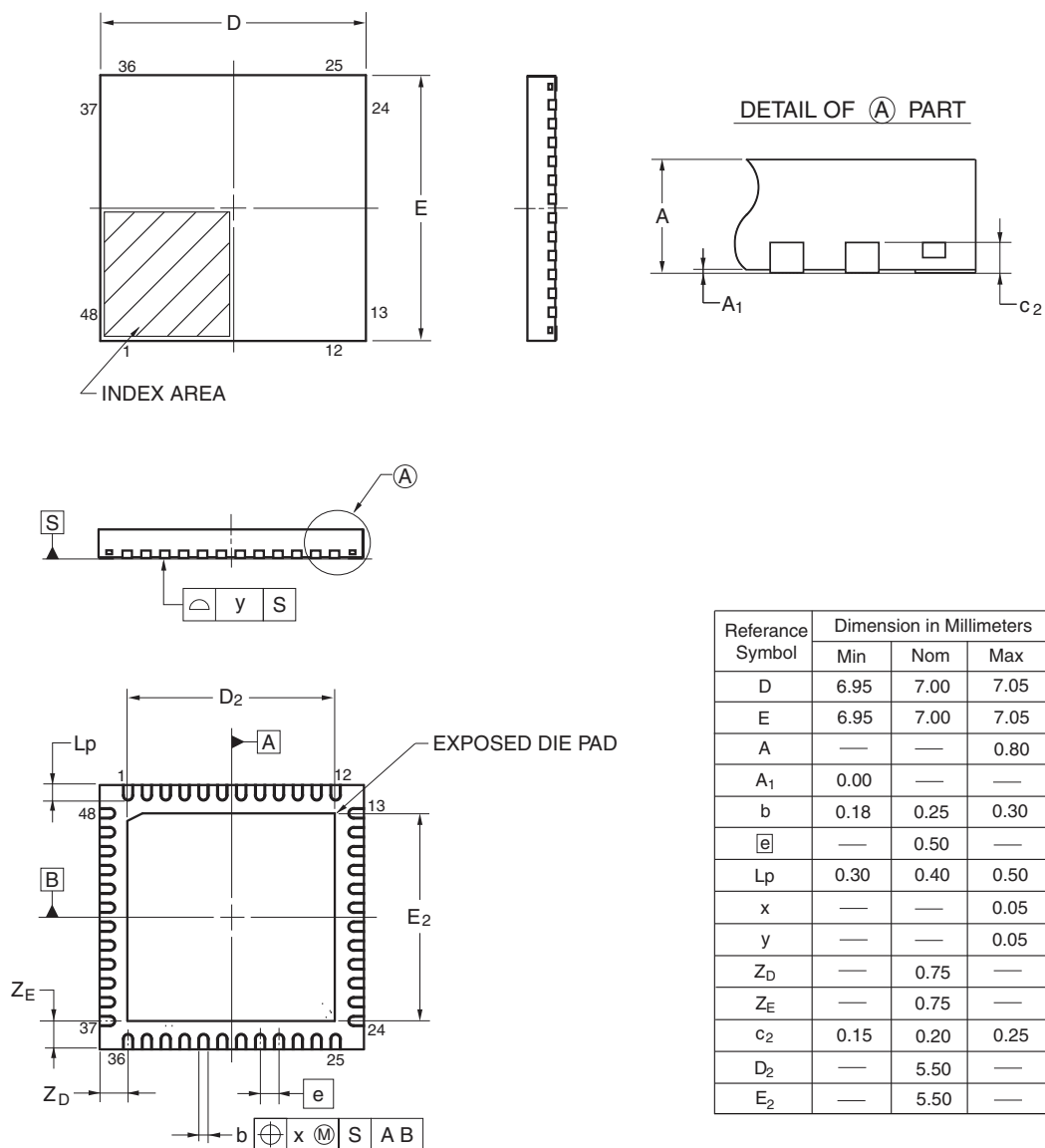
Standard mode: C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩFast mode: C<sub>b</sub> = 320 pF, R<sub>b</sub> = 1.1 kΩ

IICA serial transfer timing

**Remark** n = 0, 1

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,  
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA  
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,  
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA  
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,  
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA  
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,  
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA  
 R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,  
 R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

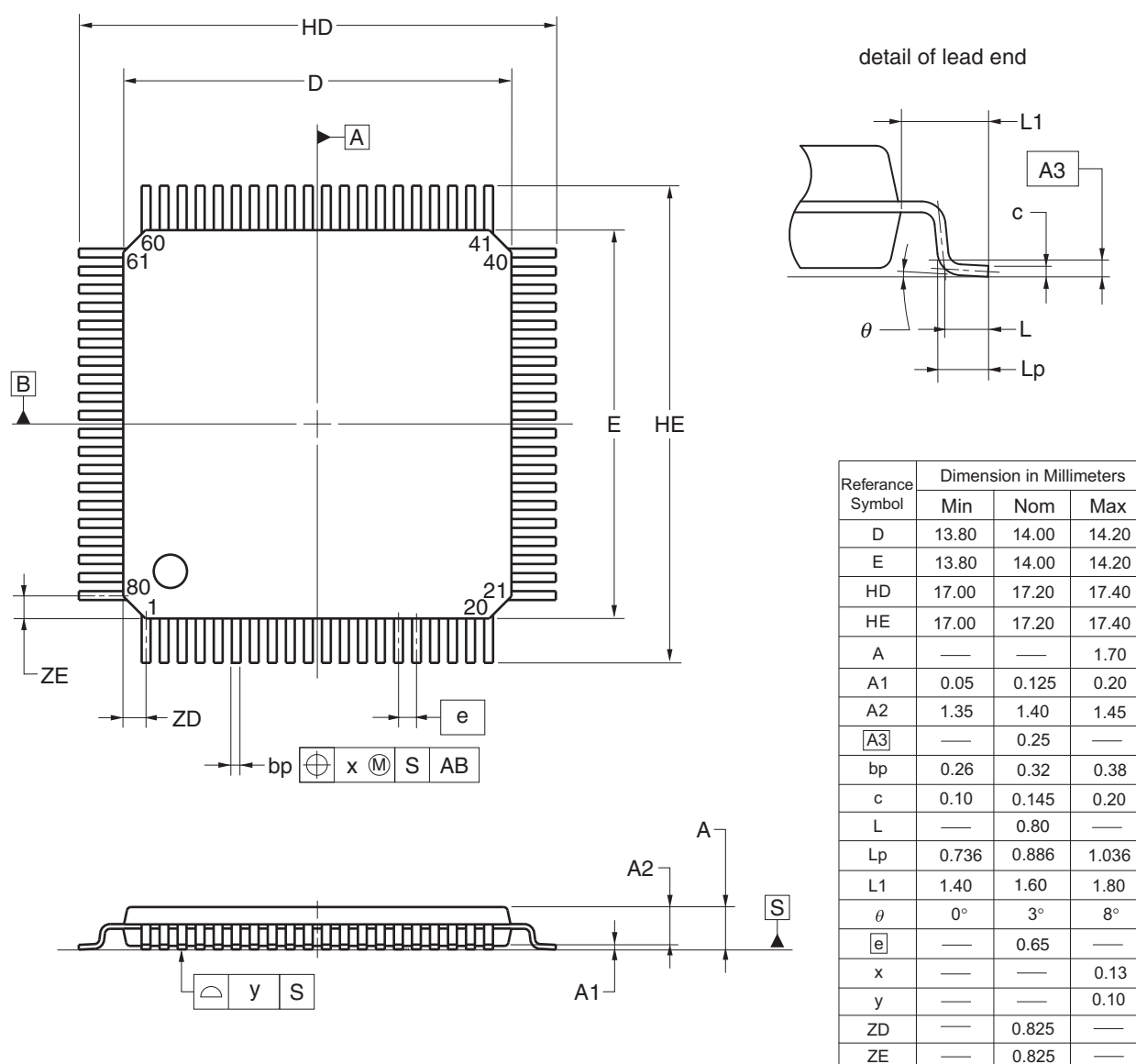


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## 4.12 80-pin Products

R5F100MFAFA, R5F100MGFAFA, R5F100MHAFA, R5F100MJFAFA, R5F100MKAFA, R5F100MLAFA  
 R5F101MFAFA, R5F101MGFAFA, R5F101MHAFA, R5F101MJFAFA, R5F101MKAFA, R5F101MLAFA  
 R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA  
 R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA  
 R5F100MFGFA, R5F100MGGFA, R5F100MHGFA, R5F100MJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



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## NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.