What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

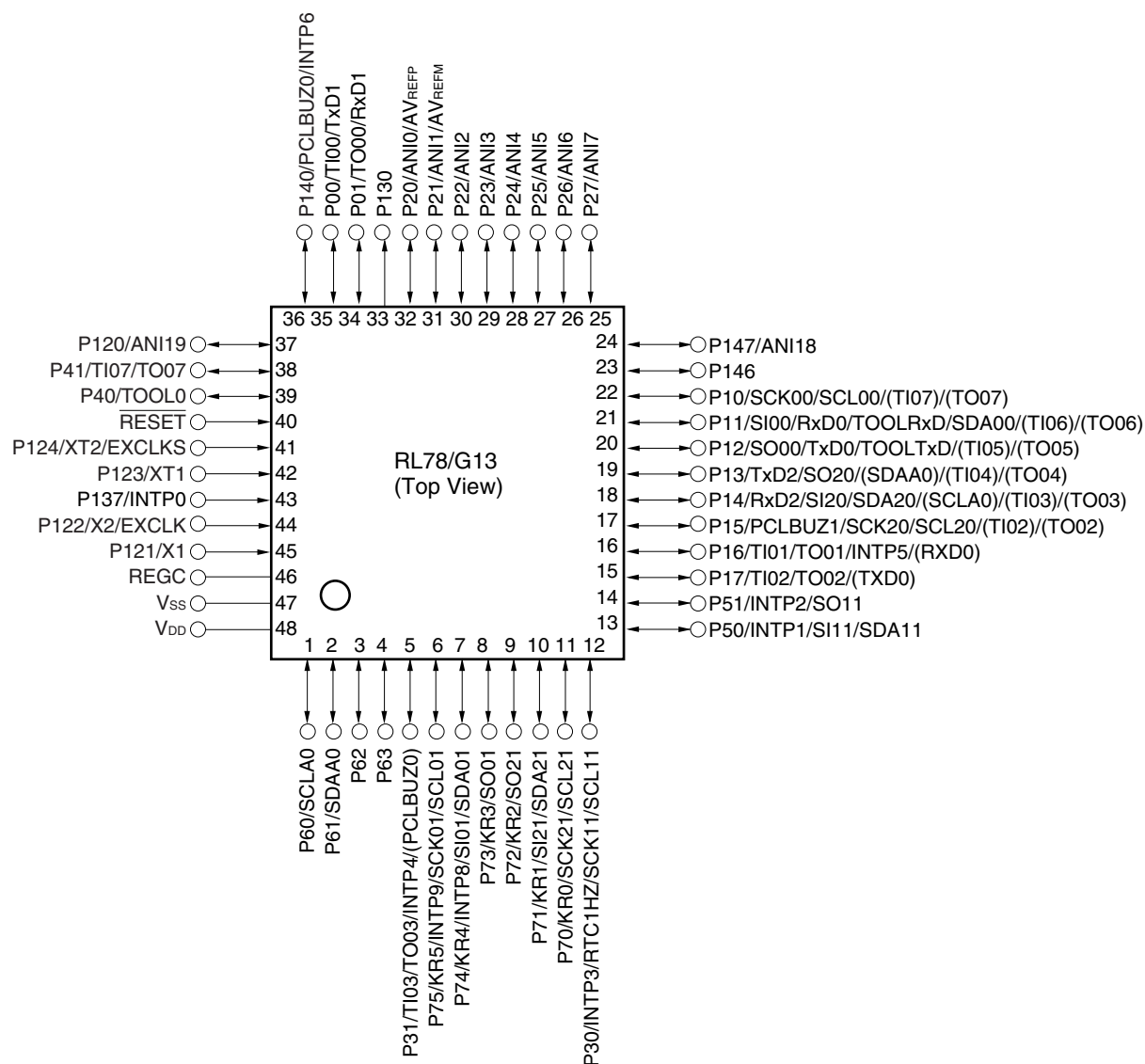| Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101fcdfp-30

Table 1-1. List of Ordering Part Numbers

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAAFB#V0, R5F100GCAFB#V0, R5F100GDAFB#V0, R5F100GEAFB#V0, R5F100GFAFB#V0, R5F100GGAFB#V0, R5F100GHAFB#V0, R5F100GJAFB#V0, R5F100GKAFB#V0, R5F100GLAFB#V0 R5F100GAAFB#X0, R5F100GCAFB#X0, R5F100GDAFB#X0, R5F100GEAFB#X0, R5F100GFAFB#X0, R5F100GGAFB#X0, R5F100GHAFB#X0, R5F100GJAFB#X0, R5F100GKAFB#X0, R5F100GLAFB#X0
			D	R5F100GADFB#V0, R5F100GCDFB#V0, R5F100GDDFB#V0, R5F100GEDFB#V0, R5F100GFDFB#V0, R5F100GGDFB#V0, R5F100GHDFB#V0, R5F100GJDFB#V0, R5F100GKDFB#V0, R5F100GLDFB#V0 R5F100GADFB#X0, R5F100GCDFB#X0, R5F100GDDFB#X0, R5F100GEDFB#X0, R5F100GFDFB#X0, R5F100GGDFB#X0, R5F100GHDFB#X0, R5F100GJDFB#X0, R5F100GKDFB#X0, R5F100GLDFB#X0
			G	R5F100GAGFB#V0, R5F100GCGFB#V0, R5F100GDGFB#V0, R5F100GEGFB#V0, R5F100GFGFB#V0, R5F100GGGFB#V0, R5F100GHGFB#V0, R5F100GJGFB#V0 R5F100GAGFB#X0, R5F100GCGFB#X0, R5F100GDGFB#X0, R5F100GEGFB#X0, R5F100GFGFB#X0, R5F100GGGFB#X0, R5F100GHGFB#X0, R5F100GJGFB#X0
		Not mounted	A	R5F101GAAFB#V0, R5F101GCAFB#V0, R5F101GDAFB#V0, R5F101GEAFB#V0, R5F101GFAFB#V0, R5F101GGAFB#V0, R5F101GHAFB#V0, R5F101GJAFB#V0, R5F101GKAFB#V0, R5F101GLAFB#V0 R5F101GAAFB#X0, R5F101GCAFB#X0, R5F101GDAFB#X0, R5F101GEAFB#X0, R5F101GFAFB#X0, R5F101GGAFB#X0, R5F101GHAFB#X0, R5F101GJAFB#X0, R5F101GKAFB#X0, R5F101GLAFB#X0
			D	R5F101GADFB#V0, R5F101GCDFB#V0, R5F101GDDFB#V0, R5F101GEDFB#V0, R5F101GFDFB#V0, R5F101GGDFB#V0, R5F101GHDFB#V0, R5F101GJDFB#V0, R5F101GKDFB#V0, R5F101GLDFB#V0 R5F101GADFB#X0, R5F101GCDFB#X0, R5F101GDDFB#X0, R5F101GEDFB#X0, R5F101GFDFB#X0, R5F101GGDFB#X0, R5F101GHDFB#X0, R5F101GJDFB#X0, R5F101GKDFB#X0, R5F101GLDFB#X0

Note　　For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.9 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)

RL78/G13
(Top View)

Top pins (36–25):
P140/PCLBUZ0/INTP6, P00/TI00/TxD1, P01/TO00/RxD1, P130, P20/ANI0/AV$_{REFP}$, P21/ANI1/AV$_{REFM}$, P22/ANI2, P23/ANI3, P24/ANI4, P25/ANI5, P26/ANI6, P27/ANI7

Left pins (37–48):
- 37 P120/ANI19
- 38 P41/TI07/TO07
- 39 P40/TOOL0
- 40 $\overline{\text{RESET}}$
- 41 P124/XT2/EXCLKS
- 42 P123/XT1
- 43 P137/INTP0
- 44 P122/X2/EXCLK
- 45 P121/X1
- 46 REGC
- 47 V$_{SS}$
- 48 V$_{DD}$

Right pins (24–13):
- 24 P147/ANI18
- 23 P146
- 22 P10/SCK00/SCL00/(TI07)/(TO07)
- 21 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 20 P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)
- 19 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 18 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 17 P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)
- 16 P16/TI01/TO01/INTP5/(RXD0)
- 15 P17/TI02/TO02/(TXD0)
- 14 P51/INTP2/SO11
- 13 P50/INTP1/SI11/SDA11

Bottom pins (1–12):
P60/SCLA0, P61/SDAA0, P62, P63, P31/TI03/TO03/INTP4/(PCLBUZ0), P75/KR5/INTP9/SCK01/SCL01, P74/KR4/INTP8/SI01/SDA01, P73/KR3/SO01, P72/KR2/SO21, P71/KR1/SI21/SDA21, P70/KR0/SCK21/SCL21, P30/INTP3/RTC1HZ/SCK11/SCL11

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
   2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.14 128-pin products

- 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)
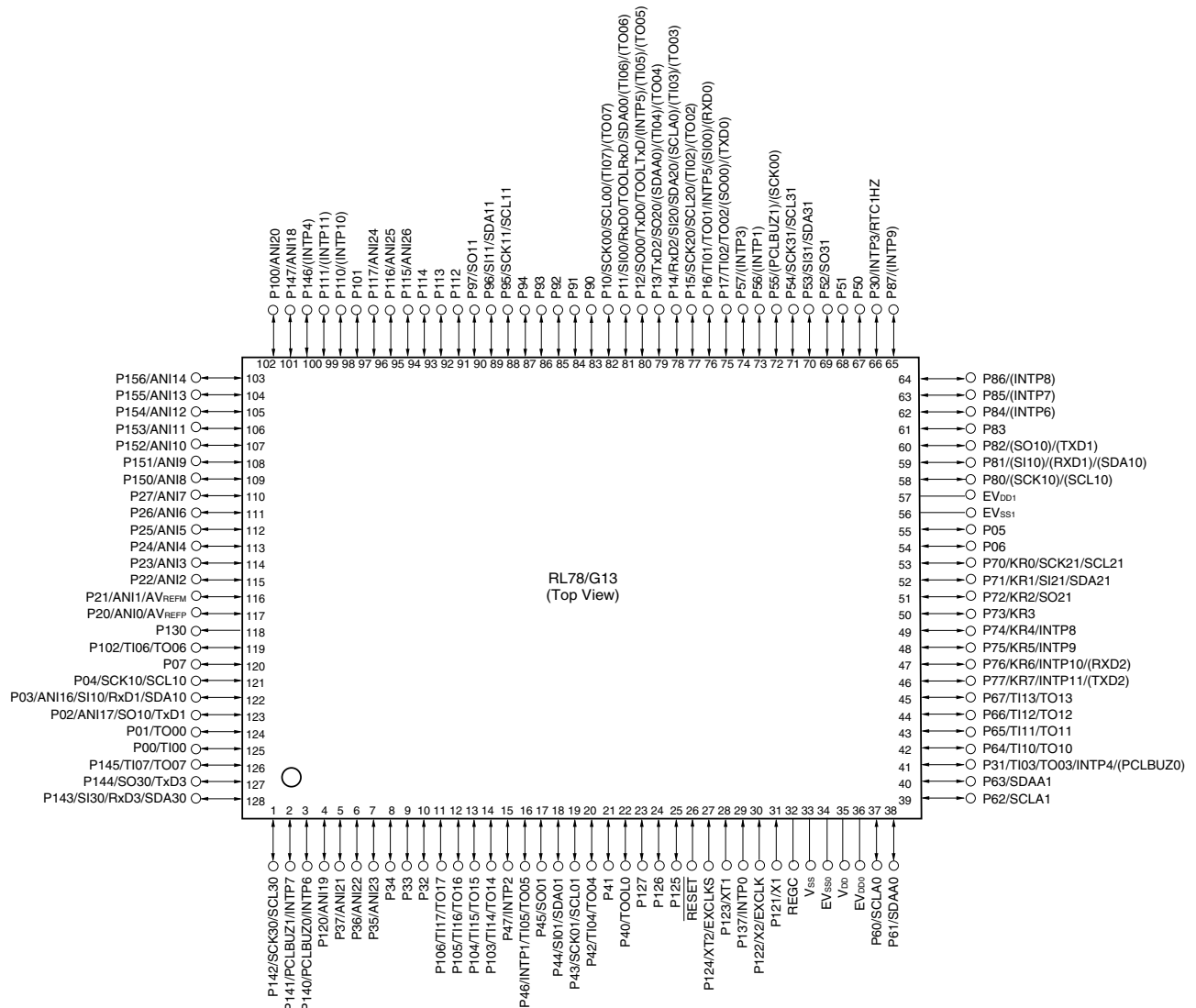
Cautions 1. Make EVss0, EVss1 pins the same potential as Vss pin.

      2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

      3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

      2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.

      3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.11 64-pin products
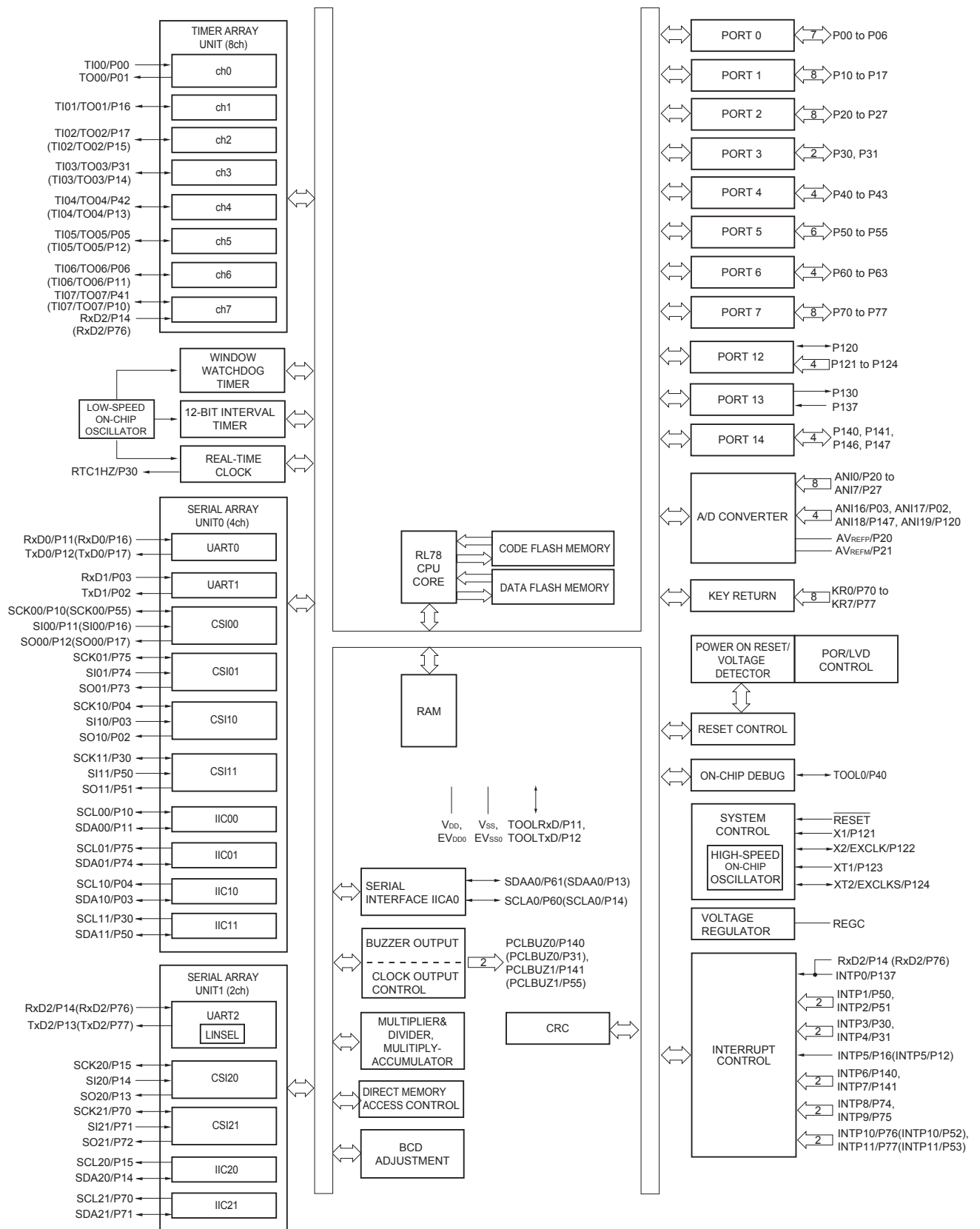
Remark Functions in the parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

3. When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
	I²C bus	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access									
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)									
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)									
<R> Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)									

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (high-speed main) mode [Note 5]	f$_{IH}$ = 32 MHz [Note 3]	Basic operation	V$_{DD}$ = 5.0 V		2.3		mA
						V$_{DD}$ = 3.0 V		2.3		mA
					Normal operation	V$_{DD}$ = 5.0 V		5.2	8.5	mA
						V$_{DD}$ = 3.0 V		5.2	8.5	mA
				f$_{IH}$ = 24 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		4.1	6.6	mA
						V$_{DD}$ = 3.0 V		4.1	6.6	mA
				f$_{IH}$ = 16 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		3.0	4.7	mA
						V$_{DD}$ = 3.0 V		3.0	4.7	mA
			LS (low-speed main) mode [Note 5]	f$_{IH}$ = 8 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.3	2.1	mA
						V$_{DD}$ = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode [Note 5]	f$_{IH}$ = 4 MHz [Note 3]	Normal operation	V$_{DD}$ = 3.0 V		1.3	1.8	mA
						V$_{DD}$ = 2.0 V		1.3	1.8	mA
			HS (high-speed main) mode [Note 5]	f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA
						Resonator connection		3.6	5.7	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA
						Resonator connection		2.1	3.2	mA
			LS (low-speed main) mode [Note 5]	f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
				f$_{MX}$ = 8 MHz [Note 2], V$_{DD}$ = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA
						Resonator connection		1.2	2.0	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = −40°C	Normal operation	Square wave input		4.8	5.9	μA
						Resonator connection		4.9	6.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C	Normal operation	Square wave input		4.9	5.9	μA
						Resonator connection		5.0	6.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C	Normal operation	Square wave input		5.0	7.6	μA
						Resonator connection		5.1	7.7	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C	Normal operation	Square wave input		5.2	9.3	μA
						Resonator connection		5.3	9.4	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C	Normal operation	Square wave input		5.7	13.3	μA
						Resonator connection		5.8	13.4	μA

(**Notes** and **Remarks** are listed on the next page.)

(4) Peripheral Functions (Common to all products)

(T$_A$ = −40 to +85°C, 1.6 V $\leq$ EV$_{DD0}$ = EV$_{DD1}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$ [Note 1]				0.20		μA
RTC operating current	I$_{RTC}$ [Notes 1, 2, 3]				0.02		μA
12-bit interval timer operating current	I$_{IT}$ [Notes 1, 2, 4]				0.02		μA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 5]	f$_{IL}$ = 15 kHz			0.22		μA
A/D converter operating current	I$_{ADC}$ [Notes 1, 6]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$ [Note 1]				75.0		μA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		μA
LVD operating current	I$_{LVI}$ [Notes 1, 7]				0.08		μA
Self-programming operating current	I$_{FSP}$ [Notes 1, 9]				2.50	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 8]				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed [Note 10]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added. I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter operates in an operation mode or the HALT mode.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode.**

Remarks 1. f$_{IL}$: Low-speed on-chip oscillator clock frequency

2. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f$_{CLK}$: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T$_A$ = 25°C

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t$_{KCY1}$	t$_{KCY1}$ ≥ 4/f$_{CLK}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t$_{KH1}$, t$_{KL1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 12		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 18		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 38		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		t$_{KCY1}$/2 − 50		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY1}$/2 − 100		t$_{KCY1}$/2 − 100		ns
SIp setup time (to SCKp↑) Note 1	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		220		220		ns
SIp hold time (from SCKp↑) Note 2	t$_{KSI1}$	1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output Note 3	t$_{KSO1}$	1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V C = 30 pF Note 4			25		25		25	ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V C = 30 pF Note 4			—		25		25	ns

Notes **1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Caution   Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

3. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ EV$_{DD0}$ < 4.0 V and 2.3 V $\leq$ V$_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

5. Use it with EV$_{DD0}$ $\geq$ V$_b$.

6. The smaller maximum transfer rate derived by using f$_{MCK}$/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ EV$_{DD0}$ < 3.3 V and 1.6 V $\leq$ V$_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

UART mode connection diagram (during communication at different potential)
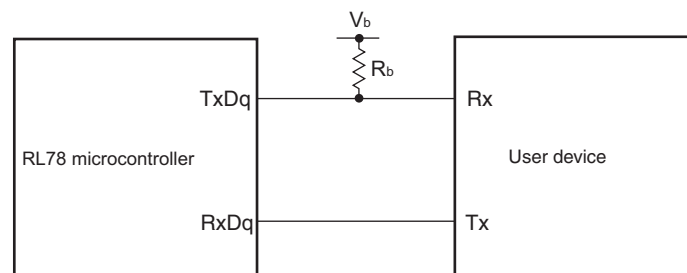
LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq V_{DD} \leq 5.5$ V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVDA0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V_{LVDA1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVDA2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVDA3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDB0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V_{LVDB1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVDB2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVDB3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVDC0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V_{LVDC1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVDC2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVDC3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V_{LVDD0}	V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V_{LVDD1}	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVDD2}	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V_{LVDD3}	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V

Caution   **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products
(T$_A$ = –40 to +105°C, 2.4 V $\leq$ EV$_{DD0}$ $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD1}$	Operating mode	HS (high-speed main) mode [Note 5]	f$_{IH}$ = 32 MHz [Note 3]	Basic operation	V$_{DD}$ = 5.0 V		2.1		mA
						V$_{DD}$ = 3.0 V		2.1		mA
					Normal operation	V$_{DD}$ = 5.0 V		4.6	7.5	mA
						V$_{DD}$ = 3.0 V		4.6	7.5	mA
				f$_{IH}$ = 24 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		3.7	5.8	mA
						V$_{DD}$ = 3.0 V		3.7	5.8	mA
				f$_{IH}$ = 16 MHz [Note 3]	Normal operation	V$_{DD}$ = 5.0 V		2.7	4.2	mA
						V$_{DD}$ = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode [Note 5]	f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = −40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +105°C	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 16 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. During HALT instruction execution by flash memory.

    3. When high-speed on-chip oscillator and subsystem clock are stopped.

    4. When high-speed system clock and subsystem clock are stopped.

    5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

    6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

    7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

        HS (high-speed main) mode: $2.7\ V \le V_{DD} \le 5.5\ V$ @ 1 MHz to 32 MHz

                                    $2.4\ V \le V_{DD} \le 5.5\ V$ @ 1 MHz to 16 MHz

    8. Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f_{IH}: High-speed on-chip oscillator clock frequency

    3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

    4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

6. Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$ or I$_{DD2}$ and I$_{ADC}$ when the A/D converter is in operation.

7. Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{LVD}$ when the LVD circuit is in operation.

8. Current flowing only during data flash rewrite.

9. Current flowing only during self programming.

10. For shift time to the SNOOZE mode, see **18.3.3 SNOOZE mode** in the RL78/G13 User's Manual.

Remarks 1. f$_{IL}$:   Low-speed on-chip oscillator clock frequency

2. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f$_{CLK}$: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T$_A$ = 25°C

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI14		0		V$_{DD}$	V
		ANI16 to ANI26		0		EV$_{DD0}$	V
		Internal reference voltage output (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 3]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 3]		V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{BGR}$ [Note 3], Reference voltage (−) = AV$_{REFM}$ [Note 4] = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	t$_{CONV}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Differential linearity error [Note 1]	DLE	8-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±1.0	LSB
Analog input voltage	V$_{AIN}$			0		V$_{BGR}$ [Note 3]	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (−) = V$_{SS}$, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (−) = AV$_{REFM}$.
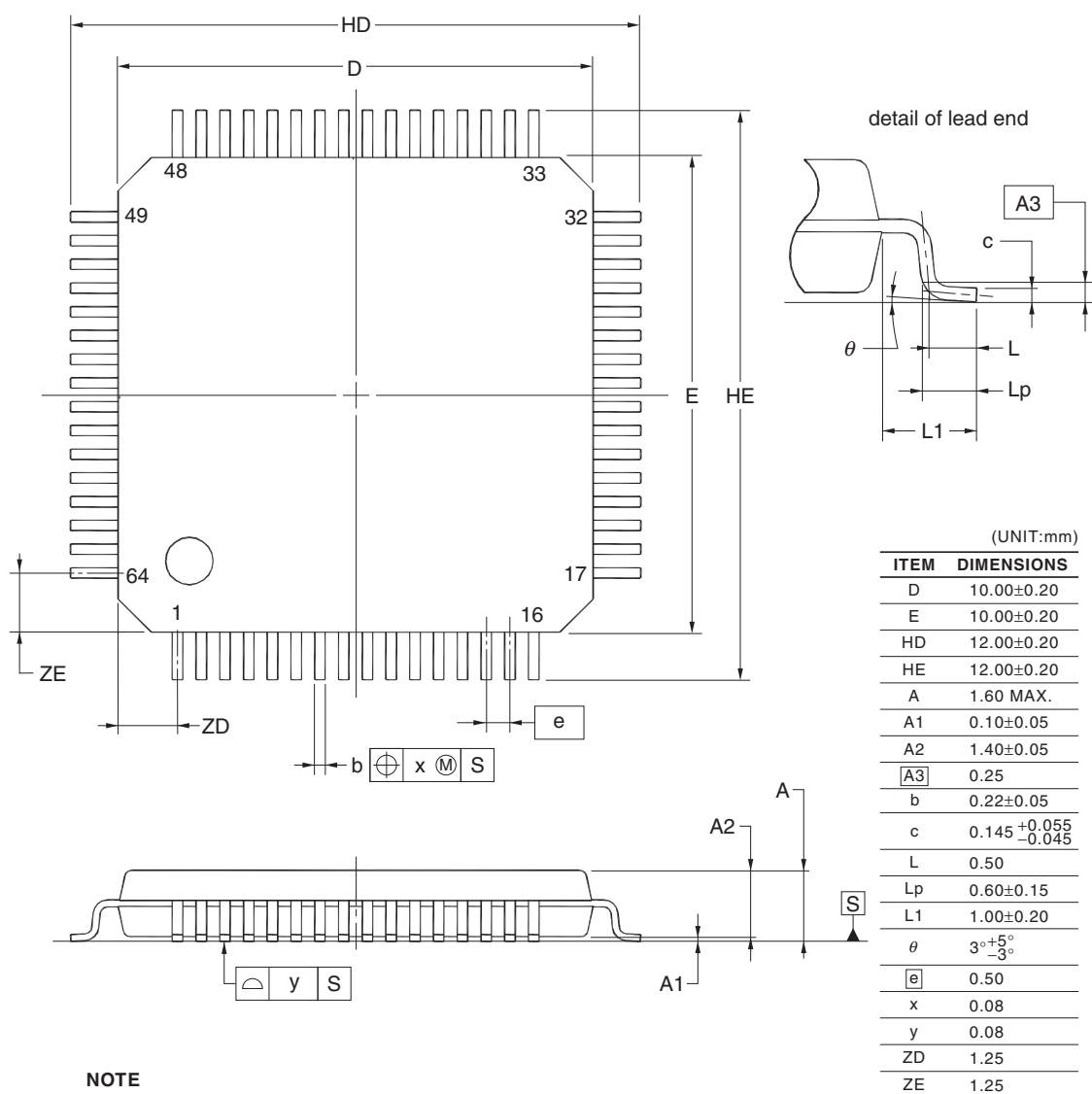
3.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB,
R5F100LKAFB, R5F100LLAFB

R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB,
R5F101LJAFB, R5F101LKAFB, R5F101LLAFB

R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB,
R5F100LKDFB, R5F100LLDFB

R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB,
R5F101LJDFB, R5F101LKDFB, R5F101LLDFB

R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB,
R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.