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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101ffafp-30

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application <small>Note</small>	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
			D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
		Not mounted	A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(7/12)

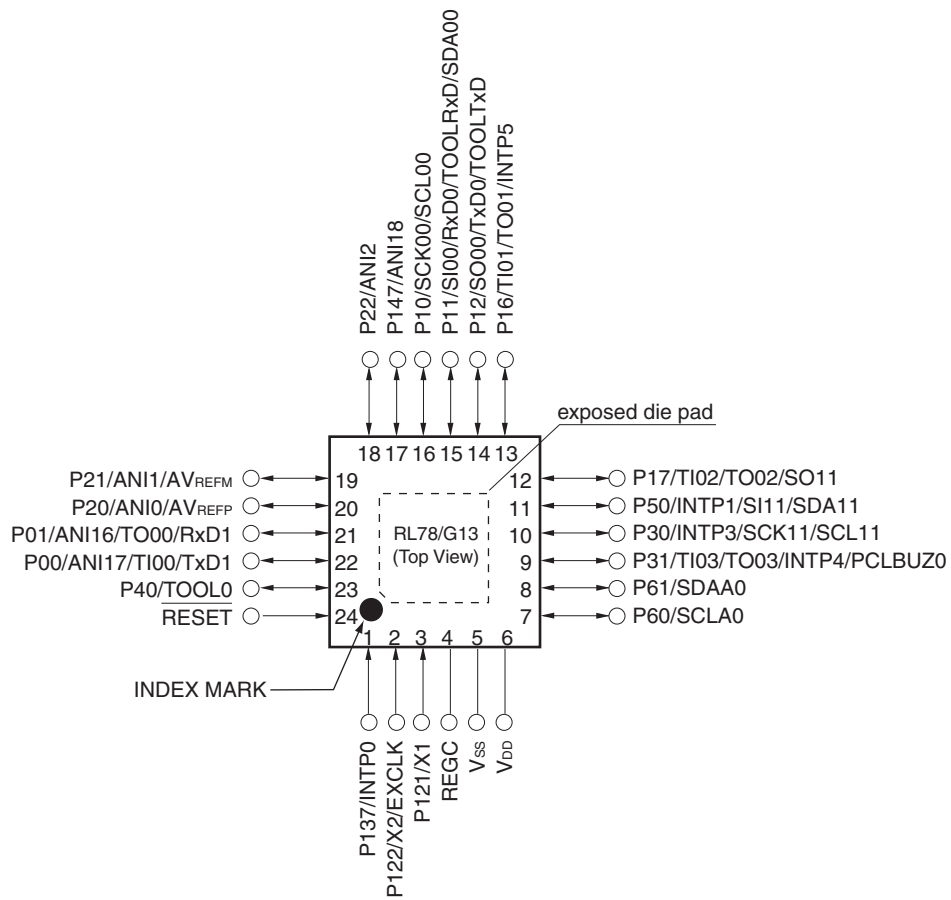
Pin count	Package	Data flash	Fields of Application <small>Note</small>	Ordering Part Number
52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	Mounted	A	R5F100JCAFA#V0, R5F100JDAFA#V0, R5F100JEAFA#V0, R5F100JFAFA#V0, R5F100JGAFA#V0, R5F100JHAFA#V0, R5F100JJAFA#V0, R5F100JKAFA#V0, R5F100JLAFA#V0 R5F100JCAFA#X0, R5F100JDAFA#X0, R5F100JEAFA#X0, R5F100JFAFA#X0, R5F100JGAFA#X0, R5F100JHAFA#X0, R5F100JJAFA#X0, R5F100JKAFA#X0, R5F100JLAFA#X0
			D	R5F100JCDFA#V0, R5F100JDDFA#V0, R5F100JEDFA#V0, R5F100JFDFA#V0, R5F100JGDFA#V0, R5F100JHDFFA#V0, R5F100JJDFA#V0, R5F100JKDFA#V0, R5F100JLDFA#V0 R5F100JCDFA#X0, R5F100JDDFA#X0, R5F100JEDFA#X0, R5F100JFDFA#X0, R5F100JGDFA#X0, R5F100JHDFFA#X0, R5F100JJDFA#X0, R5F100JKDFA#X0, R5F100JLDFA#X0
			G	R5F100JCGFA#V0, R5F100JDGFA#V0, R5F100JEGFA#V0, R5F100JFGFA#V0, R5F100JGGFA#V0, R5F100JHGFA#V0, R5F100JJGFA#V0 R5F100JCGFA#X0, R5F100JDGFA#X0, R5F100JEGFA#X0, R5F100JFGFA#X0, R5F100JGGFA#X0, R5F100JHGFA#X0, R5F100JJGFA#X0
		Not mounted	A	R5F101JCAFA#V0, R5F101JDAFA#V0, R5F101JEAFA#V0, R5F101JFAFA#V0, R5F101JGAFA#V0, R5F101JHAFA#V0, R5F101JJAFA#V0, R5F101JKAFA#V0, R5F101JLAFA#V0 R5F101JCAFA#X0, R5F101JDAFA#X0, R5F101JEAFA#X0, R5F101JFAFA#X0, R5F101JGAFA#X0, R5F101JHAFA#X0, R5F101JJAFA#X0, R5F101JKAFA#X0, R5F101JLAFA#X0
			D	R5F101JCDFA#V0, R5F101JDDFA#V0, R5F101JEDFA#V0, R5F101JFDFA#V0, R5F101JGDFA#V0, R5F101JHDFFA#V0, R5F101JJDFA#V0, R5F101JKDFA#V0, R5F101JLDFA#V0 R5F101JCDFA#X0, R5F101JDDFA#X0, R5F101JEDFA#X0, R5F101JFDFA#X0, R5F101JGDFA#X0, R5F101JHDFFA#X0, R5F101JJDFA#X0, R5F101JKDFA#X0, R5F101JLDFA#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.2 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5 mm pitch)

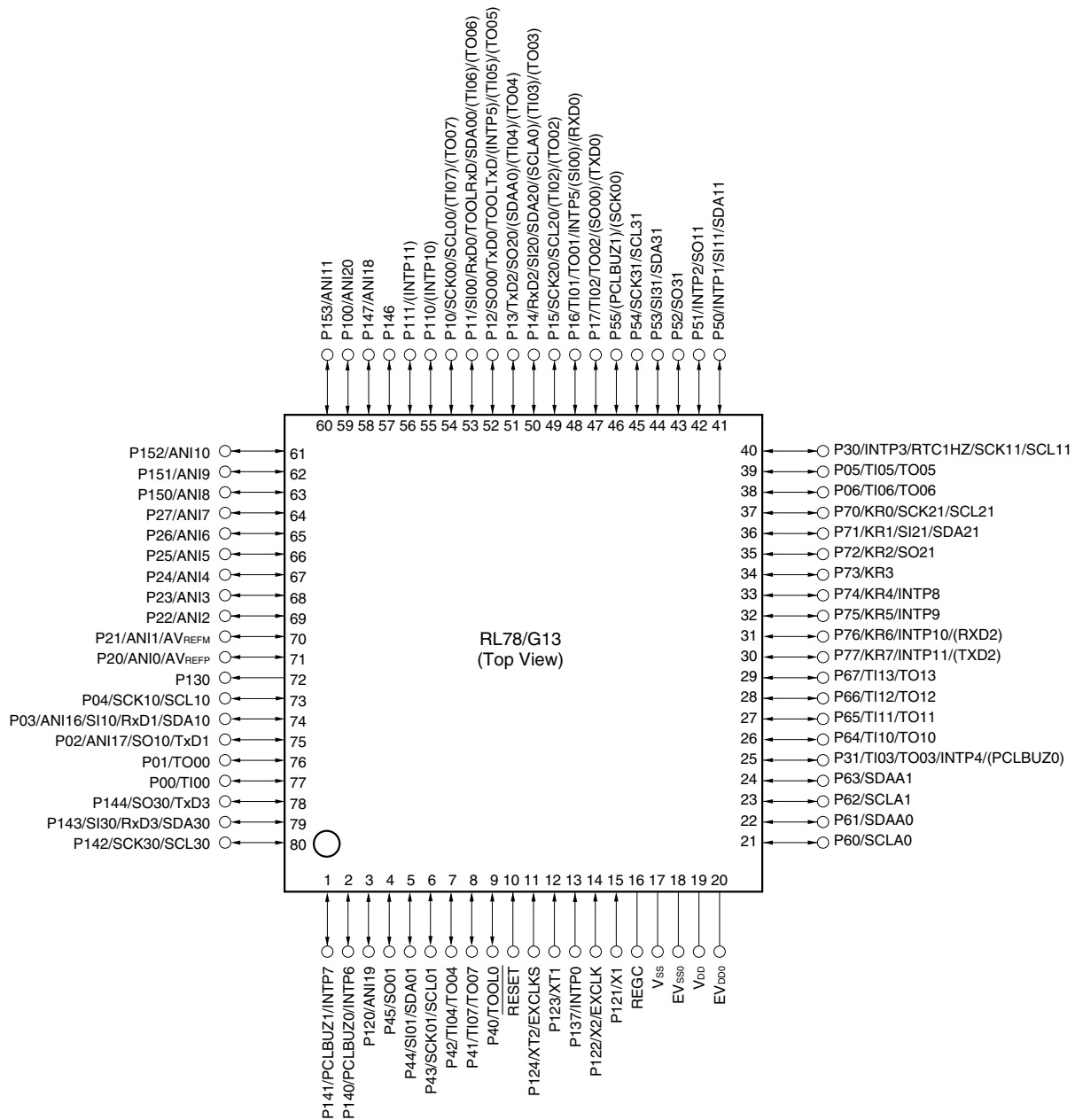


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. It is recommended to connect an exposed die pad to V_{SS}.

1.3.12 80-pin products

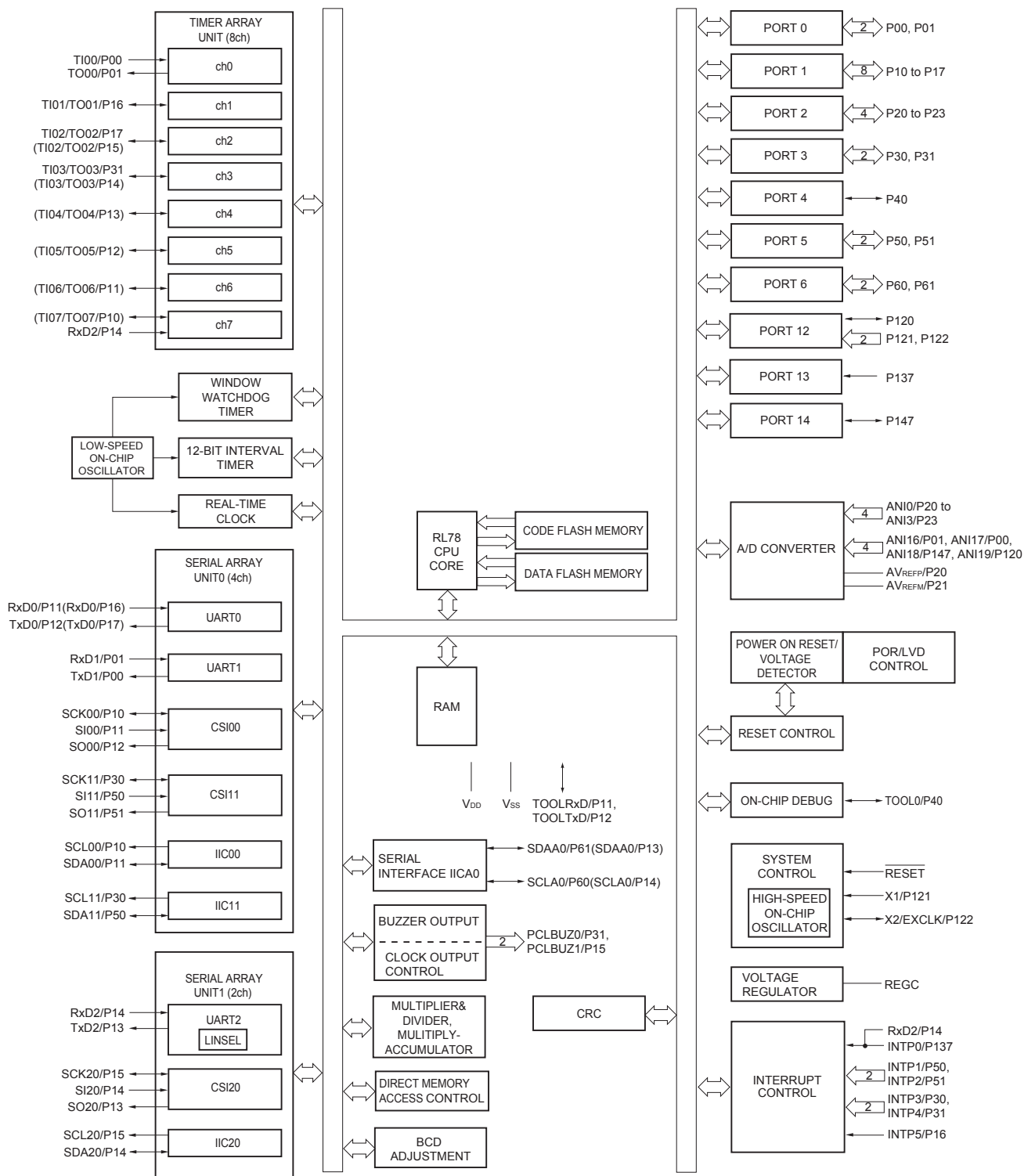
- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.4 30-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V) (3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8E _{VDD0}		E _{VDD0}	V
	V _{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ E _{VDD0} ≤ 5.5 V	2.2		E _{VDD0}	V
			TTL input buffer 3.3 V ≤ E _{VDD0} < 4.0 V	2.0		E _{VDD0}	V
			TTL input buffer 1.6 V ≤ E _{VDD0} < 3.3 V	1.5		E _{VDD0}	V
	V _{IH3}	P20 to P27, P150 to P156		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63		0.7E _{VDD0}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2E _{VDD0}	V
	V _{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ E _{VDD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ E _{VDD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ E _{VDD0} < 3.3 V	0		0.32	V
	V _{IL3}	P20 to P27, P150 to P156		0		0.3V _{DD}	V
	V _{IL4}	P60 to P63		0		0.3E _{VDD0}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V _{DD}	V

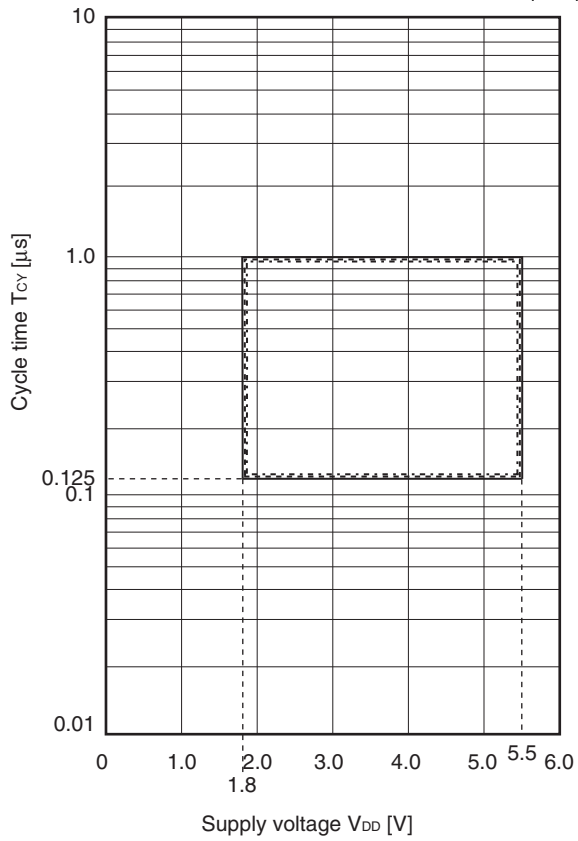
Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is E_{VDD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

- Notes**
1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 32 MHz
 - $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 16 MHz
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 8 MHz
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ @ 1 MHz to 4 MHz

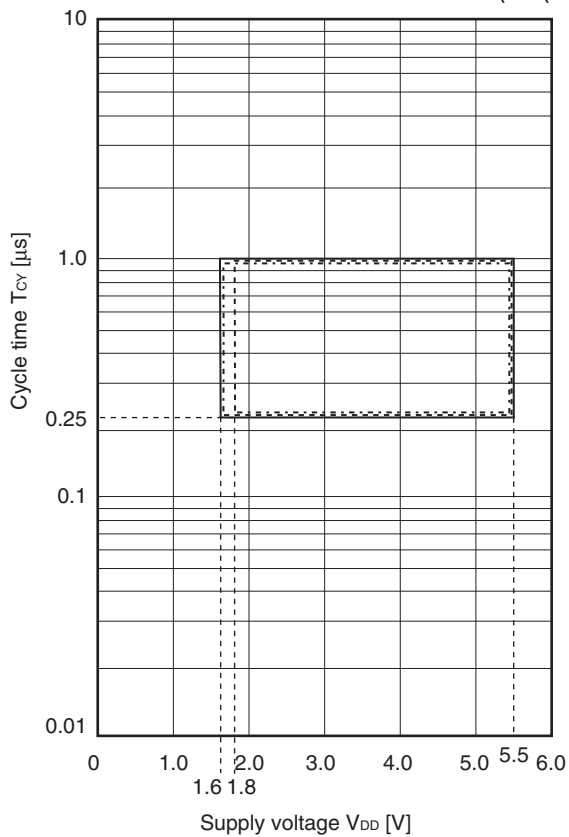
- Remarks**
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH}: High-speed on-chip oscillator clock frequency
 3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

T_{CY} vs V_{DD} (LS (low-speed main) mode)



- When the high-speed on-chip oscillator clock is selected
- - - During self programming
- · - · When high-speed system clock is selected

T_{CY} vs V_{DD} (LV (low-voltage main) mode)



- When the high-speed on-chip oscillator clock is selected
- - - During self programming
- · - · When high-speed system clock is selected

- The smaller maximum transfer rate derived by using f_{mck}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.
- Use it with EV_{DD0} ≥ V_b.
- The smaller maximum transfer rate derived by using f_{mck}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

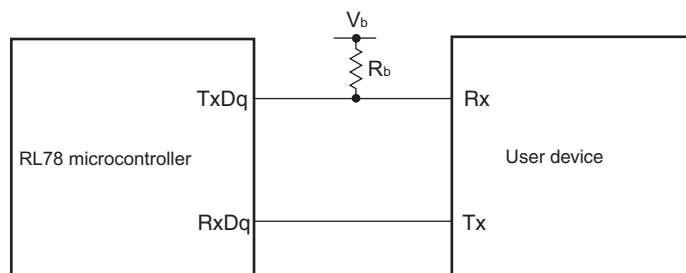
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the Rx_{Dq} pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the Tx_{Dq} pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

UART mode connection diagram (during communication at different potential)



(3) I²C fast mode plus

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz 2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.26		—	—	—	—	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	0.45	—	—	—	—	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.26		—	—	—	—	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

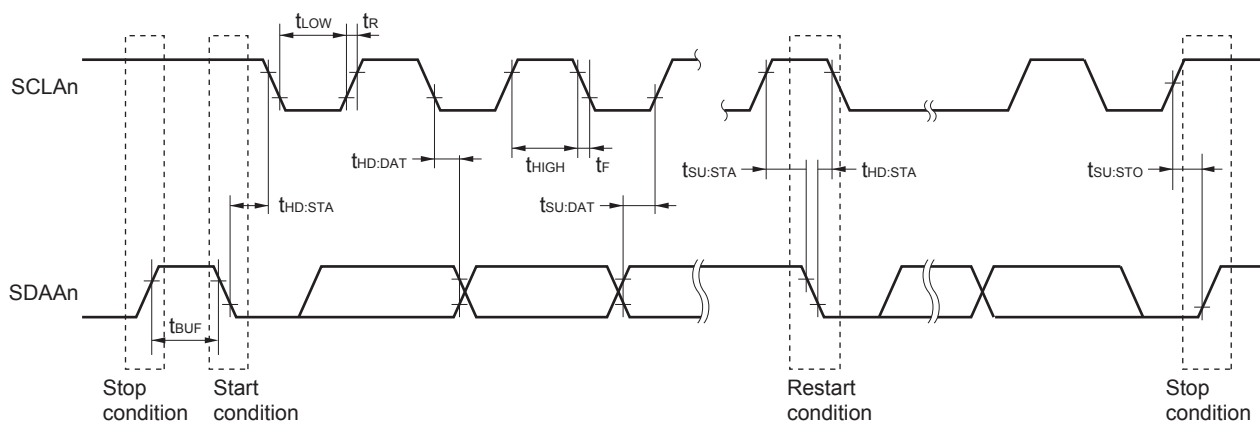
<R> 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{BGR}^{Note 3}, Reference voltage (-) = AV_{REFM} = 0 V^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±1.0	LSB
Analog input voltage	V _{AIN}			0		V _{BGR} ^{Note 3}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

4. When reference voltage (-) = V_{SS}, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AV_{REFM}.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM}.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +85°C, V_{PDR} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V		
	Power supply fall time	1.60	1.63	1.66	V		
Minimum pulse width	t _{LW}		300			μs	
Detection delay time					300	μs	

3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
XT1 clock oscillation frequency (f_x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		+1.0	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		+1.5	%
		$+85$ to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$) (5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I_{LH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	$V_i = \text{EV}_{\text{DD0}}$			1	μA
	I_{LH2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	$V_i = \text{V}_{\text{DD}}$			1	μA
	I_{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_i = \text{V}_{\text{DD}}$	In input port or external clock input			1
			In resonator connection			10	μA
Input leakage current, low	I_{LL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	$V_i = \text{EV}_{\text{SS0}}$			-1	μA
	I_{LL2}	P20 to P27, P137, P150 to P156, $\overline{\text{RESET}}$	$V_i = \text{V}_{\text{SS}}$			-1	μA
	I_{LL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	$V_i = \text{V}_{\text{SS}}$	In input port or external clock input			-1
			In resonator connection			-10	μA
On-chip pll-up resistance	R_u	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	$V_i = \text{EV}_{\text{SS0}}$, In input port	10	20	100	$\text{k}\Omega$

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit	
			MIN.	MAX.		
Transfer rate		Transmission	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V		2.6 ^{Note 2}	Mbps
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V		Note 3	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V		1.2 ^{Note 4}	Mbps
			2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V		Note 5	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V		0.43 ^{Note 6}	Mbps

Notes 1. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.4 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

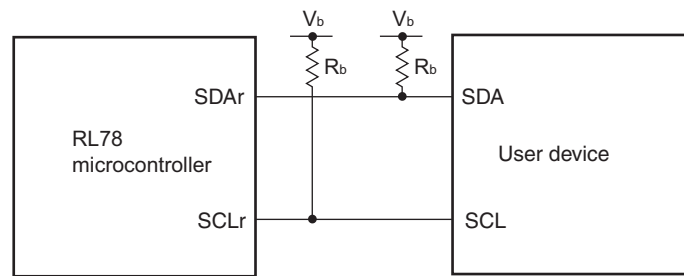
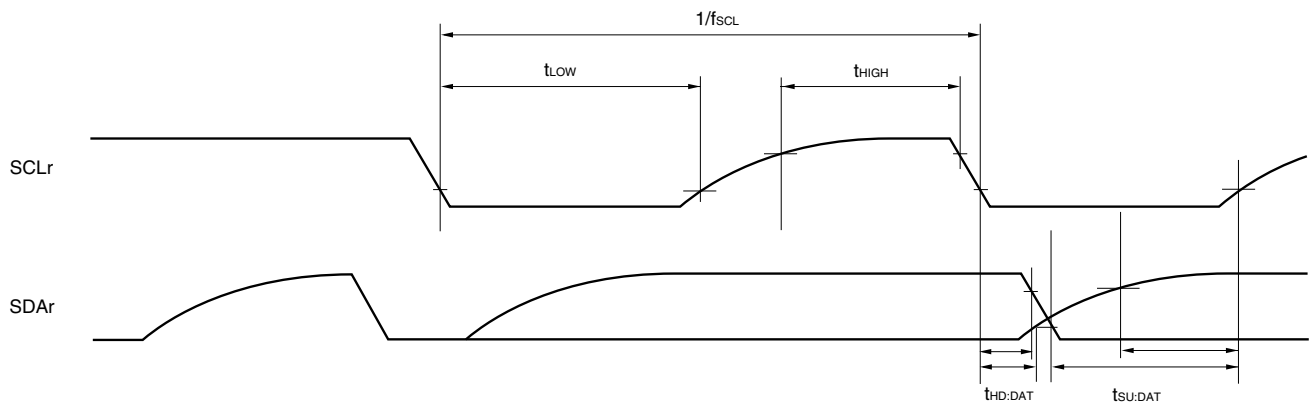
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Data setup time (reception)	$t_{\text{SU:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ <small>Note 2</small>		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 340$ <small>Note 2</small>		ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ <small>Note 2</small>		ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$1/f_{\text{MCK}} + 760$ <small>Note 2</small>		ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$1/f_{\text{MCK}} + 570$ <small>Note 2</small>		ns
Data hold time (transmission)	$t_{\text{HD:DAT}}$	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 50\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	770	ns
		$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.8\text{ k}\Omega$	0	1420	ns
		$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	0	1420	ns
		$2.4\text{ V} \leq \text{EV}_{\text{DD}0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$, $C_b = 100\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	0	1215	ns

Notes 1. The value must also be equal to or less than $f_{\text{MCK}}/4$.

2. Set the f_{MCK} value to keep the hold time of $\text{SCLr} = \text{"L"}$ and $\text{SCLr} = \text{"H"}$.

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)Simplified I²C mode serial transfer timing (during communication at different potential)

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 - r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

3.5.2 Serial interface IICA

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode				Unit
			Standard Mode		Fast Mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode: f _{CLK} ≥ 3.5 MHz	–	–	0	400	kHz
		Standard mode: f _{CLK} ≥ 1 MHz	0	100	–	–	kHz
Setup time of restart condition	t _{SU:STA}		4.7		0.6		μs
Hold time ^{Note 1}	t _{HD:STA}		4.0		0.6		μs
Hold time when SCLA0 = "L"	t _{LOW}		4.7		1.3		μs
Hold time when SCLA0 = "H"	t _{HIGH}		4.0		0.6		μs
Data setup time (reception)	t _{SU:DAT}		250		100		ns
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}		0	3.45	0	0.9	μs
Setup time of stop condition	t _{SU:STO}		4.0		0.6		μs
Bus-free time	t _{BUF}		4.7		1.3		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R> 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

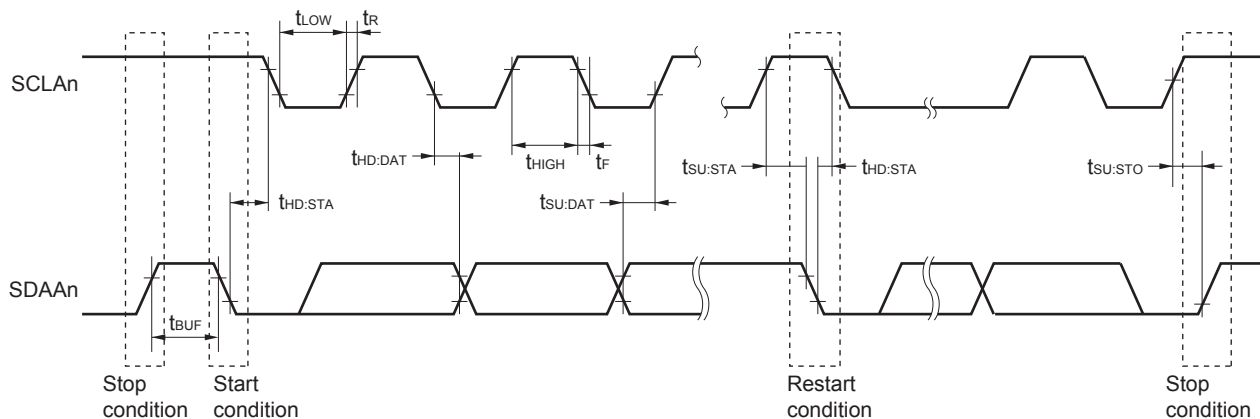
Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



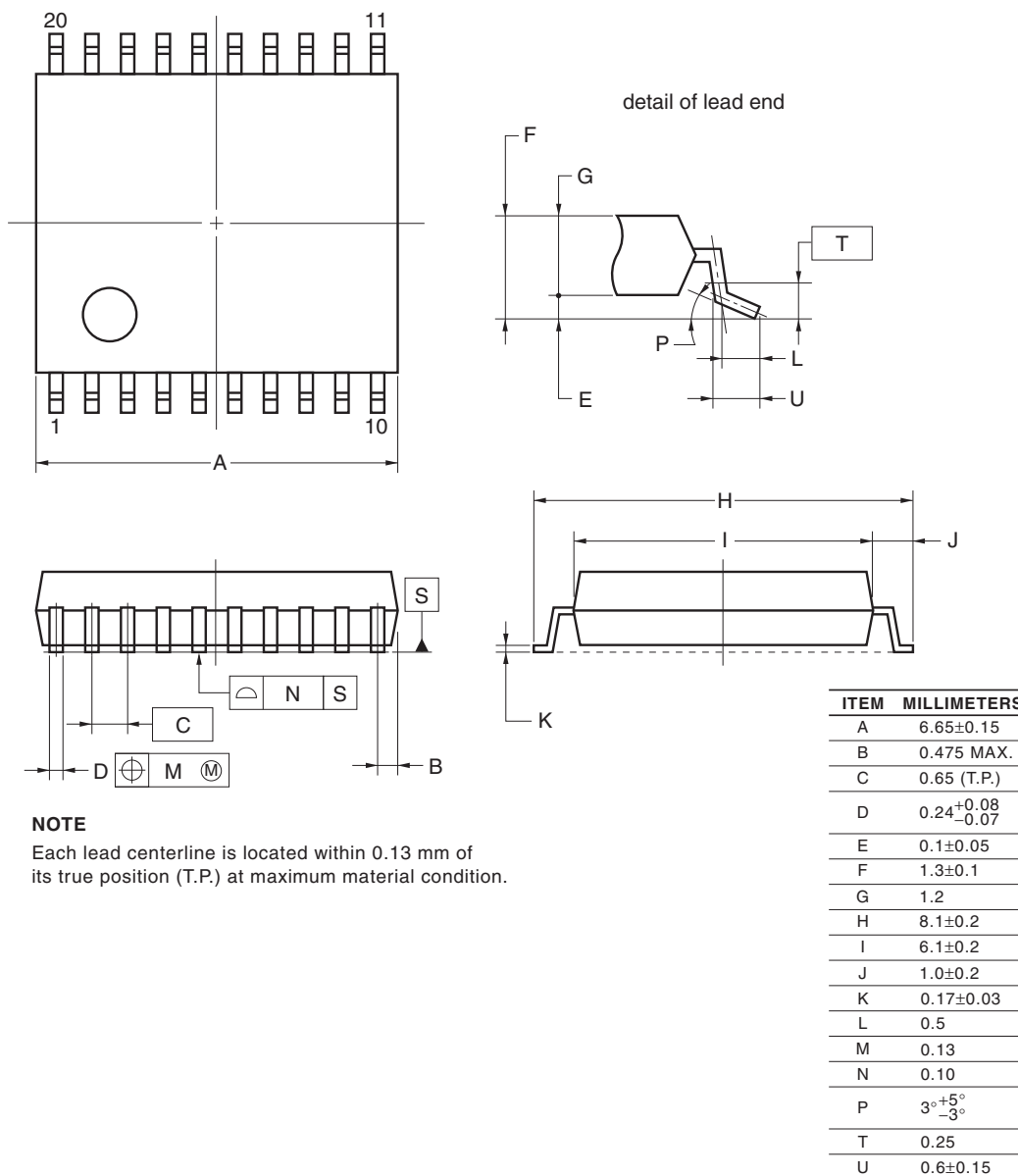
Remark n = 0, 1

4. PACKAGE DRAWINGS

4.1 20-pin Products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP
 R5F1006AGSP, R5F1006CGSP, R5F1006DGSP, R5F1006EGSP

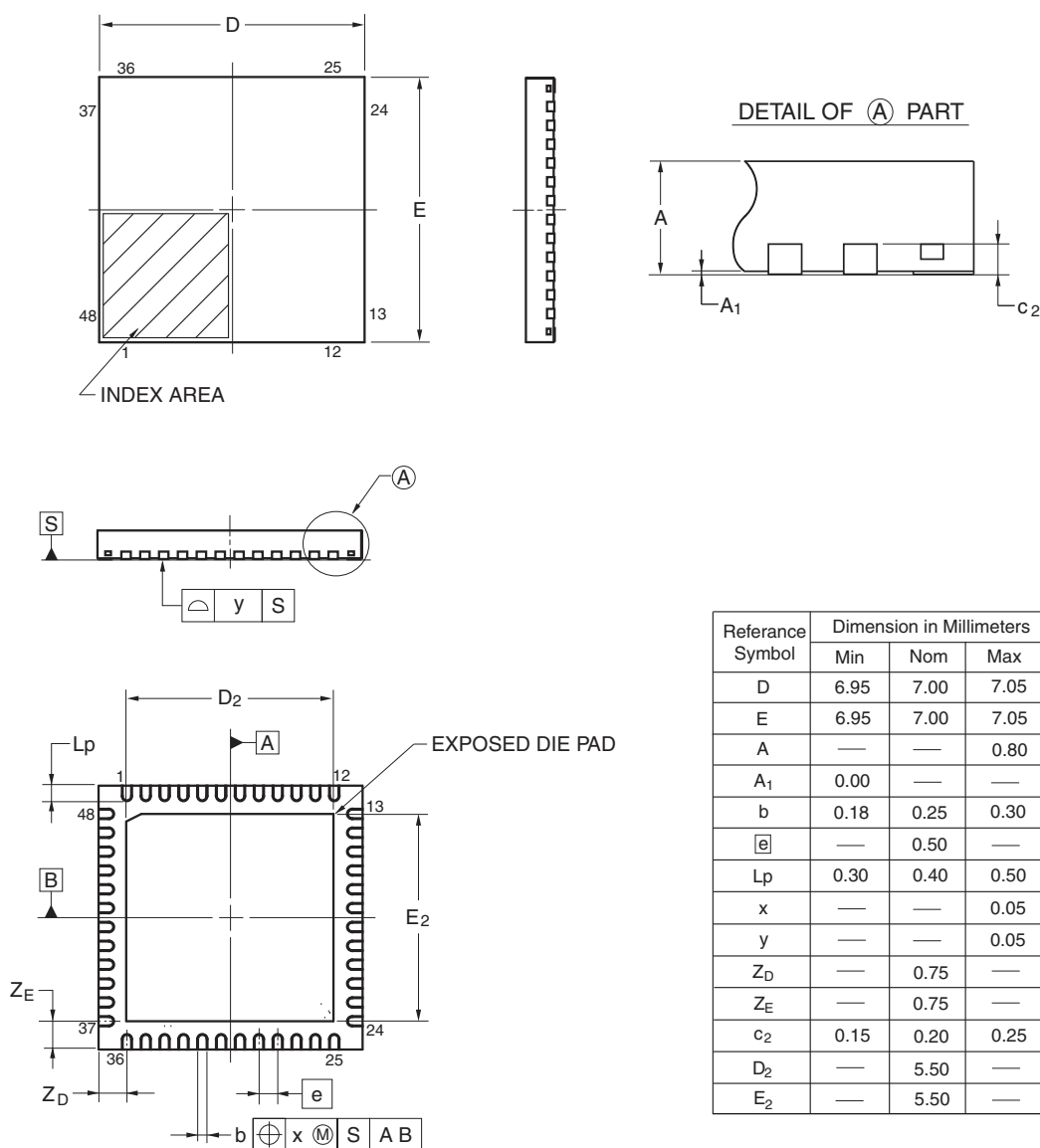
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



NOTE
 Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
 R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
 R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13



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