What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"
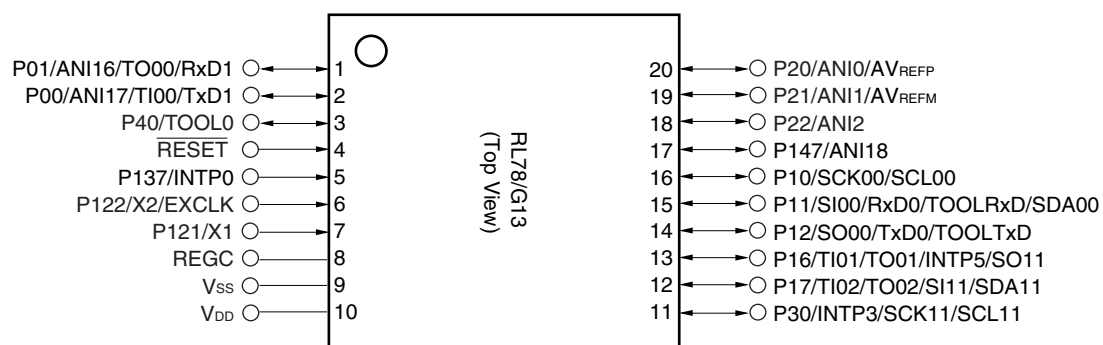
Details	
Product Status	Discontinued at Digi-Key
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	31
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101fgafp-v0

1.3 Pin Configuration (Top View)
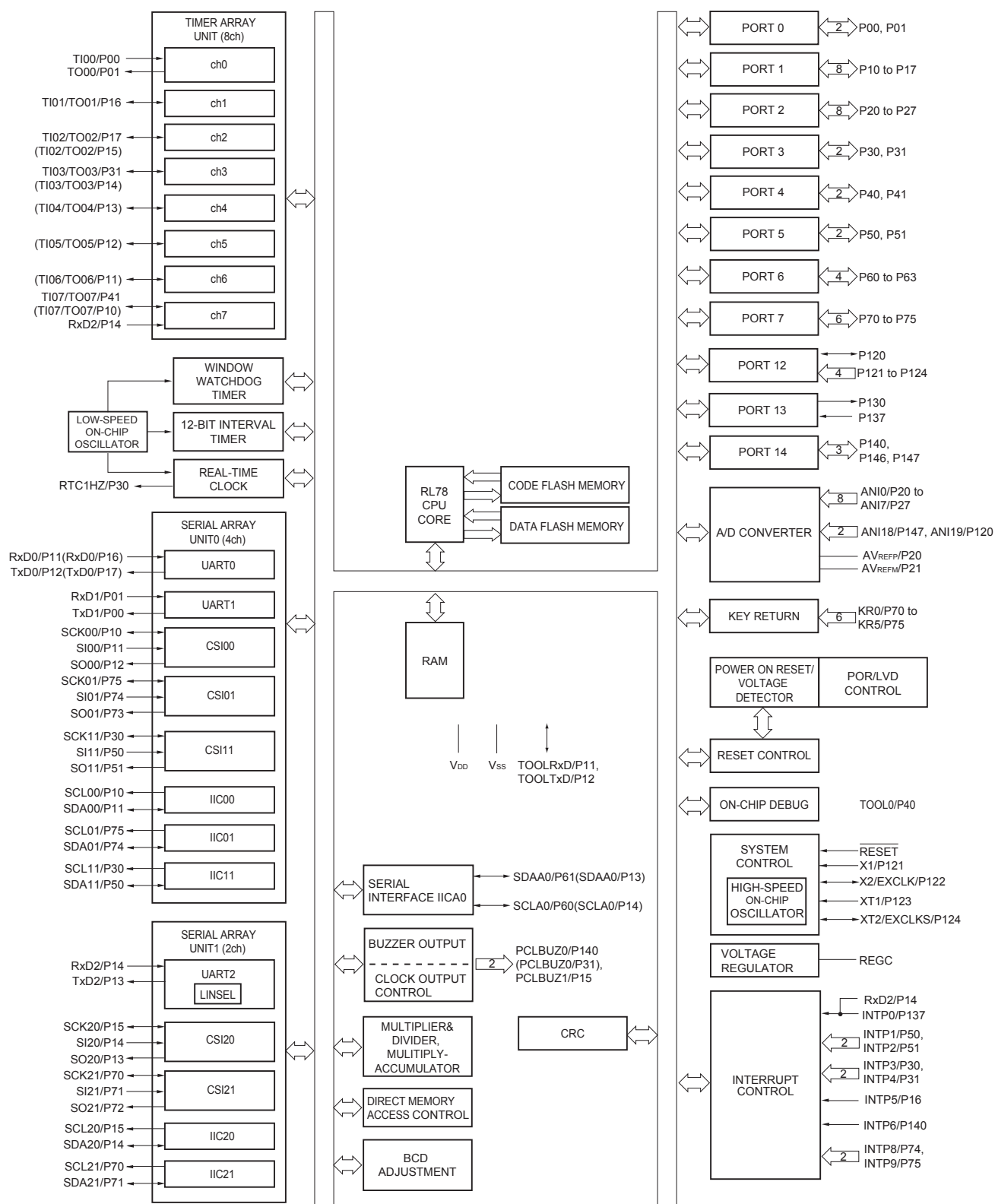
1.3.1 20-pin products

- 20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

P01/ANI16/TO00/RxD1	1
P00/ANI17/TI00/TxD1	2
P40/TOOL0	3
$\overline{\text{RESET}}$	4
P137/INTP0	5
P122/X2/EXCLK	6
P121/X1	7
REGC	8
V_{SS}	9
V_{DD}	10

RL78/G13
(Top View)

20	P20/ANI0/AV$_{REFP}$
19	P21/ANI1/AV$_{REFM}$
18	P22/ANI2
17	P147/ANI18
16	P10/SCK00/SCL00
15	P11/SI00/RxD0/TOOLRxD/SDA00
14	P12/SO00/TxD0/TOOLTxD
13	P16/TI01/TO01/INTP5/SO11
12	P17/TI02/TO02/SI11/SDA11
11	P30/INTP3/SCK11/SCL11

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark   For pin identification, see **1.4 Pin Identification**.

1.5.9 48-pin products

TIMER ARRAY UNIT (8ch)

TI00/P00
TO00/P01 — ch0

TI01/TO01/P16 — ch1

TI02/TO02/P17
(TI02/TO02/P15) — ch2

TI03/TO03/P31
(TI03/TO03/P14) — ch3

(TI04/TO04/P13) — ch4

(TI05/TO05/P12) — ch5

(TI06/TO06/P11) — ch6

TI07/TO07/P41
(TI07/TO07/P10) — ch7
RxD2/P14

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12-BIT INTERVAL TIMER

RTC1HZ/P30 — REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16)
TxD0/P12(TxD0/P17) — UART0

RxD1/P01
TxD1/P00 — UART1

SCK00/P10
SI00/P11
SO00/P12 — CSI00

SCK01/P75
SI01/P74
SO01/P73 — CSI01

SCK11/P30
SI11/P50
SO11/P51 — CSI11

SCL00/P10
SDA00/P11 — IIC00

SCL01/P75
SDA01/P74 — IIC01

SCL11/P30
SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)

RxD2/P14
TxD2/P13 — UART2
LINSEL

SCK20/P15
SI20/P14
SO20/P13 — CSI20

SCK21/P70
SI21/P71
SO21/P72 — CSI21

SCL20/P15
SDA20/P14 — IIC20

SCL21/P70
SDA21/P71 — IIC21

RL78 CPU CORE

CODE FLASH MEMORY

DATA FLASH MEMORY

RAM

V_{DD}　V_{SS}　TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13)
— SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT

CLOCK OUTPUT CONTROL — 2 — PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

CRC

PORT 0 — 2 — P00, P01

PORT 1 — 8 — P10 to P17

PORT 2 — 8 — P20 to P27

PORT 3 — 2 — P30, P31

PORT 4 — 2 — P40, P41

PORT 5 — 2 — P50, P51

PORT 6 — 4 — P60 to P63

PORT 7 — 6 — P70 to P75

PORT 12 — P120
— 4 — P121 to P124

PORT 13 — P130
— P137

PORT 14 — 3 — P140, P146, P147

A/D CONVERTER — 8 — ANI0/P20 to ANI7/P27
— 2 — ANI18/P147, ANI19/P120
— AV$_{REFP}$/P20
— AV$_{REFM}$/P21

KEY RETURN — 6 — KR0/P70 to KR5/P75

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL
HIGH-SPEED ON-CHIP OSCILLATOR — RESET
— X1/P121
— X2/EXCLK/P122
— XT1/P123
— XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL — RxD2/P14
INTP0/P137
— 2 — INTP1/P50, INTP2/P51
— 2 — INTP3/P30, INTP4/P31
— INTP5/P16
— INTP6/P140
— 2 — INTP8/P74, INTP9/P75

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8　Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.10 52-pin products

TIMER ARRAY UNIT (8ch)

TI00/P00
TO00/P01 — ch0

TI01/TO01/P16 — ch1

TI02/TO02/P17
(TI02/TO02/P15) — ch2

TI03/TO03/P31
(TI03/TO03/P14) — ch3

(TI04/TO04/P13) — ch4

(TI05/TO05/P12) — ch5

(TI06/TO06/P11) — ch6

TI07/TO07/P41
(TI07/TO07/P10) — ch7
RxD2/P14
(RxD2/P76)

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR → 12-BIT INTERVAL TIMER

RTC1HZ/P30 → REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16)
TxD0/P12(TxD0/P17) — UART0

RxD1/P03
TxD1/P02 — UART1

SCK00/P10
SI00/P11
SO00/P12 — CSI00

SCK01/P75
SI01/P74
SO01/P73 — CSI01

SCK11/P30
SI11/P50
SO11/P51 — CSI11

SCL00/P10
SDA00/P11 — IIC00

SCL01/P75
SDA01/P74 — IIC01

SCL11/P30
SDA11/P50 — IIC11

SERIAL ARRAY UNIT1 (2ch)

RxD2/P14(RxD2/P76)
TxD2/P13(TxD2/P77) — UART2 [LINSEL]

SCK20/P15
SI20/P14
SO20/P13 — CSI20

SCK21/P70
SI21/P71
SO21/P72 — CSI21

SCL20/P15
SDA20/P14 — IIC20

SCL21/P70
SDA21/P71 — IIC21

RL78 CPU CORE

CODE FLASH MEMORY
DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 → SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT
CLOCK OUTPUT CONTROL → 2 → PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P15

MULTIPLIER & DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 4 — P00 to P03
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 2 — P40, P41
PORT 5 — 2 — P50, P51
PORT 6 — 4 — P60 to P63
PORT 7 — 8 — P70 to P77
PORT 12 — P120, 4 — P121 to P124
PORT 13 — P130, P137
PORT 14 — 3 — P140, P146, P147

A/D CONVERTER — 8 — ANI0/P20 to ANI7/P27, 4 — ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120
AV_{REFP}/P20
AV_{REFM}/P21

KEY RETURN — 8 — KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR   POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL
$\overline{RESET}$
X1/P121
X2/EXCLK/P122
XT1/P123
XT2/EXCLKS/P124

HIGH-SPEED ON-CHIP OSCILLATOR

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
RxD2/P14 (RxD2/P76)
INTP0/P137
2 — INTP1/P50, INTP2/P51
2 — INTP3/P30, INTP4/P31
INTP5/P16
INTP6/P140
4 — INTP8/P74 to INTP11/P77

Remark　Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

[80-pin, 100-pin, 128-pin products]

Caution   This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Code flash memory (KB)		96 to 512		96 to 512		192 to 512	
Data flash memory (KB)		8	–	8	–	8	–
RAM (KB)		8 to 32 [Note 1]		8 to 32 [Note 1]		16 to 32 [Note 1]	
Address space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (High-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V_{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V_{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V_{DD} = 1.6 to 5.5 V)					
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz					
Low-speed on-chip oscillator		15 kHz (TYP.)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)					
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)					
		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.					
I/O port	Total	74		92		120	
	CMOS I/O	64 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 21)		82 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 24)		110 (N-ch O.D. I/O [EV_{DD} withstand voltage]: 25)	
	CMOS input	5		5		5	
	CMOS output	1		1		1	
	N-ch O.D. I/O (withstand voltage: 6 V)	4		4		4	
Timer	16-bit timer	12 channels		12 channels		16 channels	
	Watchdog timer	1 channel		1 channel		1 channel	
	Real-time clock (RTC)	1 channel		1 channel		1 channel	
	12-bit interval timer (IT)	1 channel		1 channel		1 channel	
	Timer output	12 channels (PWM outputs: 10 [Note 2])		12 channels (PWM outputs: 10 [Note 2])		16 channels (PWM outputs: 14 [Note 2])	
	RTC output	1 channel • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)					

Notes 1.   The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xJ, R5F101xJ (x = M, P):   Start address FAF00H

R5F100xL, R5F101xL (x = M, P, S):   Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution　Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark　Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)[Note]	Ceramic resonator/ crystal resonator	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V	1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V	1.0		8.0	MHz
		1.6 V ≤ V$_{DD}$ < 1.8 V	1.0		4.0	MHz
XT1 clock oscillation frequency (f$_X$)[Note]	Crystal resonator		32	32.768	35	kHz

Note   Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution   **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark   When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

2.2.2 On-chip oscillator characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency [Notes 1, 2]	f$_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	−1.0		+1.0	%
			1.6 V ≤ V$_{DD}$ < 1.8 V	−5.0		+5.0	%
		−40 to −20 °C	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	−1.5		+1.5	%
			1.6 V ≤ V$_{DD}$ < 1.8 V	−5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1.   High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

     2.   This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I$_{OL1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			70.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			15.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			9.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			80.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			35.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			20.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])				150.0	mA
	I$_{OL2}$	Per pin for P20 to P27, P150 to P156				0.4[Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV$_{SS0}$, EV$_{SS1}$ and V$_{SS}$ pin.

    2. However, do not exceed the total current value.

    3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OL}$ × 0.7)/(n × 0.01)

    <Example> Where n = 80% and I$_{OL}$ = 10.0 mA

        Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

UART mode connection diagram (during communication at same potential)
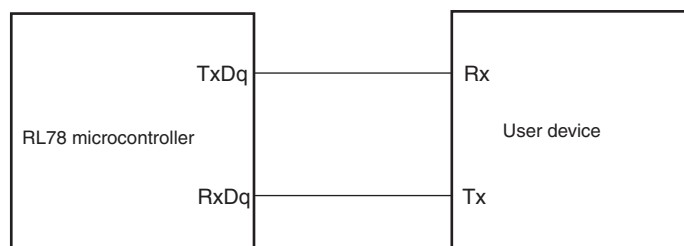
UART mode bit width (during communication at same potential) (reference)
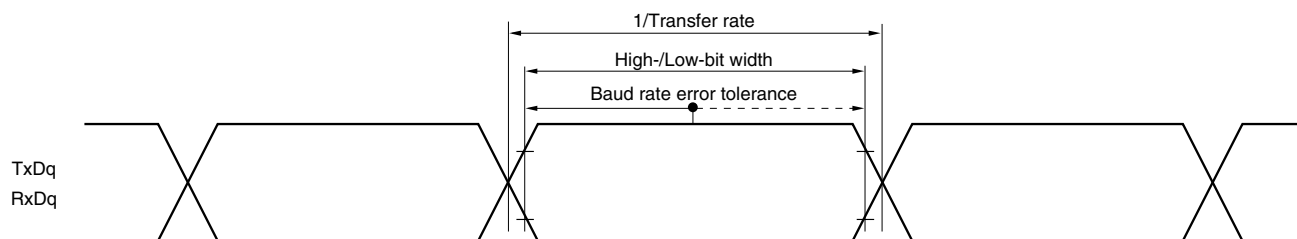
Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

    2. f$_{MCK}$: Serial array unit operation clock frequency

      (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
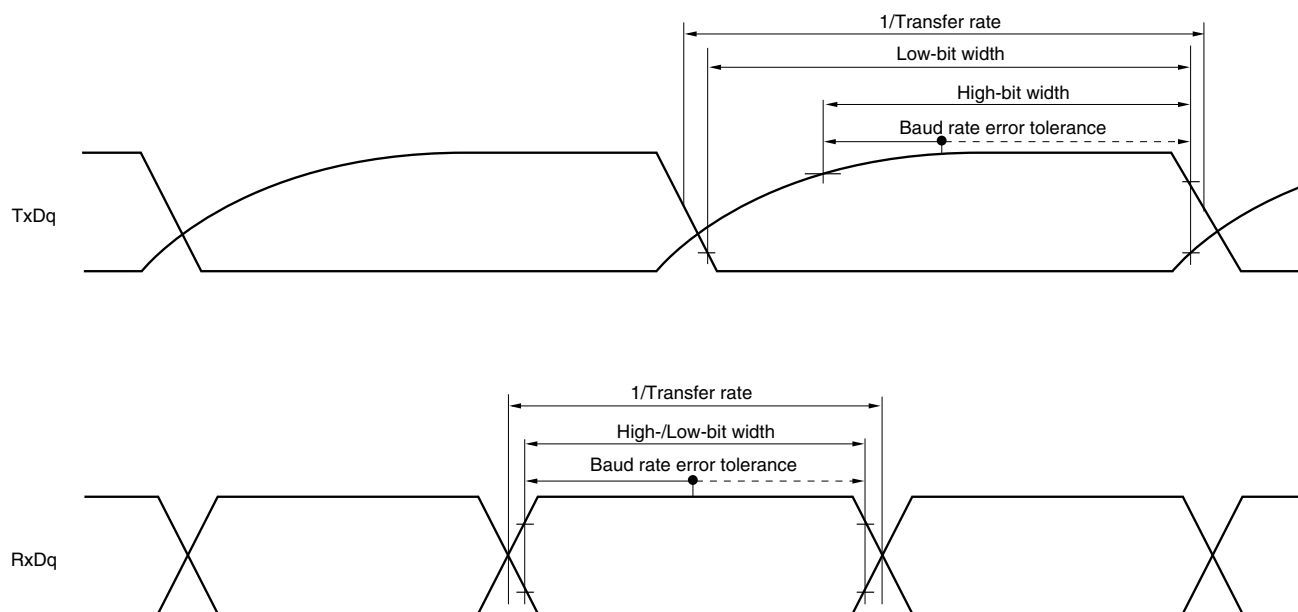
      n: Channel number (mn = 00 to 03, 10 to 13))

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +85°C, 1.8 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps
			2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1		f_{MCK}/6 Note 1	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps
			1.8 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V		f_{MCK}/6 Notes 1 to 3		f_{MCK}/6 Notes 1, 2		f_{MCK}/6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f_{MCK} = f_{CLK} Note 4		5.3		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

　　　2. Use it with $EV_{DD0} \geq V_b$.

　　　3. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

　　　　　2.4 V $\leq$ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps

　　　　　1.8 V $\leq$ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

　　　4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

　　　　　HS (high-speed main) mode:　　　　32 MHz (2.7 V $\leq$ V_{DD} $\leq$ 5.5 V)

　　　　　　　　　　　　　　　　　　　　　16 MHz (2.4 V $\leq$ V_{DD} $\leq$ 5.5 V)

　　　　　LS (low-speed main) mode:　　　　8 MHz (1.8 V $\leq$ V_{DD} $\leq$ 5.5 V)

　　　　　LV (low-voltage main) mode:　　　4 MHz (1.6 V $\leq$ V_{DD} $\leq$ 5.5 V)

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

　　　　2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

　　　　3. f_{MCK}: Serial array unit operation clock frequency

　　　　　　(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

　　　　4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

UART mode bit width (during communication at different potential) (reference)

Remarks **1.** R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

             C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

      2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

      3. f$_{MCK}$: Serial array unit operation clock frequency

           (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

           m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

      4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection

           register (PIOR) is 1.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/2)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp high-/low-level width	t_{KH2}, t_{KL2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	t_{KCY2}/2 − 12		t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	t_{KCY2}/2 − 18		t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2]	t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		t_{KCY2}/2 − 50		ns
SIp setup time (to SCKp↑) [Note 3]	t_{SIK2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V	1/f_{MCK} + 20		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2]	1/f_{MCK} + 30		1/f_{MCK} + 30		1/f_{MCK} + 30		ns
SIp hold time (from SCKp↑) [Note 4]	t_{KSI2}		1/f_{MCK} + 31		1/f_{MCK} + 31		1/f_{MCK} + 31		ns
Delay time from SCKp↓ to SOp output [Note 5]	t_{KSO2}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		2/f_{MCK} + 120		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		2/f_{MCK} + 214		2/f_{MCK} + 573		2/f_{MCK} + 573	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ		2/f_{MCK} + 573		2/f_{MCK} + 573		2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with EV_{DD0} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

t_{KCY2}

t_{KL2} t_{KH2}

SCKp

t_{SIK2} t_{KSI2}

SIp   Input data

t_{KSO2}

SOp   Output data

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

t_{KCY2}

t_{KH2} t_{KL2}

SCKp

t_{SIK2} t_{KSI2}

SIp   Input data

t_{KSO2}

SOp   Output data
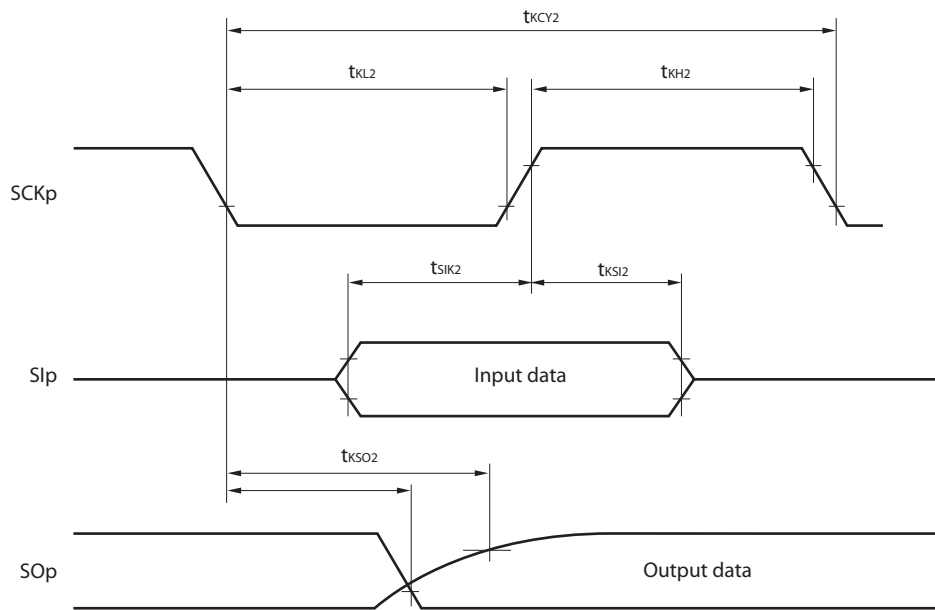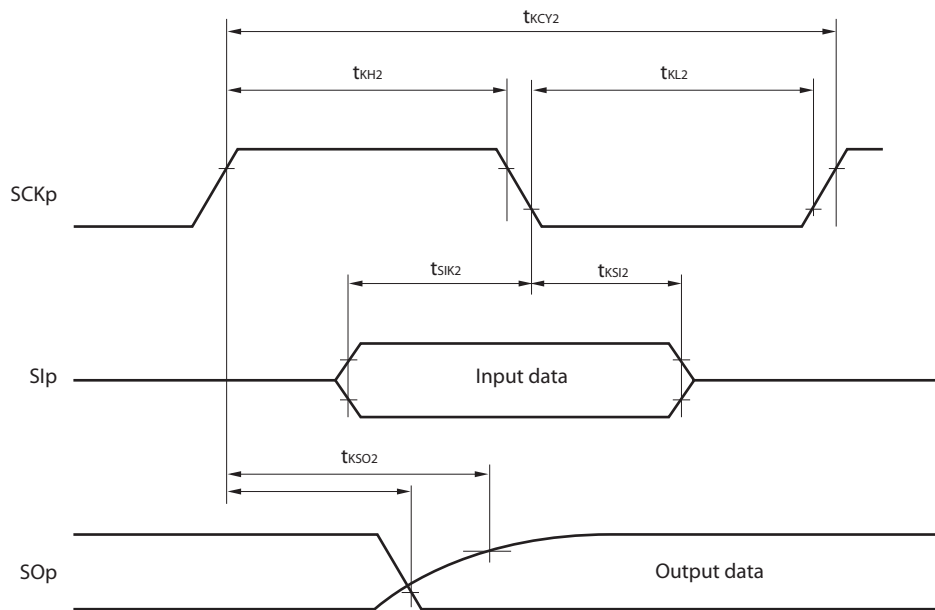
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.

<R>   **2.** The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution **The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.**

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (5/5)

| Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{DD0}$				1	μA
	I$_{LIH2}$	P20 to P27, P137, P150 to P156, RESET	V$_I$ = V$_{DD}$				1	μA
	I$_{LIH3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I$_{LIL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$				−1	μA
	I$_{LIL2}$	P20 to P27, P137, P150 to P156, RESET	V$_I$ = V$_{SS}$				−1	μA
	I$_{LIL3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R$_U$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$, In input port		10	20	100	kΩ

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	I$_{DD2}$ Note 2	HALT mode	HS (high-speed main) mode Note 7	f$_{IH}$ = 32 MHz Note 4	V$_{DD}$ = 5.0 V		0.62	3.40	mA
					V$_{DD}$ = 3.0 V		0.62	3.40	mA
				f$_{IH}$ = 24 MHz Note 4	V$_{DD}$ = 5.0 V		0.50	2.70	mA
					V$_{DD}$ = 3.0 V		0.50	2.70	mA
				f$_{IH}$ = 16 MHz Note 4	V$_{DD}$ = 5.0 V		0.44	1.90	mA
					V$_{DD}$ = 3.0 V		0.44	1.90	mA
			HS (high-speed main) mode Note 7	f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 20 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 5.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
				f$_{MX}$ = 10 MHz Note 3, V$_{DD}$ = 3.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
				f$_{SUB}$ = 32.768 kHz Note 5 T$_A$ = +105°C	Square wave input		5.50	41.00	μA
					Resonator connection		5.50	41.00	μA
	I$_{DD3}$ Note 6	STOP mode Note 8	T$_A$ = −40°C				0.19	0.52	μA
			T$_A$ = +25°C				0.25	0.52	μA
			T$_A$ = +50°C				0.32	2.21	μA
			T$_A$ = +70°C				0.55	3.94	μA
			T$_A$ = +85°C				1.00	7.95	μA
			T$_A$ = +105°C				5.00	40.00	μA

(**Notes** and **Remarks** are listed on the next page.)

Simplified I^{2}C mode mode connection diagram (during communication at same potential)
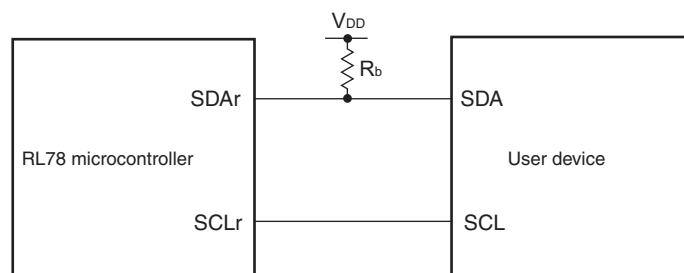
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
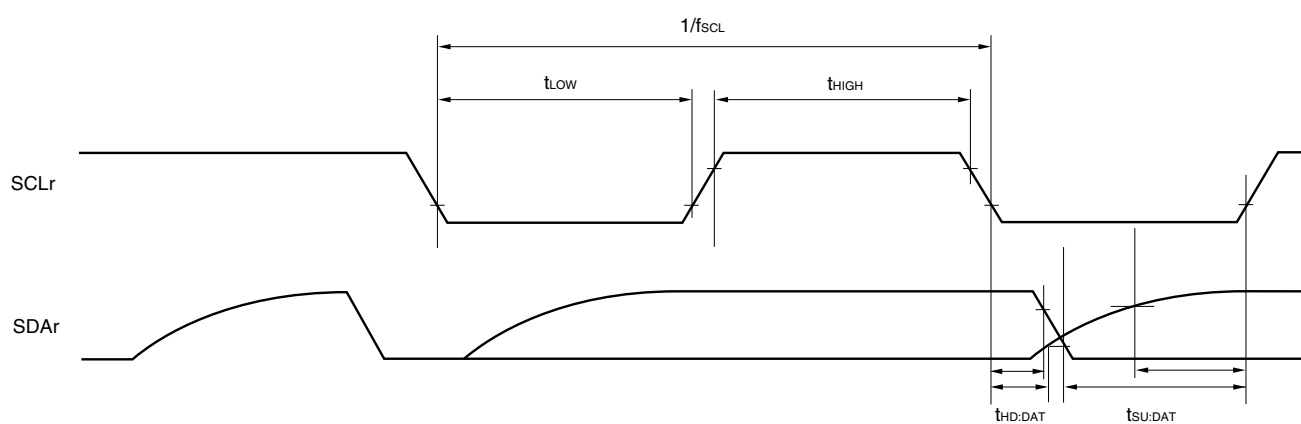
Remarks 1. R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m

= 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
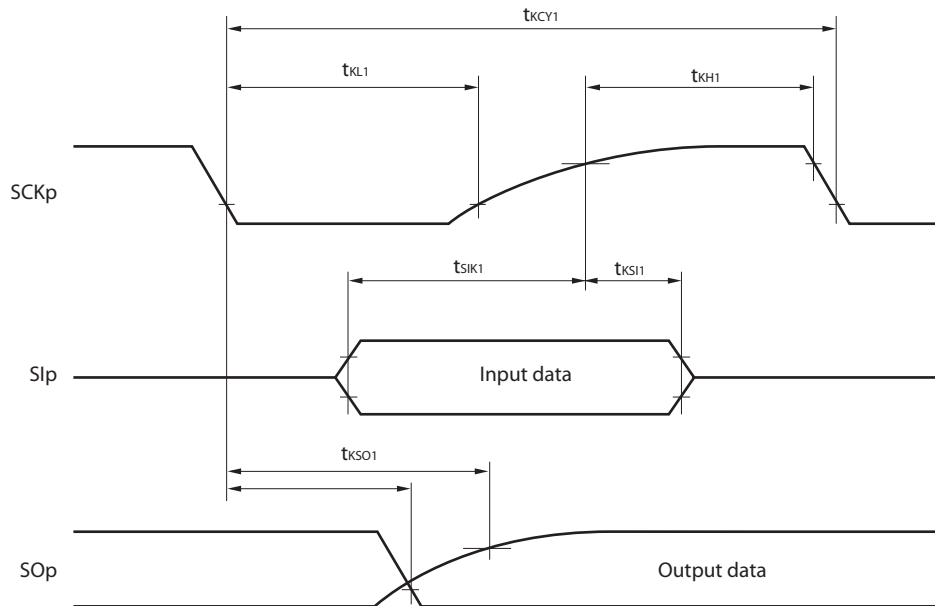
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
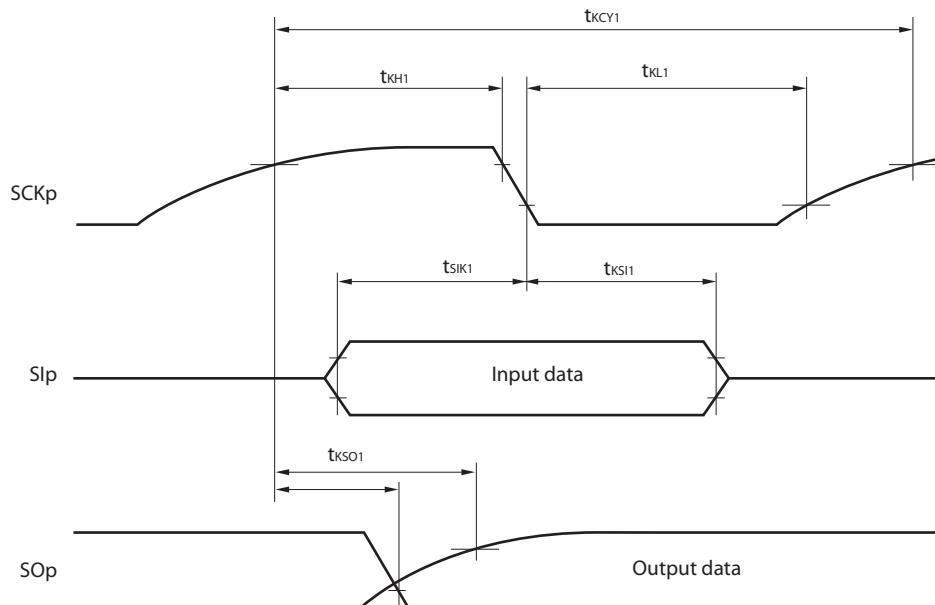
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel
number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
   2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

CSI mode connection diagram (during communication at different potential)
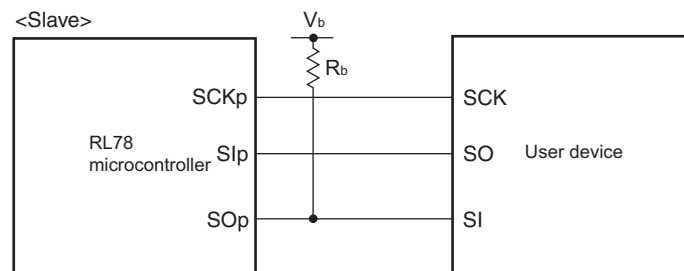
Remarks 1. R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02,
 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

 3. f$_{MCK}$: Serial array unit operation clock frequency

 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

 m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
 Use other CSI for communication at different potential.

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	2.4 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI14		0		V$_{DD}$	V
		ANI16 to ANI26		0		EV$_{DD0}$	V
		Internal reference voltage output (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 3]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 3]		V

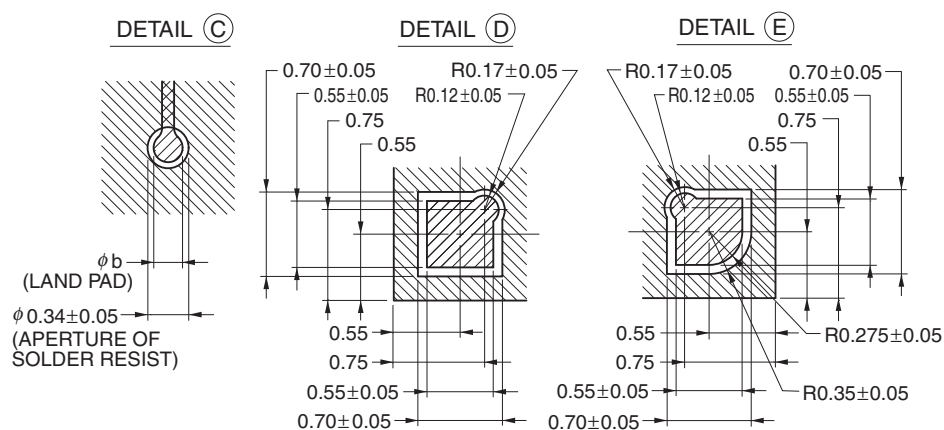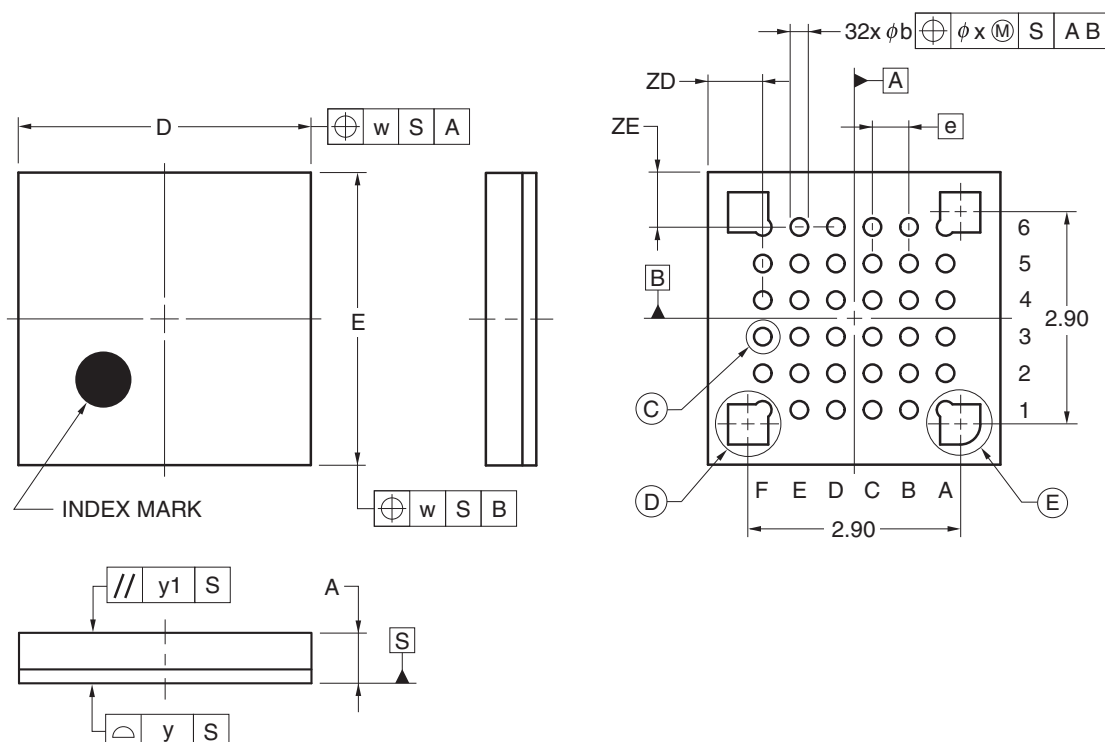**Notes 1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

INDEX MARK

DETAIL C

φ b
(LAND PAD)

φ 0.34±0.05
(APERTURE OF
SOLDER RESIST)

DETAIL D

0.70±0.05
0.55±0.05
0.75
0.55
R0.17±0.05
R0.12±0.05
0.55
0.75
0.55±0.05
0.70±0.05

DETAIL E

R0.17±0.05
R0.12±0.05
0.70±0.05
0.55±0.05
0.75
0.55
0.55
0.75
R0.275±0.05
0.55±0.05
0.70±0.05
R0.35±0.05

32x φb

ZD
ZE

2.90

2.90

F E D C B A

(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75