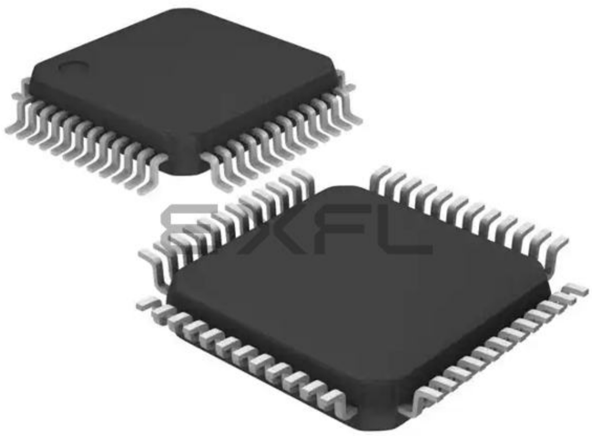

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 10x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gcafb-50 |

○ ROM, RAM capacities

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | 20 pins | 24 pins | 25 pins | 30 pins | 32 pins | 36 pins |
| 128 KB | 8 KB | 12 KB | – | – | – | R5F100AG | R5F100BG | R5F100CG |
| | – | | – | – | – | R5F101AG | R5F101BG | R5F101CG |
| 96 KB | 8 KB | 8 KB | – | – | – | R5F100AF | R5F100BF | R5F100CF |
| | – | | – | – | – | R5F101AF | R5F101BF | R5F101CF |
| 64 KB | 4 KB | 4 KB Note | R5F1006E | R5F1007E | R5F1008E | R5F100AE | R5F100BE | R5F100CE |
| | – | | R5F1016E | R5F1017E | R5F1018E | R5F101AE | R5F101BE | R5F101CE |
| 48 KB | 4 KB | 3 KB Note | R5F1006D | R5F1007D | R5F1008D | R5F100AD | R5F100BD | R5F100CD |
| | – | | R5F1016D | R5F1017D | R5F1018D | R5F101AD | R5F101BD | R5F101CD |
| 32 KB | 4 KB | 2 KB | R5F1006C | R5F1007C | R5F1008C | R5F100AC | R5F100BC | R5F100CC |
| | – | | R5F1016C | R5F1017C | R5F1018C | R5F101AC | R5F101BC | R5F101CC |
| 16 KB | 4 KB | 2 KB | R5F1006A | R5F1007A | R5F1008A | R5F100AA | R5F100BA | R5F100CA |
| | – | | R5F1016A | R5F1017A | R5F1018A | R5F101AA | R5F101BA | R5F101CA |

| Flash ROM | Data flash | RAM | RL78/G13 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | 40 pins | 44 pins | 48 pins | 52 pins | 64 pins | 80 pins | 100 pins | 128 pins |
| 512 KB | 8 KB | 32 KB Note | – | R5F100FL | R5F100GL | R5F100JL | R5F100LL | R5F100ML | R5F100PL | R5F100SL |
| | – | | – | R5F101FL | R5F101GL | R5F101JL | R5F101LL | R5F101ML | R5F101PL | R5F101SL |
| 384 KB | 8 KB | 24 KB | – | R5F100FK | R5F100GK | R5F100JK | R5F100LK | R5F100MK | R5F100PK | R5F100SK |
| | – | | – | R5F101FK | R5F101GK | R5F101JK | R5F101LK | R5F101MK | R5F101PK | R5F101SK |
| 256 KB | 8 KB | 20 KB Note | – | R5F100FJ | R5F100GJ | R5F100JJ | R5F100LJ | R5F100MJ | R5F100PJ | R5F100SJ |
| | – | | – | R5F101FJ | R5F101GJ | R5F101JJ | R5F101LJ | R5F101MJ | R5F101PJ | R5F101SJ |
| 192 KB | 8 KB | 16 KB | R5F100EH | R5F100FH | R5F100GH | R5F100JH | R5F100LH | R5F100MH | R5F100PH | R5F100SH |
| | – | | R5F101EH | R5F101FH | R5F101GH | R5F101JH | R5F101LH | R5F101MH | R5F101PH | R5F101SH |
| 128 KB | 8 KB | 12 KB | R5F100EG | R5F100FG | R5F100GG | R5F100JG | R5F100LG | R5F100MG | R5F100PG | – |
| | – | | R5F101EG | R5F101FG | R5F101GG | R5F101JG | R5F101LG | R5F101MG | R5F101PG | – |
| 96 KB | 8 KB | 8 KB | R5F100EF | R5F100FF | R5F100GF | R5F100JF | R5F100LF | R5F100MF | R5F100PF | – |
| | – | | R5F101EF | R5F101FF | R5F101GF | R5F101JF | R5F101LF | R5F101MF | R5F101PF | – |
| 64 KB | 4 KB | 4 KB Note | R5F100EE | R5F100FE | R5F100GE | R5F100JE | R5F100LE | – | – | – |
| | – | | R5F101EE | R5F101FE | R5F101GE | R5F101JE | R5F101LE | – | – | – |
| 48 KB | 4 KB | 3 KB Note | R5F100ED | R5F100FD | R5F100GD | R5F100JD | R5F100LD | – | – | – |
| | – | | R5F101ED | R5F101FD | R5F101GD | R5F101JD | R5F101LD | – | – | – |
| 32 KB | 4 KB | 2 KB | R5F100EC | R5F100FC | R5F100GC | R5F100JC | R5F100LC | – | – | – |
| | – | | R5F101EC | R5F101FC | R5F101GC | R5F101JC | R5F101LC | – | – | – |
| 16 KB | 4 KB | 2 KB | R5F100EA | R5F100FA | R5F100GA | – | – | – | – | – |
| | – | | R5F101EA | R5F101FA | R5F101GA | – | – | – | – | – |

**Note** The flash library uses RAM in self-programming and rewriting of the data flash memory.

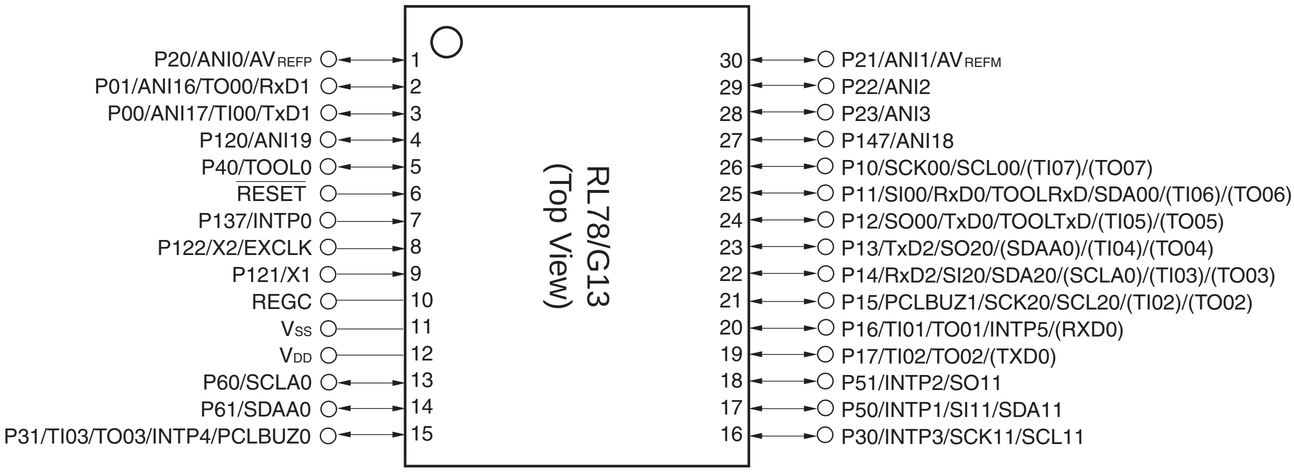
The target products and start address of the RAM areas used by the flash library are shown below.

R5F100xD, R5F101xD (x = 6 to 8, A to C, E to G, J, L): Start address FF300H
R5F100xE, R5F101xE (x = 6 to 8, A to C, E to G, J, L): Start address FEF00H
R5F100xJ, R5F101xJ (x = F, G, J, L, M, P): Start address FAF00H
R5F100xL, R5F101xL (x = F, G, J, L, M, P, S): Start address F7F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

### 1.3.4 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)

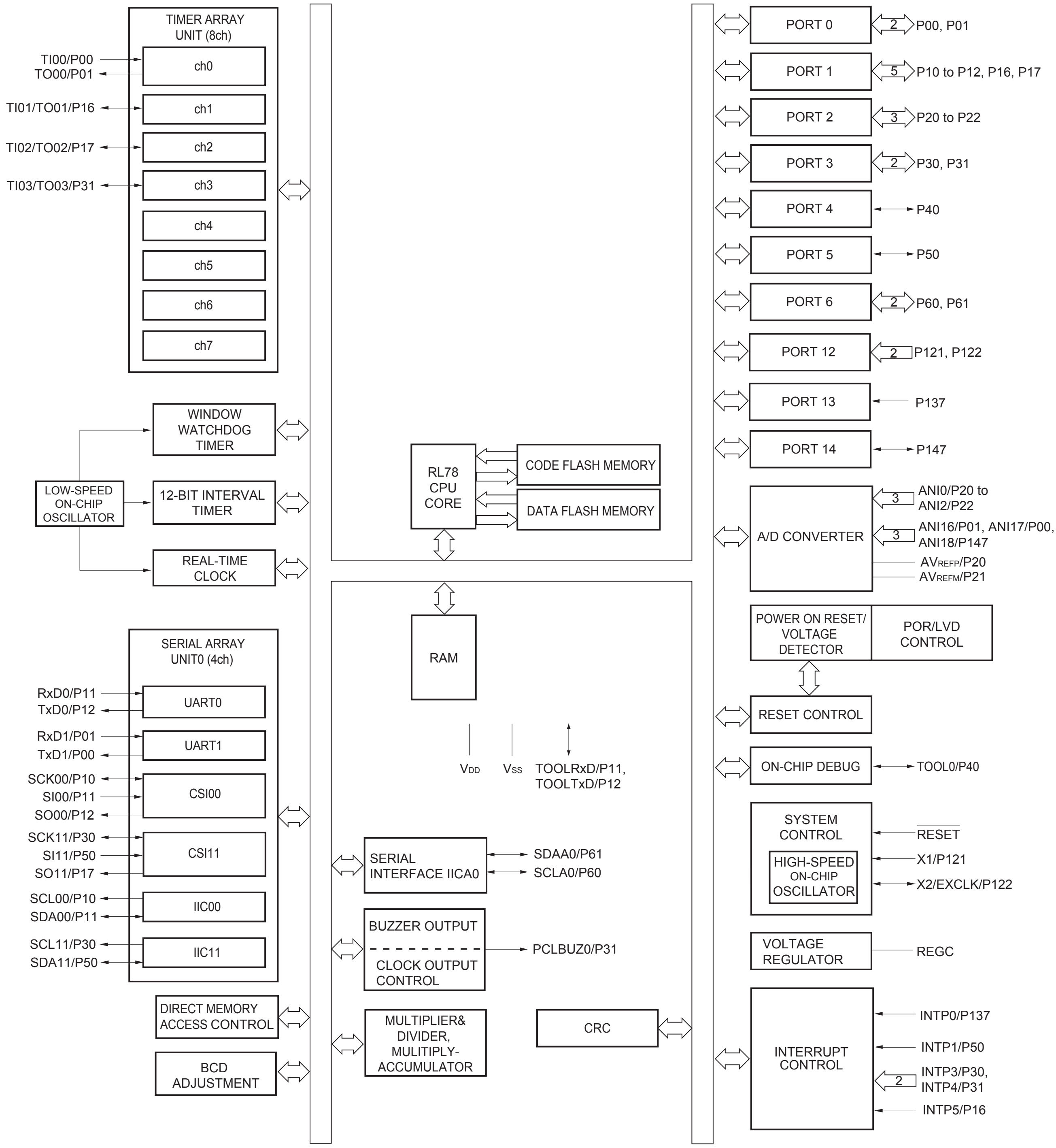



**Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

### 1.5.2 24-pin products



**2.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

**3.** When setting to PIOR = 1

(2/2)

| Item | | 40-pin | | 44-pin | | 48-pin | | 52-pin | | 64-pin | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | R5F100Ex | R5F101Ex | R5F100Fx | R5F101Fx | R5F100Gx | R5F101Gx | R5F100Jx | R5F101Jx | R5F100Lx | R5F101Lx |
| Clock output/buzzer output | | 2 | | 2 | | 2 | | 2 | | 2 | |
| | | • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz<br>(Main system clock: $f_{MAIN}$ = 20 MHz operation)<br>• 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz<br>(Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | | | | | |
| 8/10-bit resolution A/D converter | | 9 channels | | 10 channels | | 10 channels | | 12 channels | | 12 channels | |
| Serial interface | | [40-pin, 44-pin products]<br>• CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel<br>• CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel<br>• CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel<br>[48-pin, 52-pin products]<br>• CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel<br>• CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel<br>• CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel<br>[64-pin products]<br>• CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel<br>• CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel<br>• CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel | | | | | | | | | |
| | I²C bus | 1 channel | | 1 channel | | 1 channel | | 1 channel | | 1 channel | |
| Multiplier and divider/multiply-accumulator | | • 16 bits × 16 bits = 32 bits (Unsigned or signed)<br>• 32 bits ÷ 32 bits = 32 bits (Unsigned)<br>• 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) | | | | | | | | | |
| DMA controller | | 2 channels | | | | | | | | | |
| Vectored interrupt sources | Internal | 27 | | 27 | | 27 | | 27 | | 27 | |
| | External | 7 | | 7 | | 10 | | 12 | | 13 | |
| Key interrupt | | 4 | | 4 | | 6 | | 8 | | 8 | |
| Reset | | • Reset by RESET pin<br>• Internal reset by watchdog timer<br>• Internal reset by power-on-reset<br>• Internal reset by voltage detector<br>• Internal reset by illegal instruction execution [Note]<br>• Internal reset by RAM parity error<br>• Internal reset by illegal-memory access | | | | | | | | | |
| Power-on-reset circuit | | • Power-on-reset: 1.51 V (TYP.)<br>• Power-down-reset: 1.50 V (TYP.) | | | | | | | | | |
| Voltage detector | | • Rising edge : 1.67 V to 4.06 V (14 stages)<br>• Falling edge : 1.63 V to 3.98 V (14 stages) | | | | | | | | | |
| On-chip debug function | | Provided | | | | | | | | | |
| Power supply voltage | | $V_{DD}$ = 1.6 to 5.5 V ($T_A$ = -40 to +85°C)<br>$V_{DD}$ = 2.4 to 5.5 V ($T_A$ = -40 to +105°C) | | | | | | | | | |
| <R> Operating ambient temperature | | $T_A$ = 40 to +85°C (A: Consumer applications, D: Industrial applications)<br>$T_A$ = 40 to +105°C (G: Industrial applications) | | | | | | | | | |

**Note** The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin, 128-pin products]

**Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.**

(1/2)

| Item | | 80-pin | | 100-pin | | 128-pin | |
|---|---|---|---|---|---|---|---|
| | | R5F100Mx | R5F101Mx | R5F100Px | R5F101Px | R5F100Sx | R5F101Sx |
| Code flash memory (KB) | | 96 to 512 | | 96 to 512 | | 192 to 512 | |
| Data flash memory (KB) | | 8 | – | 8 | – | 8 | – |
| RAM (KB) | | 8 to 32 Note 1 | | 8 to 32 Note 1 | | 16 to 32 Note 1 | |
| Address space | | 1 MB | | | | | |
| Main system clock | High-speed system clock | X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK)<br>HS (High-speed main) mode: 1 to 20 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| | High-speed on-chip oscillator | HS (High-speed main) mode: 1 to 32 MHz ($V_{DD}$ = 2.7 to 5.5 V),<br>HS (High-speed main) mode: 1 to 16 MHz ($V_{DD}$ = 2.4 to 5.5 V),<br>LS (Low-speed main) mode: 1 to 8 MHz ($V_{DD}$ = 1.8 to 5.5 V),<br>LV (Low-voltage main) mode: 1 to 4 MHz ($V_{DD}$ = 1.6 to 5.5 V) | | | | | |
| Subsystem clock | | XT1 (crystal) oscillation, external subsystem clock input (EXCLKS)<br>32.768 kHz | | | | | |
| Low-speed on-chip oscillator | | 15 kHz (TYP.) | | | | | |
| General-purpose register | | (8-bit register × 8) × 4 banks | | | | | |
| Minimum instruction execution time | | 0.03125 μs (High-speed on-chip oscillator: $f_{IH}$ = 32 MHz operation) | | | | | |
| | | 0.05 μs (High-speed system clock: $f_{MX}$ = 20 MHz operation) | | | | | |
| | | 30.5 μs (Subsystem clock: $f_{SUB}$ = 32.768 kHz operation) | | | | | |
| Instruction set | | • Data transfer (8/16 bits)<br>• Adder and subtractor/logical operation (8/16 bits)<br>• Multiplication (8 bits × 8 bits)<br>• Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. | | | | | |
| I/O port | Total | 74 | | 92 | | 120 | |
| | CMOS I/O | 64<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 21) | | 82<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 24) | | 110<br>(N-ch O.D. I/O [$EV_{DD}$ withstand voltage]: 25) | |
| | CMOS input | 5 | | 5 | | 5 | |
| | CMOS output | 1 | | 1 | | 1 | |
| | N-ch O.D. I/O (withstand voltage: 6 V) | 4 | | 4 | | 4 | |
| Timer | 16-bit timer | 12 channels | | 12 channels | | 16 channels | |
| | Watchdog timer | 1 channel | | 1 channel | | 1 channel | |
| | Real-time clock (RTC) | 1 channel | | 1 channel | | 1 channel | |
| | 12-bit interval timer (IT) | 1 channel | | 1 channel | | 1 channel | |
| | Timer output | 12 channels<br>(PWM outputs: 10 Note 2) | | 12 channels<br>(PWM outputs: 10 Note 2) | | 16 channels<br>(PWM outputs: 14 Note 2) | |
| | RTC output | 1 channel<br>• 1 Hz (subsystem clock: $f_{SUB}$ = 32.768 kHz) | | | | | |

**Notes 1.** The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F100xJ, R5F101xJ (x = M, P): Start address FAF00H
R5F100xL, R5F101xL (x = M, P, S): Start address F7F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

## 2.2 Oscillator Characteristics

### 2.2.1 X1, XT1 oscillator characteristics

**($T_A$ = −40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)[Note] | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| | | 1.8 V ≤ $V_{DD}$ < 2.4 V | 1.0 | | 8.0 | MHz |
| | | 1.6 V ≤ $V_{DD}$ < 1.8 V | 1.0 | | 4.0 | MHz |
| XT1 clock oscillation frequency ($f_X$)[Note] | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note** Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark** When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

### 2.2.2 On-chip oscillator characteristics

**($T_A$ = −40 to +85°C, 1.6 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency [Notes 1, 2] | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | −20 to +85 °C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | −1.0 | | +1.0 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | −5.0 | | +5.0 | % |
| | | −40 to −20 °C | 1.8 V ≤ $V_{DD}$ ≤ 5.5 V | −1.5 | | +1.5 | % |
| | | | 1.6 V ≤ $V_{DD}$ < 1.8 V | −5.5 | | +5.5 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | −15 | | +15 | % |

**Notes 1.** High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.** This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

## 2.3.2 Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**

**($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | $I_{DD1}$ | Operating mode | HS (high-speed main) mode [Note 5] | $f_{IH}$ = 32 MHz [Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 2.1 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.1 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 4.6 | 7.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.6 | 7.0 | mA |
| | | | | $f_{IH}$ = 24 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 3.7 | 5.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.7 | 5.5 | mA |
| | | | | $f_{IH}$ = 16 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 2.7 | 4.0 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.7 | 4.0 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{IH}$ = 8 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.2 | 1.8 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.8 | mA |
| | | | LV (low-voltage main) mode [Note 5] | $f_{IH}$ = 4 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.2 | 1.7 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.2 | 1.7 | mA |
| | | | HS (high-speed main) mode [Note 5] | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | mA |
| | | | | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.0 | 4.6 | mA |
| | | | | | | Resonator connection | | 3.2 | 4.8 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.9 | 2.7 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.7 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | mA |
| | | | | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.1 | 1.7 | mA |
| | | | | | | Resonator connection | | 1.1 | 1.7 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = –40°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +25°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +50°C | Normal operation | Square wave input | | 4.2 | 5.5 | μA |
| | | | | | | Resonator connection | | 4.3 | 5.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +70°C | Normal operation | Square wave input | | 4.3 | 6.3 | μA |
| | | | | | | Resonator connection | | 4.4 | 6.4 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +85°C | Normal operation | Square wave input | | 4.6 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.7 | 7.8 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$ and $EV_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$ or $V_{SS}$, $EV_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 32 MHz
2.4 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V $\leq V_{DD} \leq$ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

### (3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

### ($T_A$ = –40 to +85°C, 1.6 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (1/2)

| Parameter | Symbol | Conditions | | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | $I_{DD1}$ | Operating mode | HS (high-speed main) mode [Note 5] | $f_{IH}$ = 32 MHz [Note 3] | Basic operation | $V_{DD}$ = 5.0 V | | 2.6 | | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 2.6 | | mA |
| | | | | | Normal operation | $V_{DD}$ = 5.0 V | | 6.1 | 9.5 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 6.1 | 9.5 | mA |
| | | | | $f_{IH}$ = 24 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 4.8 | 7.4 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 4.8 | 7.4 | mA |
| | | | | $f_{IH}$ = 16 MHz [Note 3] | Normal operation | $V_{DD}$ = 5.0 V | | 3.5 | 5.3 | mA |
| | | | | | | $V_{DD}$ = 3.0 V | | 3.5 | 5.3 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{IH}$ = 8 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.3 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.3 | mA |
| | | | LV (low-voltage main) mode [Note 5] | $f_{IH}$ = 4 MHz [Note 3] | Normal operation | $V_{DD}$ = 3.0 V | | 1.5 | 2.0 | mA |
| | | | | | | $V_{DD}$ = 2.0 V | | 1.5 | 2.0 | mA |
| | | | HS (high-speed main) mode [Note 5] | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 20 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.9 | 6.1 | mA |
| | | | | | | Resonator connection | | 4.1 | 6.3 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 5.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | | $f_{MX}$ = 10 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 2.5 | 3.7 | mA |
| | | | | | | Resonator connection | | 2.5 | 3.7 | mA |
| | | | LS (low-speed main) mode [Note 5] | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | | $f_{MX}$ = 8 MHz [Note 2], $V_{DD}$ = 2.0 V | Normal operation | Square wave input | | 1.4 | 2.2 | mA |
| | | | | | | Resonator connection | | 1.4 | 2.2 | mA |
| | | | Subsystem clock operation | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = –40°C | Normal operation | Square wave input | | 5.4 | 6.5 | μA |
| | | | | | | Resonator connection | | 5.5 | 6.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +25°C | Normal operation | Square wave input | | 5.5 | 6.5 | μA |
| | | | | | | Resonator connection | | 5.6 | 6.6 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +50°C | Normal operation | Square wave input | | 5.6 | 9.4 | μA |
| | | | | | | Resonator connection | | 5.7 | 9.5 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +70°C | Normal operation | Square wave input | | 5.9 | 12.0 | μA |
| | | | | | | Resonator connection | | 6.0 | 12.1 | μA |
| | | | | $f_{SUB}$ = 32.768 kHz [Note 4] $T_A$ = +85°C | Normal operation | Square wave input | | 6.6 | 16.3 | μA |
| | | | | | | Resonator connection | | 6.7 | 16.4 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to $V_{DD}$, $EV_{DD0}$, and $EV_{DD1}$, or $V_{SS}$, $EV_{SS0}$, and $EV_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ $V_{DD}$ ≤ 5.5 V @1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ $V_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz

**Remarks 1.** $f_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

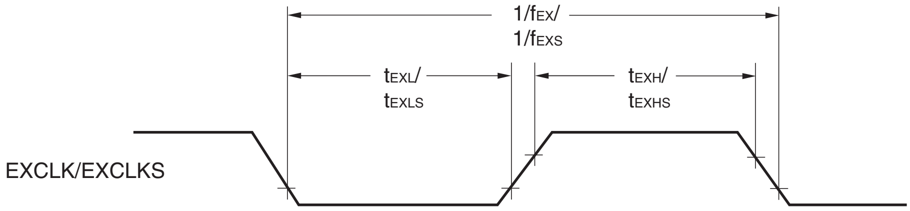
**2.** $f_{IH}$: High-speed on-chip oscillator clock frequency

**3.** $f_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

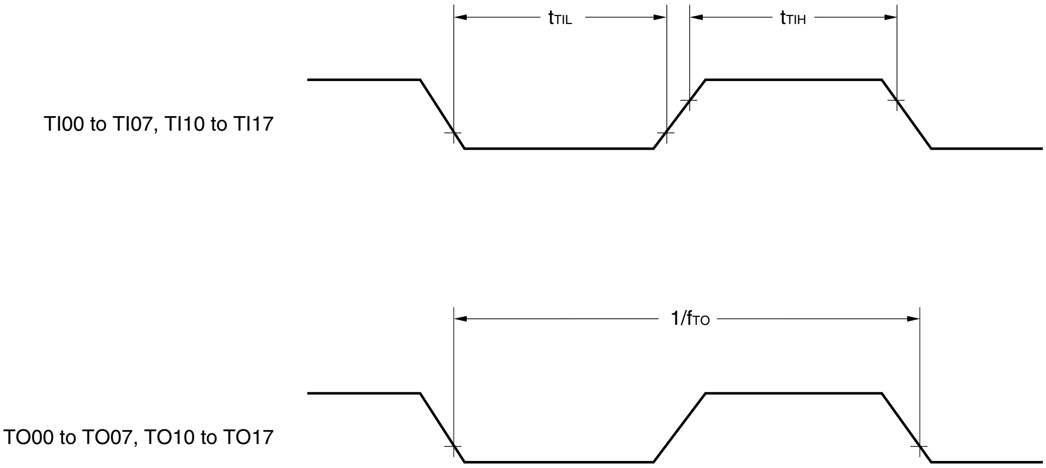
**4.** Except subsystem clock operation, temperature condition of the TYP. value is $T_A$ = 25°C

**AC Timing Test Points**

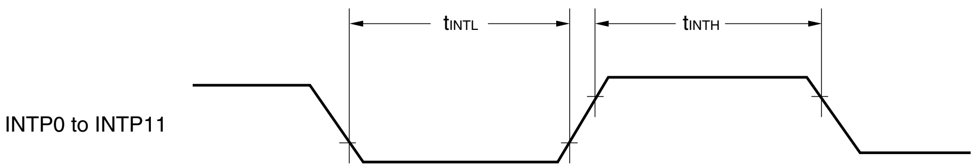

**External System Clock Timing**



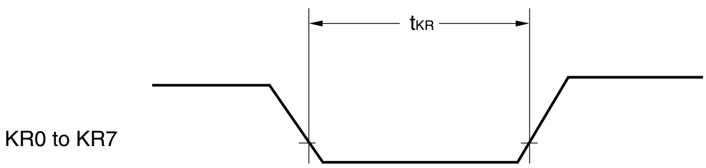

**TI/TO Timing**



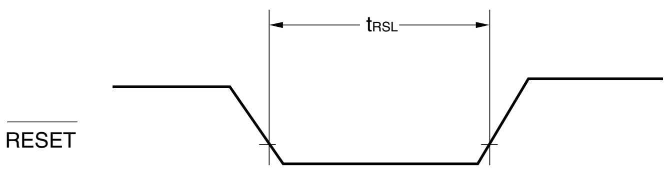

**Interrupt Request Input Timing**



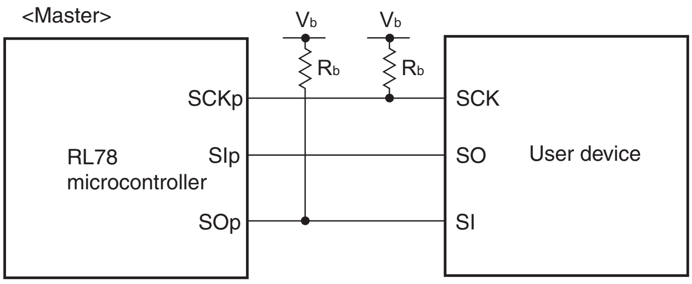

**Key Interrupt Input Timing**




**RESET Input Timing**



**CSI mode connection diagram (during communication at different potential)**



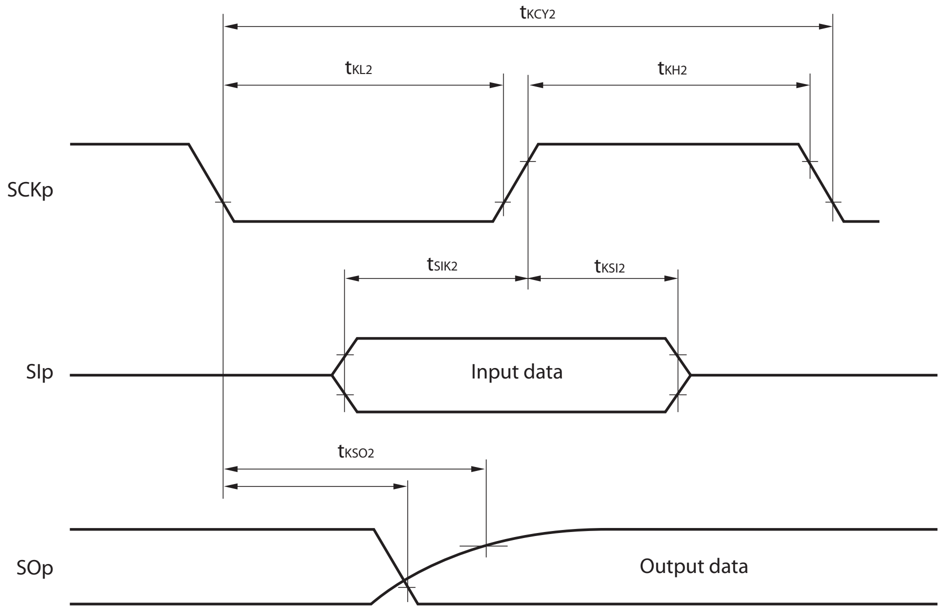

**Remarks 1.** $R_b$[Ω]:Communication line (SCKp, SOp) pull-up resistance, $C_b$[F]: Communication line (SCKp, SOp) load capacitance, $V_b$[V]: Communication line voltage

**2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number , n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

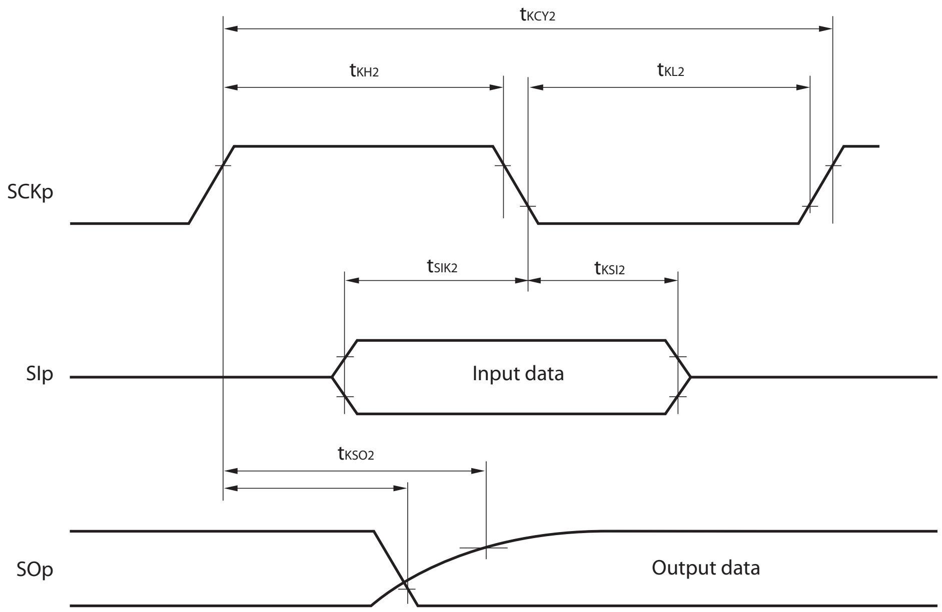
**3.** $f_{MCK}$: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

**4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**




**CSI mode serial transfer timing (slave mode) (during communication at different potential)**
**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**




**Remarks 1.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

**2.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (4/5)**

| Items | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Output voltage, high | $V_{OH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –3.0 mA | $EV_{DD0}$ – 0.7 | | | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –2.0 mA | $EV_{DD0}$ – 0.6 | | | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OH1}$ = –1.5 mA | $EV_{DD0}$ – 0.5 | | | V |
| | $V_{OH2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OH2}$ = –100 μA | $V_{DD}$ – 0.5 | | | V |
| Output voltage, low | $V_{OL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 8.5 mA | | | 0.7 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 3.0 mA | | | 0.6 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 1.5 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL1}$ = 0.6 mA | | | 0.4 | V |
| | $V_{OL2}$ | P20 to P27, P150 to P156 | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $I_{OL2}$ = 400 μA | | | 0.4 | V |
| | $V_{OL3}$ | P60 to P63 | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 15.0 mA | | | 2.0 | V |
| | | | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 5.0 mA | | | 0.4 | V |
| | | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 3.0 mA | | | 0.4 | V |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V, $I_{OL3}$ = 2.0 mA | | | 0.4 | V |

**Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

**Remark** Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

**(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**
**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | HS (high-speed main) Mode MIN. | HS (high-speed main) Mode MAX. | Unit |
|---|---|---|---|---|---|---|
| SCKp cycle time Note 5 | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | 20 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 20 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | 16 MHz < $f_{MCK}$ | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 16 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 16/$f_{MCK}$ | | ns |
| | | | | 12/$f_{MCK}$ and 1000 | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 14 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 16 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | $t_{KCY2}$/2 – 36 | | ns |
| SIp setup time (to SCKp↑) Note 1 | $t_{SIK2}$ | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+60 | | ns |
| SIp hold time (from SCKp↑) Note 2 | $t_{KSI2}$ | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 1/$f_{MCK}$+62 | | ns |
| Delay time from SCKp↓ to SOp output Note 3 | $t_{KSO2}$ | C = 30 pF Note 4 | 2.7 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+66 | ns |
| | | | 2.4 V ≤ $EV_{DD0}$ ≤ 5.5 V | | 2/$f_{MCK}$+113 | ns |

**Notes 1.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** C is the load capacitance of the SOp output lines.

**5.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

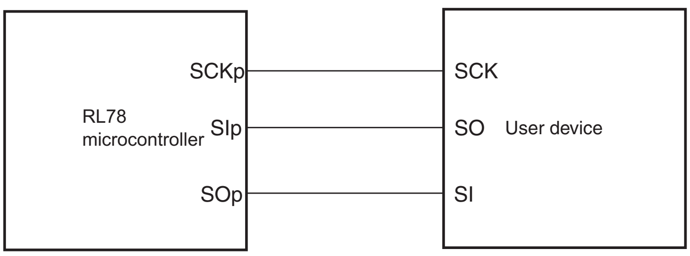
**Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**Remarks 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

**2.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

**CSI mode connection diagram (during communication at same potential)**



**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)**

**($T_A$ = −40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| SIp setup time (to SCKp↑) Note | $t_{SIK1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 162 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 354 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | 958 | | ns |
| SIp hold time (from SCKp↑) Note | $t_{KSI1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | 38 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | 38 | | ns |
| Delay time from SCKp↓ to SOp output Note | $t_{KSO1}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 200 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 390 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V, $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 966 | ns |

**Note** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

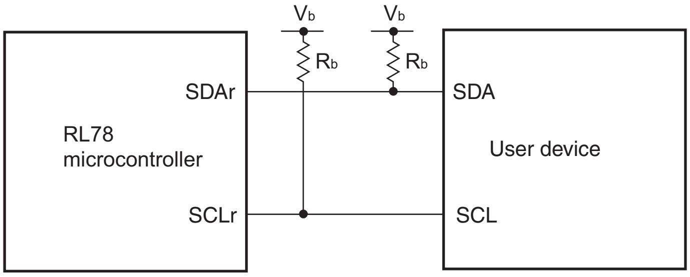
**(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**

**($T_A$ = –40 to +105°C, 2.4 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V)**

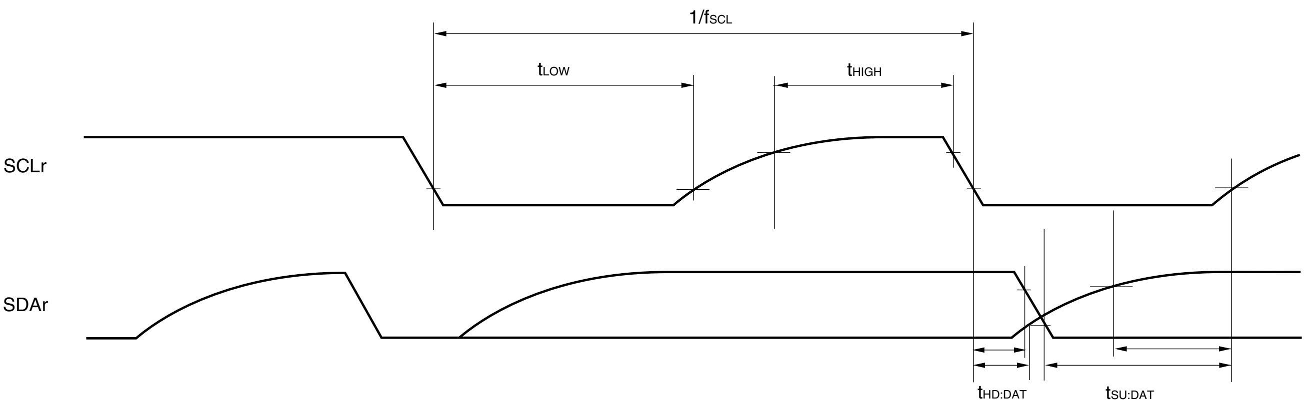
| Parameter | Symbol | Conditions | | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|---|
| | | | | MIN. | MAX. | |
| SCKp cycle time [Note 1] | $t_{KCY2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 24 MHz < $f_{MCK}$ | 28/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 24/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 20 MHz | 20/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 24 MHz < $f_{MCK}$ | 40/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 32/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 28/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 24/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 16/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 12/$f_{MCK}$ | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | 24 MHz < $f_{MCK}$ | 96/$f_{MCK}$ | | ns |
| | | | 20 MHz < $f_{MCK}$ ≤ 24 MHz | 72/$f_{MCK}$ | | ns |
| | | | 16 MHz < $f_{MCK}$ ≤ 20 MHz | 64/$f_{MCK}$ | | ns |
| | | | 8 MHz < $f_{MCK}$ ≤ 16 MHz | 52/$f_{MCK}$ | | ns |
| | | | 4 MHz < $f_{MCK}$ ≤ 8 MHz | 32/$f_{MCK}$ | | ns |
| | | | $f_{MCK}$ ≤ 4 MHz | 20/$f_{MCK}$ | | ns |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | $t_{KCY2}$/2 – 24 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | $t_{KCY2}$/2 – 36 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2] | | $t_{KCY2}$/2 – 100 | | ns |
| SIp setup time (to SCKp↑) [Note2] | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | | 1/$f_{MCK}$ + 40 | | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V | | 1/$f_{MCK}$ + 60 | | ns |
| SIp hold time (from SCKp↑) [Note 3] | $t_{KSI2}$ | | | 1/$f_{MCK}$ + 62 | | ns |
| Delay time from SCKp↓ to SOp output [Note 4] | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | | 2/$f_{MCK}$ + 240 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | | 2/$f_{MCK}$ + 428 | ns |
| | | 2.4 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | | 2/$f_{MCK}$ + 1146 | ns |

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

**Simplified I²C mode connection diagram (during communication at different potential)**




**Simplified I²C mode serial transfer timing (during communication at different potential)**




**Caution** **Select the TTL input buffer and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**Remarks 1.** $R_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, $C_b$[F]: Communication line (SDAr, SCLr) load capacitance, $V_b$[V]: Communication line voltage

**2.** r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

**3.** $f_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13)

**Notes 1.** Excludes quantization error (±1/2 LSB).

**2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**3.** When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

**4.** Refer to **3.6.2 Temperature sensor/internal reference voltage characteristics**.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.