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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| Details | |
| --- | --- |
| Product Status | Obsolete |
| Core Processor | RL78 |
| Core Size | 16-Bit |
| Speed | 32MHz |
| Connectivity | CSI, I²C, LINbus, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 34 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.6V ~ 5.5V |
| Data Converters | A/D 10x8/10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-LQFP |
| Supplier Device Package | 48-LFQFP (7x7) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gcafb-x0 |

**Table 1-1.  List of Ordering Part Numbers**

(6/12)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 48 pins | 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch) | Mounted | A | R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 <br> R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0 |
| | | | D | R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 <br> R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0 |
| | | | G | R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 <br> R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0 |
| | | Not mounted | A | R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 <br> R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0 |
| | | | D | R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 <br> R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0 |

**Note**    For the fields of application, refer to **Figure 1-1  Part Number, Memory Size, and Package of RL78/G13**.

**Caution  The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.**

**Table 1-1.  List of Ordering Part Numbers**

(12/12)

| Pin count | Package | Data flash | Fields of Application Note | Ordering Part Number |
|---|---|---|---|---|
| 128 pins | 128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch) | Mounted | A | R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0 |
| | | | D | R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0 |
| | | Not mounted | A | R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0 |
| | | | D | R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0 |

**Note**      For the fields of application, refer to **Figure 1-1  Part Number, Memory Size, and Package of RL78/G13**.

**Caution  The ordering part numbers represent the numbers at the time of publication. For the latest ordering**

**part numbers, refer to the target product page of the Renesas Electronics website.**

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)
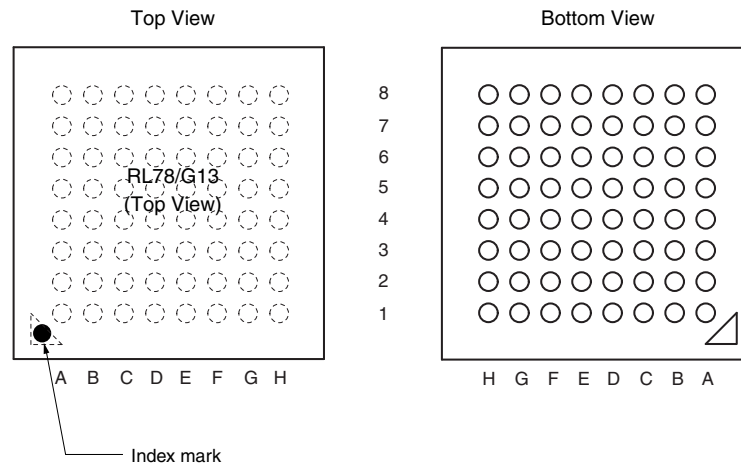


| Pin No. | Name | Pin No. | Name | Pin No. | Name | Pin No. | Name |
|---|---|---|---|---|---|---|---|
| A1 | P05/TI05/TO05 | C1 | P51/INTP2/SO11 | E1 | P13/TxD2/SO20/ (SDAA0)/(TI04)/(TO04) | G1 | P146 |
| A2 | P30/INTP3/RTC1HZ /SCK11/SCL11 | C2 | P71/KR1/SI21/SDA21 | E2 | P14/RxD2/SI20/SDA20 /(SCLA0)/(TI03)/(TO03) | G2 | P25/ANI5 |
| A3 | P70/KR0/SCK21 /SCL21 | C3 | P74/KR4/INTP8/SI01 /SDA01 | E3 | P15/SCK20/SCL20/ (TI02)/(TO02) | G3 | P24/ANI4 |
| A4 | P75/KR5/INTP9 /SCK01/SCL01 | C4 | P52/(INTP10) | E4 | P16/TI01/TO01/INTP5 /(SI00)/(RxD0) | G4 | P22/ANI2 |
| A5 | P77/KR7/INTP11/ (TxD2) | C5 | P53/(INTP11) | E5 | P03/ANI16/SI10/RxD1 /SDA10 | G5 | P130 |
| A6 | P61/SDAA0 | C6 | P63 | E6 | P41/TI07/TO07 | G6 | P02/ANI17/SO10/TxD1 |
| A7 | P60/SCLA0 | C7 | $V_{SS}$ | E7 | $\overline{RESET}$ | G7 | P00/TI00 |
| A8 | $EV_{DD0}$ | C8 | P121/X1 | E8 | P137/INTP0 | G8 | P124/XT2/EXCLKS |
| B1 | P50/INTP1/SI11 /SDA11 | D1 | P55/(PCLBUZ1)/ (SCK00) | F1 | P10/SCK00/SCL00/ (TI07)/(TO07) | H1 | P147/ANI18 |
| B2 | P72/KR2/SO21 | D2 | P06/TI06/TO06 | F2 | P11/SI00/RxD0 /TOOLRxD/SDA00/ (TI06)/(TO06) | H2 | P27/ANI7 |
| B3 | P73/KR3/SO01 | D3 | P17/TI02/TO02/ (SO00)/(TxD0) | F3 | P12/SO00/TxD0 /TOOLTxD/(INTP5)/ (TI05)/(TO05) | H3 | P26/ANI6 |
| B4 | P76/KR6/INTP10/ (RxD2) | D4 | P54 | F4 | P21/ANI1/$AV_{REFM}$ | H4 | P23/ANI3 |
| B5 | P31/TI03/TO03 /INTP4/(PCLBUZ0) | D5 | P42/TI04/TO04 | F5 | P04/SCK10/SCL10 | H5 | P20/ANI0/$AV_{REFP}$ |
| B6 | P62 | D6 | P40/TOOL0 | F6 | P43 | H6 | P141/PCLBUZ1/INTP7 |
| B7 | $V_{DD}$ | D7 | REGC | F7 | P01/TO00 | H7 | P140/PCLBUZ0/INTP6 |
| B8 | $EV_{SS0}$ | D8 | P122/X2/EXCLK | F8 | P123/XT1 | H8 | P120/ANI19 |

**Cautions 1. Make $EV_{SS0}$ pin the same potential as $V_{SS}$ pin.**

**2. Make $V_{DD}$ pin the potential that is higher than $EV_{DD0}$ pin.**

**3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 $\mu$F).**

**Remarks 1.** For pin identification, see **1.4 Pin Identification**.

**2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the $V_{DD}$ and $EV_{DD0}$ pins and connect the $V_{SS}$ and $EV_{SS0}$ pins to separate ground lines.

**3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

## 1.5.4  30-pin products
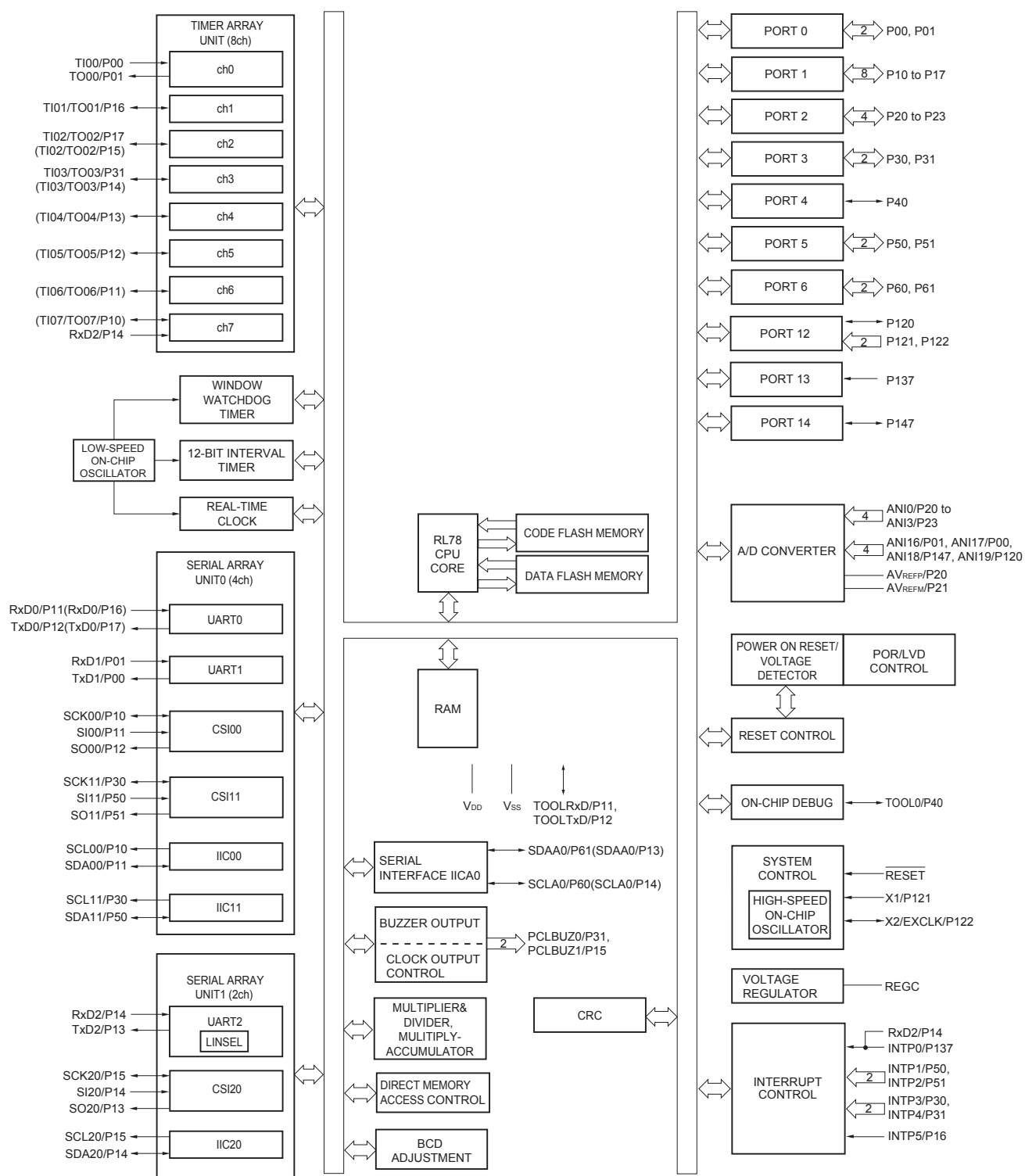


**Remark**  Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).  Refer to **Figure 4-8  Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (5/5)**

| Items | Symbol | Conditions | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|
| Input leakage current, high | I$_{LIH1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | V$_I$ = EV$_{DD0}$ | | | | 1 | μA |
| | I$_{LIH2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | V$_I$ = V$_{DD}$ | | | | 1 | μA |
| | I$_{LIH3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | V$_I$ = V$_{DD}$ | In input port or external clock input | | | 1 | μA |
| | | | | In resonator connection | | | 10 | μA |
| Input leakage current, low | I$_{LIL1}$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | V$_I$ = EV$_{SS0}$ | | | | −1 | μA |
| | I$_{LIL2}$ | P20 to P27, P137, P150 to P156, $\overline{RESET}$ | V$_I$ = V$_{SS}$ | | | | −1 | μA |
| | I$_{LIL3}$ | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS) | V$_I$ = V$_{SS}$ | In input port or external clock input | | | −1 | μA |
| | | | | In resonator connection | | | −10 | μA |
| On-chip pll-up resistance | R$_U$ | P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147 | V$_I$ = EV$_{SS0}$, In input port | | 10 | 20 | 100 | kΩ |

**Remark**  Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

## (4) Peripheral Functions (Common to all products)

**(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Low-speed on-chip oscillator operating current | I$_{FIL}$ [Note 1] | | | | 0.20 | | μA |
| RTC operating current | I$_{RTC}$ [Notes 1, 2, 3] | | | | 0.02 | | μA |
| 12-bit interval timer operating current | I$_{IT}$ [Notes 1, 2, 4] | | | | 0.02 | | μA |
| Watchdog timer operating current | I$_{WDT}$ [Notes 1, 2, 5] | f$_{IL}$ = 15 kHz | | | 0.22 | | μA |
| A/D converter operating current | I$_{ADC}$ [Notes 1, 6] | When conversion at maximum speed | Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V | | 1.3 | 1.7 | mA |
| | | | Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V | | 0.5 | 0.7 | mA |
| A/D converter reference voltage current | I$_{ADREF}$ [Note 1] | | | | 75.0 | | μA |
| Temperature sensor operating current | I$_{TMPS}$ [Note 1] | | | | 75.0 | | μA |
| LVD operating current | I$_{LVI}$ [Notes 1, 7] | | | | 0.08 | | μA |
| Self-programming operating current | I$_{FSP}$ [Notes 1, 9] | | | | 2.50 | 12.20 | mA |
| BGO operating current | I$_{BGO}$ [Notes 1, 8] | | | | 2.50 | 12.20 | mA |
| SNOOZE operating current | I$_{SNOZ}$ [Note 1] | ADC operation | The mode is performed [Note 10] | | 0.50 | 0.60 | mA |
| | | | The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V | | 1.20 | 1.44 | mA |
| | | CSI/UART operation | | | 0.70 | 0.84 | mA |

**Notes  1.** Current flowing to V$_{DD}$.

**2.** When high speed on-chip oscillator and high-speed system clock are stopped.

**3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator).  The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.  I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

**4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator).  The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode.  When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

**5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator).  The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

**(5)  During communication at same potential (simplified I$^2$C mode) (1/2)**

**(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCLr clock frequency | f$_{SCL}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | | 1000 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ | | 400 Note 1 | | 400 Note 1 | | 400 Note 1 | kHz |
| | | 1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | | 300 Note 1 | | 300 Note 1 | | 300 Note 1 | kHz |
| | | 1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | | 250 Note 1 | | 250 Note 1 | | 250 Note 1 | kHz |
| | | 1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | | — | | 250 Note 1 | | 250 Note 1 | kHz |
| Hold time when SCLr = "L" | t$_{LOW}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |
| Hold time when SCLr = "H" | t$_{HIGH}$ | 2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 475 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ | 1150 | | 1150 | | 1150 | | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | 1550 | | 1550 | | 1550 | | ns |
| | | 1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | 1850 | | 1850 | | 1850 | | ns |
| | | 1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ | — | | 1850 | | 1850 | | ns |

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

**3.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V $\leq$ $EV_{DD0}$ < 4.0 V and 2.3 V $\leq$ $V_b$ $\leq$ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

**4.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

**5.** Use it with $EV_{DD0} \geq V_b$.

**6.** The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V $\leq$ $EV_{DD0}$ < 3.3 V and 1.6 V $\leq$ $V_b$ $\leq$ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

   * This value is the theoretical value of the relative difference between the transmission and reception sides.

**7.** This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to Note 6 above to calculate the maximum transfer rate under conditions of the customer.

**Caution**   **Select the TTL input buffer for the RxDq pin and the N-ch open drain output ($V_{DD}$ tolerance (When 20- to 52-pin products)/$EV_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**UART mode connection diagram (during communication at different potential)**
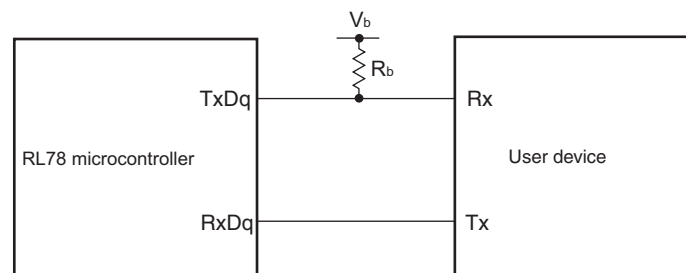
**(9) Communication at different potential (1.8 V, 2.5 V, 3 V)　(CSI mode) (slave mode, SCKp... external clock input)**

($T_A$ = –40 to +85°C, 1.8 V ≤ $EV_{DD0}$ = $EV_{DD1}$ ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = $EV_{SS0}$ = $EV_{SS1}$ = 0 V) (2/2)

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| SCKp high-/low-level width | $t_{KH2}$, $t_{KL2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | $t_{KCY2}$/2 − 12 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | $t_{KCY2}$/2 − 18 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2] | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | $t_{KCY2}$/2 − 50 | | ns |
| SIp setup time (to SCKp↑) [Note 3] | $t_{SIK2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V | 1/$f_{MCK}$ + 20 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2] | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | 1/$f_{MCK}$ + 30 | | ns |
| SIp hold time (from SCKp↑) [Note 4] | $t_{KSI2}$ | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | 1/$f_{MCK}$ + 31 | | ns |
| Delay time from SCKp↓ to SOp output [Note 5] | $t_{KSO2}$ | 4.0 V ≤ $EV_{DD0}$ ≤ 5.5 V, 2.7 V ≤ $V_b$ ≤ 4.0 V, $C_b$ = 30 pF, $R_b$ = 1.4 kΩ | | 2/$f_{MCK}$ + 120 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 2.7 V ≤ $EV_{DD0}$ < 4.0 V, 2.3 V ≤ $V_b$ ≤ 2.7 V, $C_b$ = 30 pF, $R_b$ = 2.7 kΩ | | 2/$f_{MCK}$ + 214 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |
| | | 1.8 V ≤ $EV_{DD0}$ < 3.3 V, 1.6 V ≤ $V_b$ ≤ 2.0 V [Note 2], $C_b$ = 30 pF, $R_b$ = 5.5 kΩ | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | | 2/$f_{MCK}$ + 573 | ns |

**Notes　1.** Transfer rate in the SNOOZE mode : MAX. 1 Mbps

**2.** Use it with $EV_{DD0}$ ≥ $V_b$.

**3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.　The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.　The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**5.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.　The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution　Select the TTL input buffer for the SIp pin and the N-ch open drain output ($V_{DD}$ tolerance (for the 20- to 52-pin products)/$EV_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For $V_{IH}$ and $V_{IL}$, see the DC characteristics with TTL input buffer selected.**

**(Remarks** are listed on the next page.)

**(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I$^2$C mode) (2/2)**

**(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | LS (low-speed main) Mode | | LV (low-voltage main) Mode | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Data setup time (reception) | t$_{SU:DAT}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 1/f$_{MCK}$ + 135 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | kHz |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 1/f$_{MCK}$ + 135 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | kHz |
| | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | kHz |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | kHz |
| | | 1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | 1/f$_{MCK}$ + 190 [Note 3] | | kHz |
| Data hold time (transmission) | t$_{HD:DAT}$ | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ | 0 | 305 | 0 | 305 | 0 | 305 | ns |
| | | 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ | 0 | 355 | 0 | 355 | 0 | 355 | ns |
| | | 1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ | 0 | 405 | 0 | 405 | 0 | 405 | ns |

**Notes 1.** The value must also be equal to or less than f$_{MCK}$/4.

     **2.** Use it with EV$_{DD0}$ ≥ V$_b$.

     **3.** Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

**Caution**   **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

### 3.2  Oscillator Characteristics

#### 3.2.1  X1, XT1 oscillator characteristics

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Parameter | Resonator | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| X1 clock oscillation frequency ($f_X$)[Note] | Ceramic resonator/ crystal resonator | 2.7 V ≤ $V_{DD}$ ≤ 5.5 V | 1.0 | | 20.0 | MHz |
| | | 2.4 V ≤ $V_{DD}$ < 2.7 V | 1.0 | | 16.0 | MHz |
| XT1 clock oscillation frequency ($f_X$)[Note] | Crystal resonator | | 32 | 32.768 | 35 | kHz |

**Note**  Indicates only permissible oscillator frequency ranges.  Refer to AC Characteristics for instruction execution time.  Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

**Caution**  **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

**Remark**  When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

#### 3.2.2  On-chip oscillator characteristics

**($T_A$ = −40 to +105°C, 2.4 V ≤ $V_{DD}$ ≤ 5.5 V, $V_{SS}$ = 0 V)**

| Oscillators | Parameters | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| High-speed on-chip oscillator clock frequency[Notes 1, 2] | $f_{IH}$ | | | 1 | | 32 | MHz |
| High-speed on-chip oscillator clock frequency accuracy | | −20 to +85 °C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | −1.0 | | +1.0 | % |
| | | −40 to −20 °C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | −1.5 | | +1.5 | % |
| | | +85 to +105 °C | 2.4 V ≤ $V_{DD}$ ≤ 5.5 V | −2.0 | | +2.0 | % |
| Low-speed on-chip oscillator clock frequency | $f_{IL}$ | | | | 15 | | kHz |
| Low-speed on-chip oscillator clock frequency accuracy | | | | −15 | | +15 | % |

**Notes 1.**  High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

**2.**  This indicates the oscillator characteristics only.  Refer to AC Characteristics for instruction execution time.

### 3.3.2  Supply current characteristics

**(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products**
**(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = 0 V) (1/2)**

| Parameter | Symbol | Conditions | | | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|---|---|
| Supply current [Note 1] | I$_{DD1}$ | Operating mode | HS (high-speed main) mode [Note 5] | f$_{IH}$ = 32 MHz [Note 3] | Basic operation | V$_{DD}$ = 5.0 V | | 2.1 | | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 2.1 | | mA |
| | | | | | Normal operation | V$_{DD}$ = 5.0 V | | 4.6 | 7.5 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 4.6 | 7.5 | mA |
| | | | | f$_{IH}$ = 24 MHz [Note 3] | Normal operation | V$_{DD}$ = 5.0 V | | 3.7 | 5.8 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 3.7 | 5.8 | mA |
| | | | | f$_{IH}$ = 16 MHz [Note 3] | Normal operation | V$_{DD}$ = 5.0 V | | 2.7 | 4.2 | mA |
| | | | | | | V$_{DD}$ = 3.0 V | | 2.7 | 4.2 | mA |
| | | | HS (high-speed main) mode [Note 5] | f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 5.0 V | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | | | f$_{MX}$ = 20 MHz [Note 2], V$_{DD}$ = 3.0 V | Normal operation | Square wave input | | 3.0 | 4.9 | mA |
| | | | | | | Resonator connection | | 3.2 | 5.0 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 5.0 V | Normal operation | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | mA |
| | | | | f$_{MX}$ = 10 MHz [Note 2], V$_{DD}$ = 3.0 V | Normal operation | Square wave input | | 1.9 | 2.9 | mA |
| | | | | | | Resonator connection | | 1.9 | 2.9 | mA |
| | | | Subsystem clock operation | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = −40°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +25°C | Normal operation | Square wave input | | 4.1 | 4.9 | μA |
| | | | | | | Resonator connection | | 4.2 | 5.0 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +50°C | Normal operation | Square wave input | | 4.2 | 5.5 | μA |
| | | | | | | Resonator connection | | 4.3 | 5.6 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +70°C | Normal operation | Square wave input | | 4.3 | 6.3 | μA |
| | | | | | | Resonator connection | | 4.4 | 6.4 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +85°C | Normal operation | Square wave input | | 4.6 | 7.7 | μA |
| | | | | | | Resonator connection | | 4.7 | 7.8 | μA |
| | | | | f$_{SUB}$ = 32.768 kHz [Note 4] T$_A$ = +105°C | Normal operation | Square wave input | | 6.9 | 19.7 | μA |
| | | | | | | Resonator connection | | 7.0 | 19.8 | μA |

(**Notes** and **Remarks** are listed on the next page.)

**Notes 1.** Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** When high-speed on-chip oscillator and subsystem clock are stopped.

**3.** When high-speed system clock and subsystem clock are stopped.

**4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 32 MHz

2.4 V ≤ V$_{DD}$ ≤ 5.5 V @ 1 MHz to 16 MHz

**Remarks 1.** f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** f$_{IH}$: High-speed on-chip oscillator clock frequency

**3.** f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

**Notes 1.** Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$.  The values below the MAX. column include the peripheral operation current.  However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

**2.** During HALT instruction execution by flash memory.

**3.** When high-speed on-chip oscillator and subsystem clock are stopped.

**4.** When high-speed system clock and subsystem clock are stopped.

**5.** When high-speed on-chip oscillator and high-speed system clock are stopped.  When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1).  The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

**6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

**7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

    HS (high-speed main) mode:  2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                   2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

**8.** Regarding the value for current operate the subsystem clock in STOP mode, refer to that in HALT mode.

**Remarks 1.** f$_{MX}$:   High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**2.** f$_{IH}$:   High-speed on-chip oscillator clock frequency

**3.** f$_{SUB}$:   Subsystem clock frequency (XT1 clock oscillation frequency)

**4.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

**TI/TO Timing**

TI00 to TI07, TI10 to TI17

$t_{TIL}$     $t_{TIH}$

TO00 to TO07, TO10 to TO17

$1/f_{TO}$
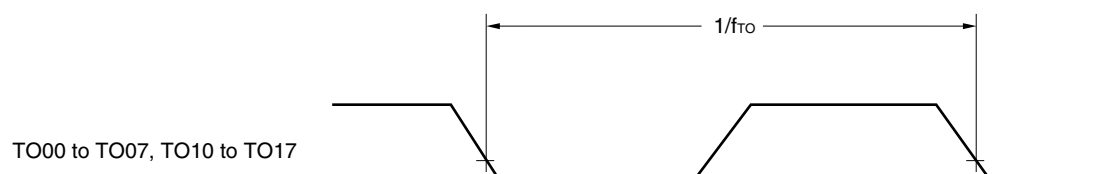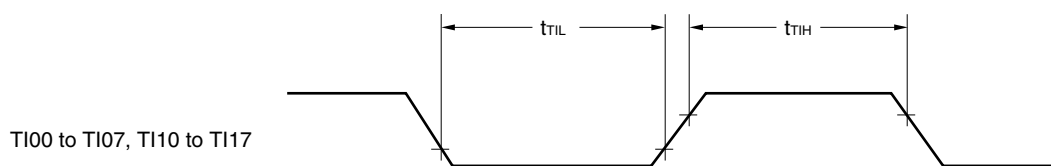
**Interrupt Request Input Timing**

INTP0 to INTP11

$t_{INTL}$     $t_{INTH}$
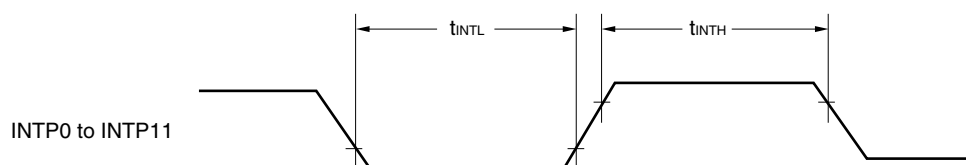
**Key Interrupt Input Timing**

KR0 to KR7

$t_{KR}$
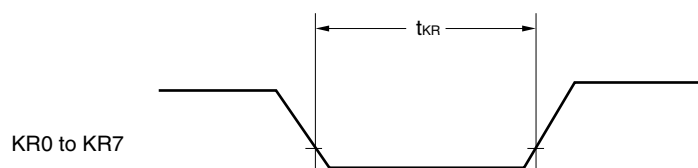
**$\overline{\text{RESET}}$ Input Timing**

$\overline{\text{RESET}}$

$t_{RSL}$
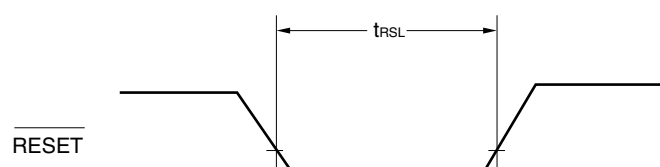
## 3.5 Peripheral Functions Characteristics

**AC Timing Test Points**
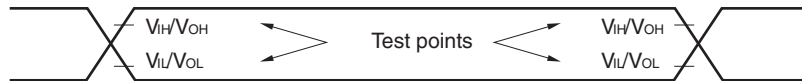


### 3.5.1 Serial array unit

**(1) During communication at same potential (UART mode)**

**(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)**

| Parameter | Symbol | Conditions | HS (high-speed main) Mode | | Unit |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| Transfer rate [Note 1] | | | | f$_{MCK}$/12 [Note 2] | bps |
| | | Theoretical value of the maximum transfer rate f$_{CLK}$ = 32 MHz, f$_{MCK}$ = f$_{CLK}$ | | 2.6 | Mbps |

**Notes 1.** Transfer rate in the SNOOZE mode is 4800 bps only.

    **2.** The following conditions are required for low voltage interface when E$_{VDD0}$ < V$_{DD}$.

       2.4 V ≤ EV$_{DD0}$ < 2.7 V : MAX. 1.3 Mbps

**Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

**UART mode connection diagram (during communication at same potential)**
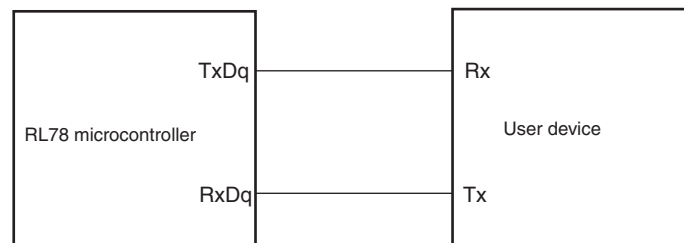


**UART mode bit width (during communication at same potential) (reference)**
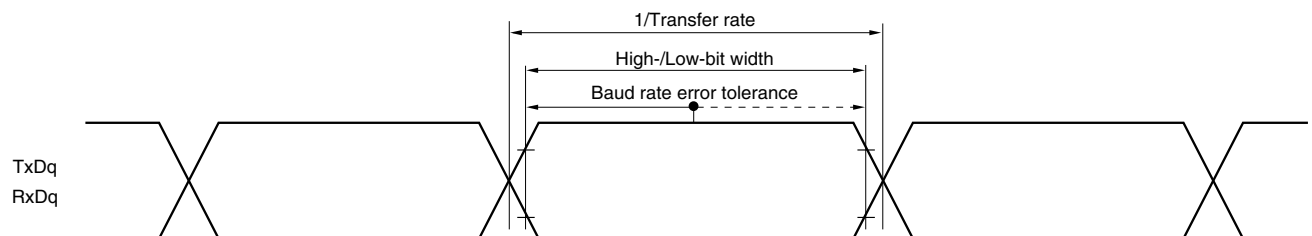


**Remarks 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

    **2.** f$_{MCK}$: Serial array unit operation clock frequency

       (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

       n: Channel number (mn = 00 to 03, 10 to 13))

### 3.6.3  POR circuit characteristics

**(T$_A$ = –40 to +105°C, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Detection voltage | V$_{POR}$ | Power supply rise time | 1.45 | 1.51 | 1.57 | V |
|  | V$_{PDR}$ | Power supply fall time | 1.44 | 1.50 | 1.56 | V |
| Minimum pulse width | T$_{PW}$ |  | 300 |  |  | $\mu$s |

**Note**  Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$.  This is also the minimum time
required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is
entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock
operation status control register (CSC).
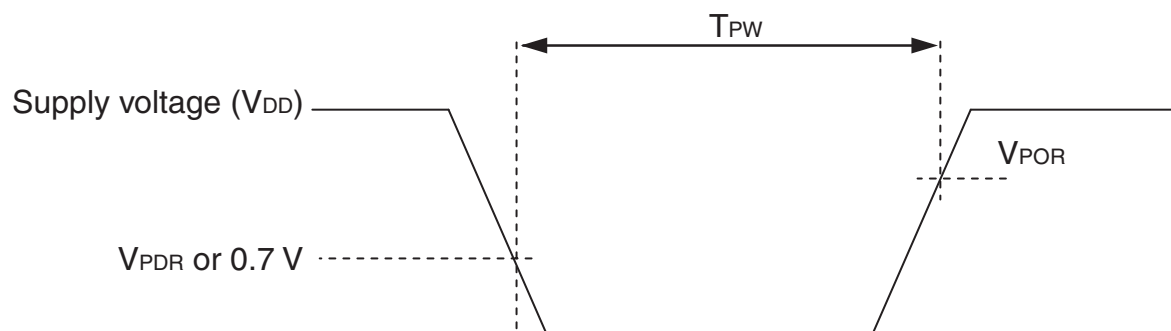
### 3.6.5  Power supply voltage rising slope characteristics

**(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage rising slope | S$_{VDD}$ | | | | 54 | V/ms |

**Caution**  **Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 3.4 AC Characteristics.**

### 3.7  RAM Data Retention Characteristics

**(T$_A$ = −40 to +105°C, V$_{SS}$ = 0 V)**

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| Data retention supply voltage | V$_{DDDR}$ | | 1.44[Note] | | 5.5 | V |

**Note**  This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.
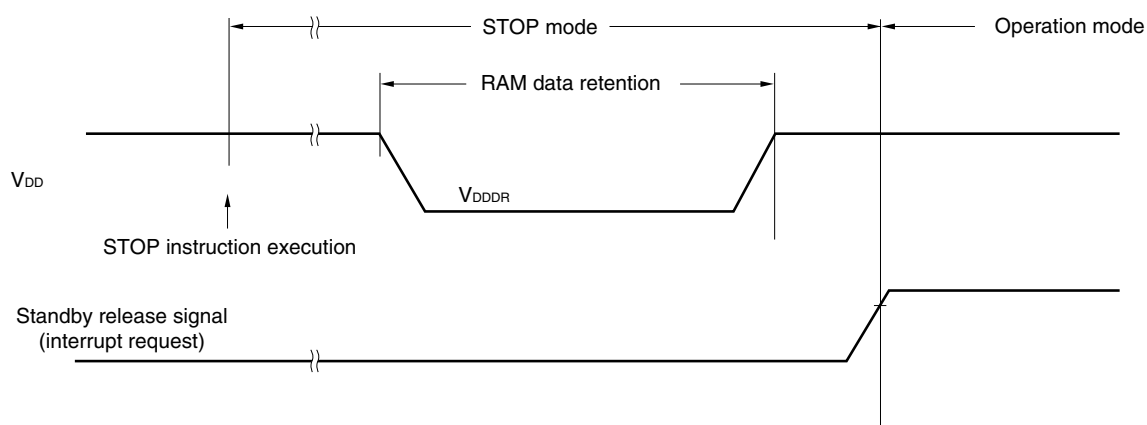
## 4.3  25-pin Products

R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA
R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA
R5F1008AGLA, R5F1008CGLA, R5F1008DGLA, R5F1008EGLA

| JEITA Package Code | RENESAS Code | Previous Code | MASS (TYP.) [g] |
|---|---|---|---|
| P-WFLGA25-3x3-0.50 | PWLG0025KA-A | P25FC-50-2N2-2 | 0.01 |



| (UNIT:mm) | |
|---|---|
| **ITEM** | **DIMENSIONS** |
| D | 3.00 ±0.10 |
| E | 3.00 ±0.10 |
| w | 0.20 |
| e | 0.50 |
| A | 0.69 ±0.07 |
| b | 0.24 ±0.05 |
| x | 0.05 |
| y | 0.08 |
| y1 | 0.20 |
| ZD | 0.50 |
| ZE | 0.50 |
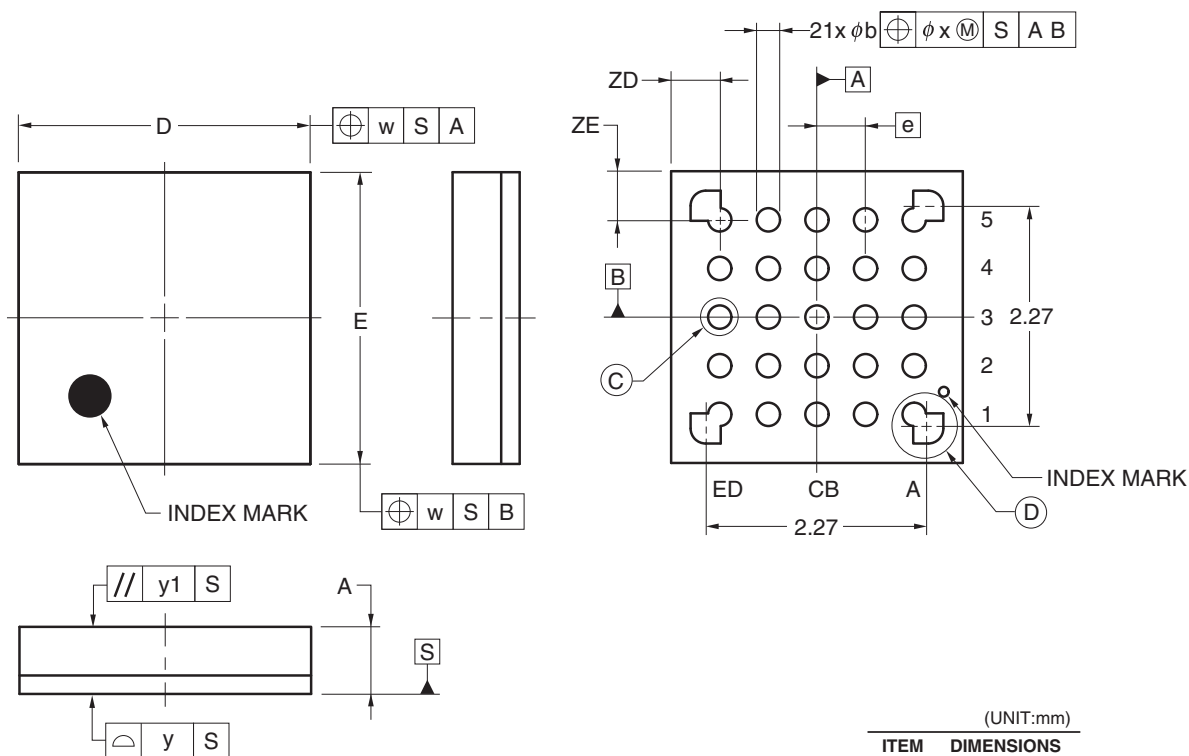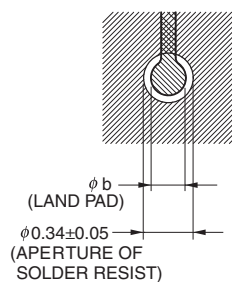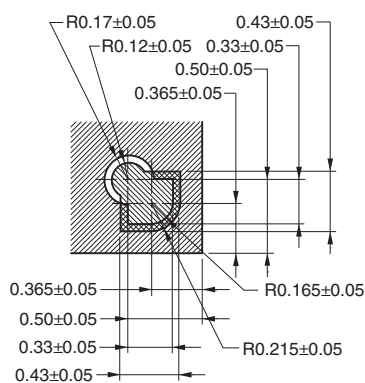
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