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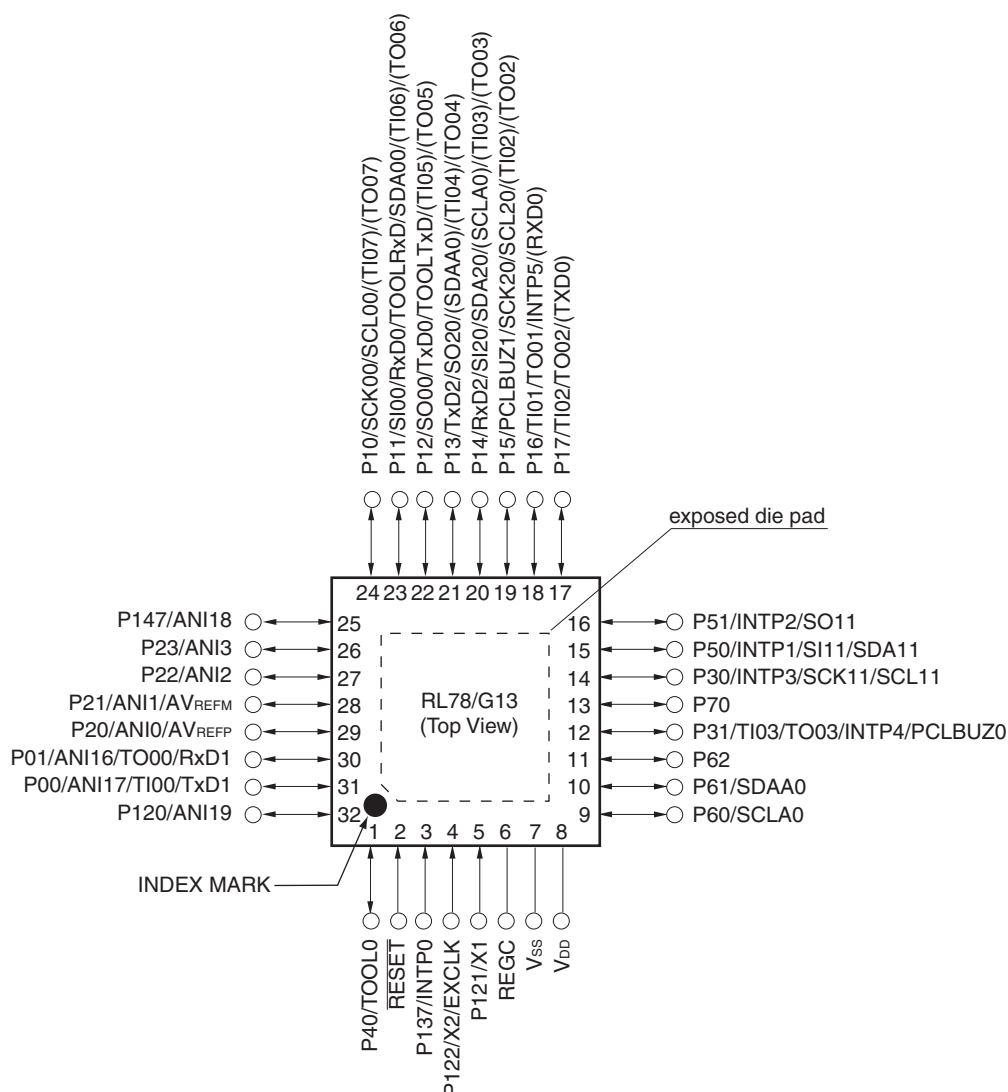
Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gcdfb-x0

1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)

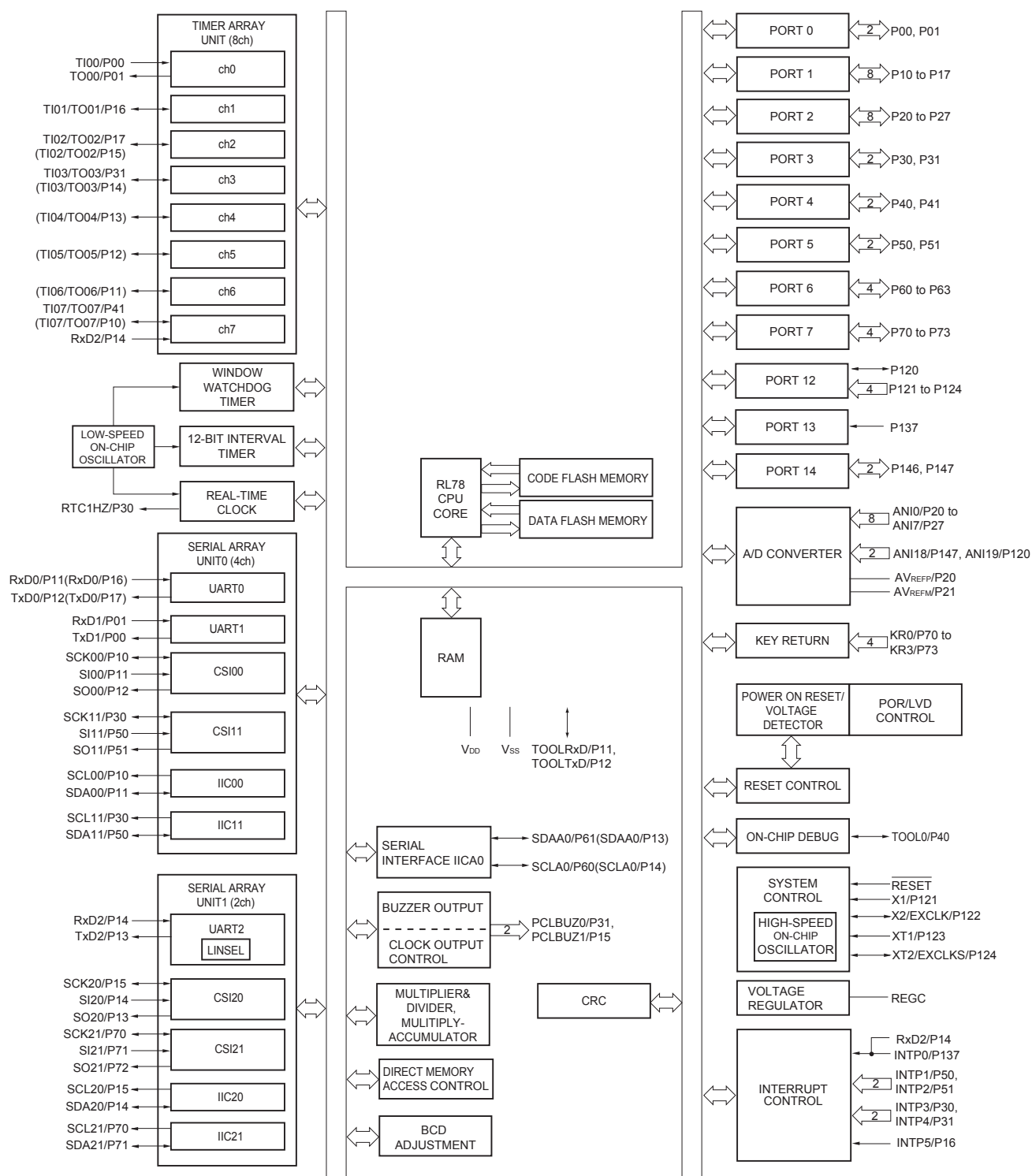


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

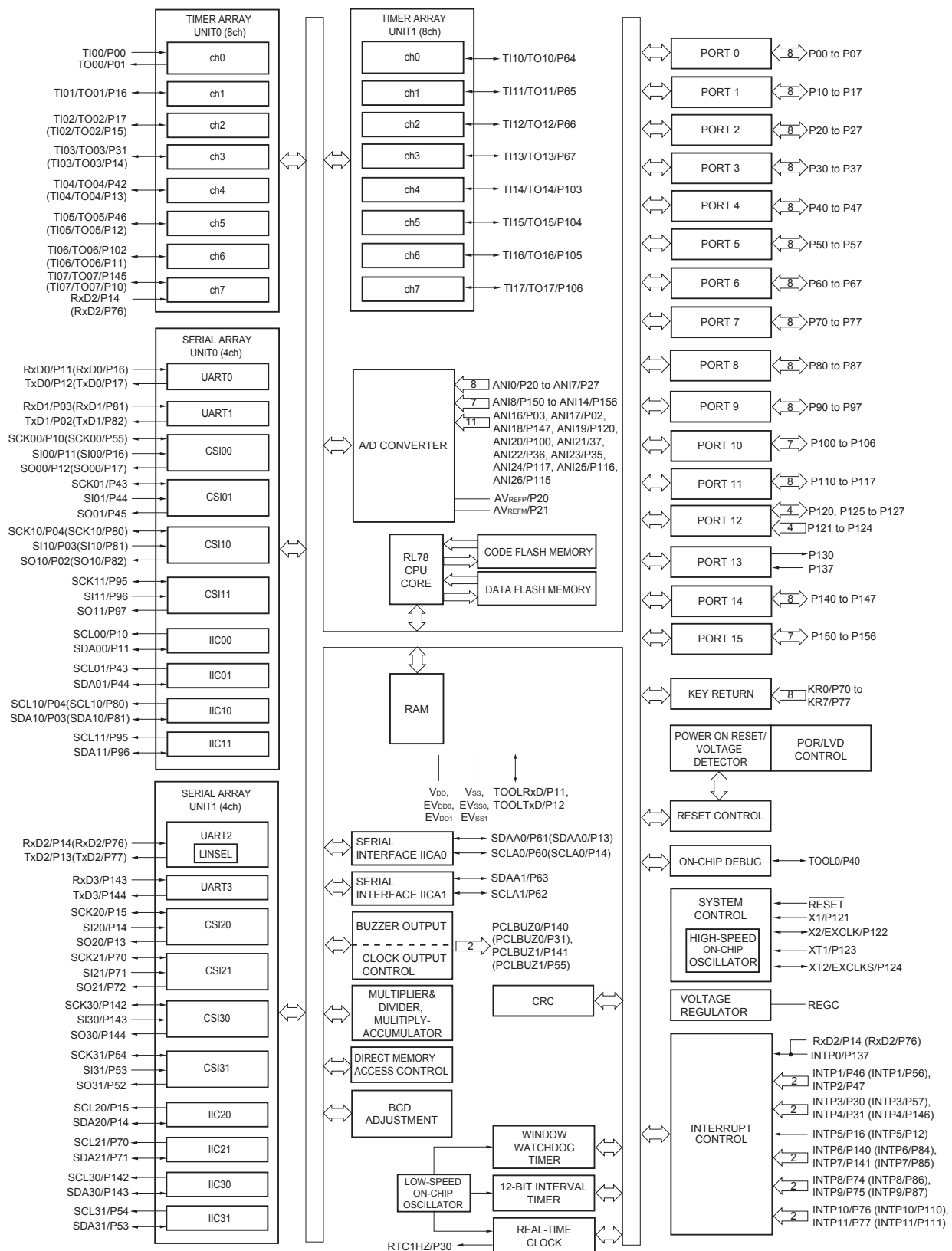
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.
3. It is recommended to connect an exposed die pad to V_{SS}.

1.5.8 44-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, I _{OL} ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			20.0 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		70.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		15.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		9.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		80.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		35.0	mA
			1.8 V ≤ EV _{DD0} < 2.7 V		20.0	mA
			1.6 V ≤ EV _{DD0} < 1.8 V		10.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})			150.0	mA
	I _{OL2}	Per pin for P20 to P27, P150 to P156			0.4 ^{Note 2}	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ V _{DD} ≤ 5.5 V		5.0	mA

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor ≤ 70%.
The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
 - Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V) (4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OH1} = -10.0 mA	E _{VDD0} - 1.5		V
			4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OH1} = -3.0 mA	E _{VDD0} - 0.7		V
			2.7 V ≤ E _{VDD0} ≤ 5.5 V, I _{OH1} = -2.0 mA	E _{VDD0} - 0.6		V
			1.8 V ≤ E _{VDD0} ≤ 5.5 V, I _{OH1} = -1.5 mA	E _{VDD0} - 0.5		V
			1.6 V ≤ E _{VDD0} < 5.5 V, I _{OH1} = -1.0 mA	E _{VDD0} - 0.5		V
	V _{OH2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OH2} = -100 μA	V _{DD} - 0.5		V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL1} = 20 mA		1.3	V
			4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL1} = 8.5 mA		0.7	V
			2.7 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL1} = 3.0 mA		0.6	V
			2.7 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL1} = 1.5 mA		0.4	V
			1.8 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL1} = 0.6 mA		0.4	V
			1.6 V ≤ E _{VDD0} < 5.5 V, I _{OL1} = 0.3 mA		0.4	V
	V _{OL2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OL2} = 400 μA		0.4	V
	V _{OL3}	P60 to P63	4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL3} = 15.0 mA		2.0	V
			4.0 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL3} = 5.0 mA		0.4	V
			2.7 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL3} = 3.0 mA		0.4	V
			1.8 V ≤ E _{VDD0} ≤ 5.5 V, I _{OL3} = 2.0 mA		0.4	V
			1.6 V ≤ E _{VDD0} < 5.5 V, I _{OL3} = 1.0 mA		0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	2.7 V ≤ E _{VDD0} ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ E _{VDD0} ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ E _{VDD0} ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ E _{VDD0} ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ E _{VDD0} ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	t _{KH1} , t _{KL1}	4.0 V ≤ E _{VDD0} ≤ 5.5 V		t _{KCY1} /2 – 12		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.7 V ≤ E _{VDD0} ≤ 5.5 V		t _{KCY1} /2 – 18		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		2.4 V ≤ E _{VDD0} ≤ 5.5 V		t _{KCY1} /2 – 38		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		1.8 V ≤ E _{VDD0} ≤ 5.5 V		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		ns
		1.7 V ≤ E _{VDD0} ≤ 5.5 V		t _{KCY1} /2 – 100		t _{KCY1} /2 – 100		t _{KCY1} /2 – 100		ns
		1.6 V ≤ E _{VDD0} ≤ 5.5 V		—		t _{KCY1} /2 – 100		t _{KCY1} /2 – 100		ns
Slp setup time (to SCKp↑) <small>Note 1</small>	t _{SIK1}	4.0 V ≤ E _{VDD0} ≤ 5.5 V		44		110		110		ns
		2.7 V ≤ E _{VDD0} ≤ 5.5 V		44		110		110		ns
		2.4 V ≤ E _{VDD0} ≤ 5.5 V		75		110		110		ns
		1.8 V ≤ E _{VDD0} ≤ 5.5 V		110		110		110		ns
		1.7 V ≤ E _{VDD0} ≤ 5.5 V		220		220		220		ns
		1.6 V ≤ E _{VDD0} ≤ 5.5 V		—		220		220		ns
Slp hold time (from SCKp↑) <small>Note 2</small>	t _{KSI1}	1.7 V ≤ E _{VDD0} ≤ 5.5 V		19		19		19		ns
		1.6 V ≤ E _{VDD0} ≤ 5.5 V		—		19		19		ns
Delay time from SCKp↓ to SOp output <small>Note 3</small>	t _{KSO1}	1.7 V ≤ E _{VDD0} ≤ 5.5 V C = 30 pF <small>Note 4</small>			25		25		25	ns
		1.6 V ≤ E _{VDD0} ≤ 5.5 V C = 30 pF <small>Note 4</small>			—		25		25	ns

- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		1/f _{MCK} + 190 ^{Note 3}		kHz
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.2. Use it with EV_{DD0} ≥ V_b.3. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

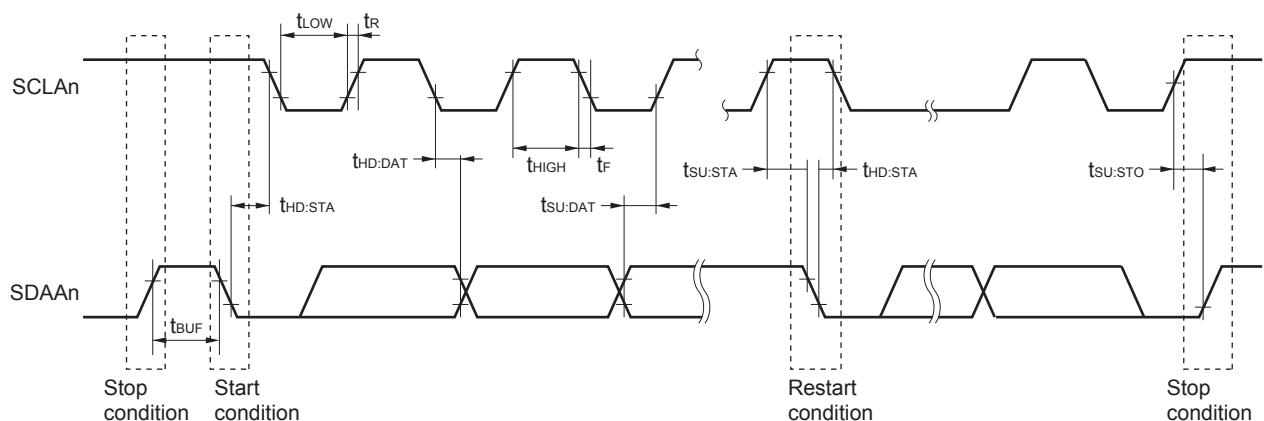
(3) I²C fast mode plus(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f _{SCL}	Fast mode plus: f _{CLK} ≥ 10 MHz	2.7 V ≤ EV _{DD0} ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	t _{SU:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Hold time ^{Note 1}	t _{HD:STA}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		50		—	—	—	—	μs
Data hold time (transmission) ^{Note 2}	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0	0.45	—	—	—	—	μs
Setup time of stop condition	t _{SU:STO}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.26		—	—	—	—	μs
Bus-free time	t _{BUF}	2.7 V ≤ EV _{DD0} ≤ 5.5 V		0.5		—	—	—	—	μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.<R> 2. The maximum value (MAX.) of t_{HD:DAT} is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. At this time, the pin characteristics (I_{OH1}, I_{OL1}, V_{OH1}, V_{OL1}) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ**I²C serial transfer timing****Remark** n = 0, 1

2.6.5 Power supply voltage rising slope characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

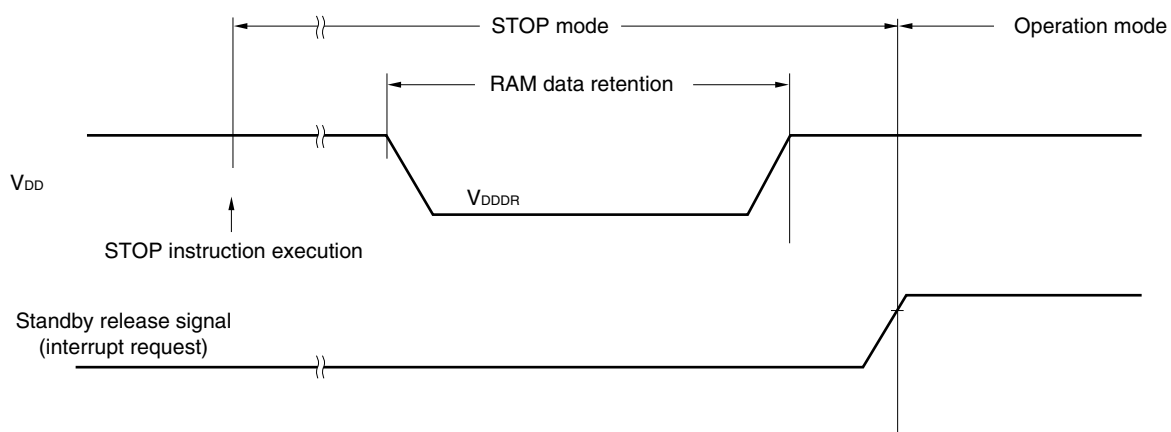
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 ^{Note}		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
		$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		16.0	MHz
XT1 clock oscillation frequency (f_x) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator.

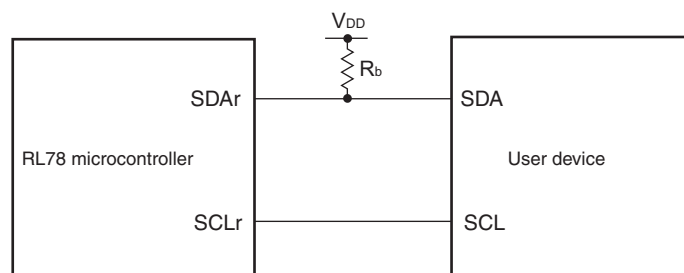
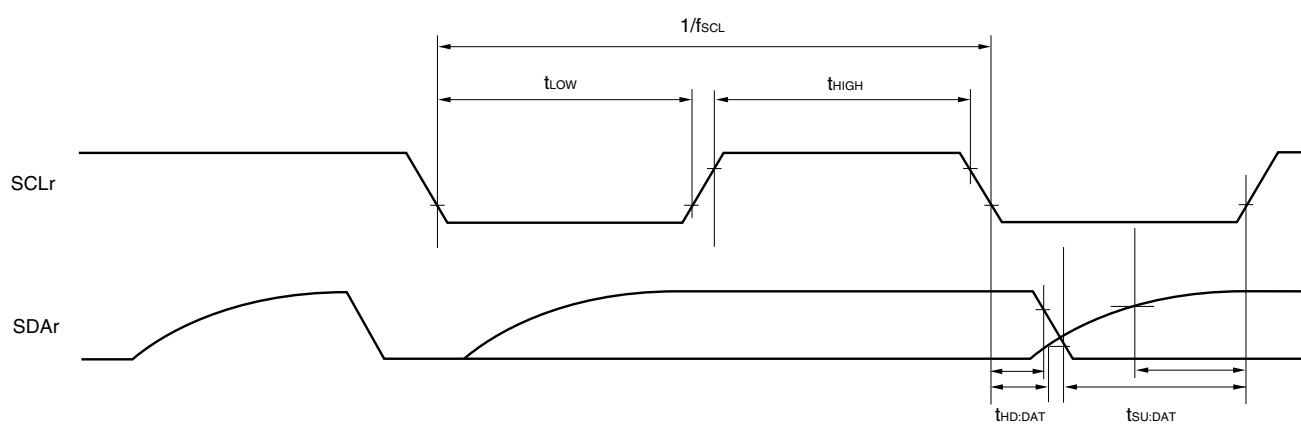
3.2.2 On-chip oscillator characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f_{IH}			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to $+85^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.0		$+1.0$	%
		-40 to -20°C	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-1.5		$+1.5$	%
		$+85$ to $+105^\circ\text{C}$	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	-2.0		$+2.0$	%
Low-speed on-chip oscillator clock frequency	f_{IL}				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		$+15$	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

Simplified I²C mode connection diagram (during communication at same potential)**Simplified I²C mode serial transfer timing (during communication at same potential)**

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	88		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	88		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	220		ns
Slp hold time (from SCKp↓) ^{Note}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	38		ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	38		ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		50	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		50	ns
		$2.4\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (–) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin : ANI16 to ANI26

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (–) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$	1.2	± 5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target pin : ANI16 to ANI26	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125	39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875	39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17	39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 0.35	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 3.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		± 2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI26	0		AV_{REFP} and EV_{DD0}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

3.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f _{CLK}	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		32	MHz
Number of code flash rewrites <small>Notes 1,2,3</small>	C _{enwr}	Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	1,000			Times
Number of data flash rewrites <small>Notes 1,2,3</small>		Retained for 1 years $T_A = 25^\circ\text{C}$		1,000,000		
		Retained for 5 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	100,000			
		Retained for 20 years $T_A = 85^\circ\text{C}$ <small>Note 4</small>	10,000			

- Notes**
- 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
 2. When using flash memory programmer and Renesas Electronics self programming library.
 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
 4. This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

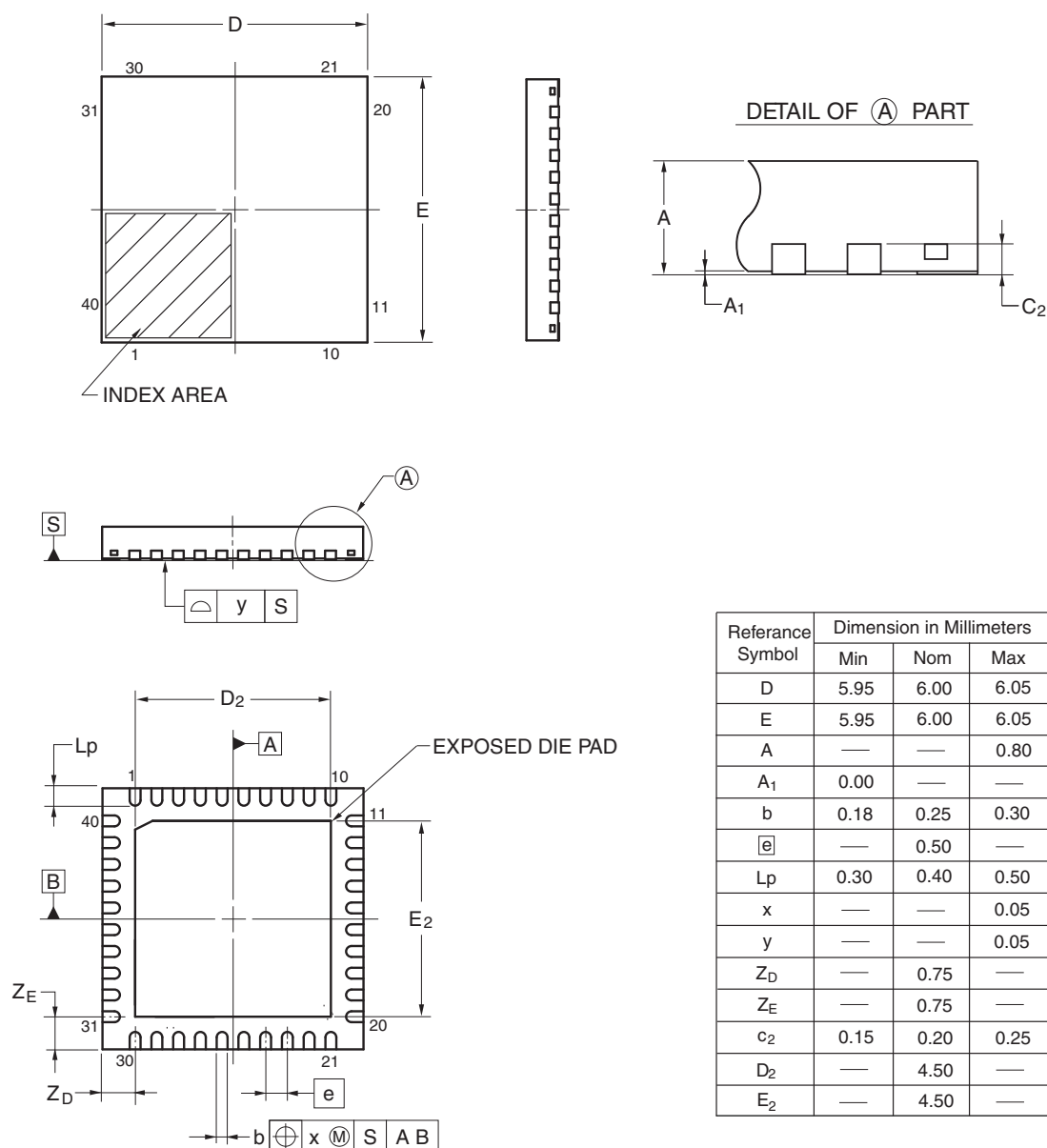
($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD0} = V_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = V_{SS0} = V_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.7 40-pin Products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA,
 R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA,
 R5F101EHDNA
 R5F100EAGNA, R5F100ECGNA, R5F100EDGNA, R5F100EEGNA, R5F100EFGNA, R5F100EGGNA,
 R5F100EHGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-5	0.09

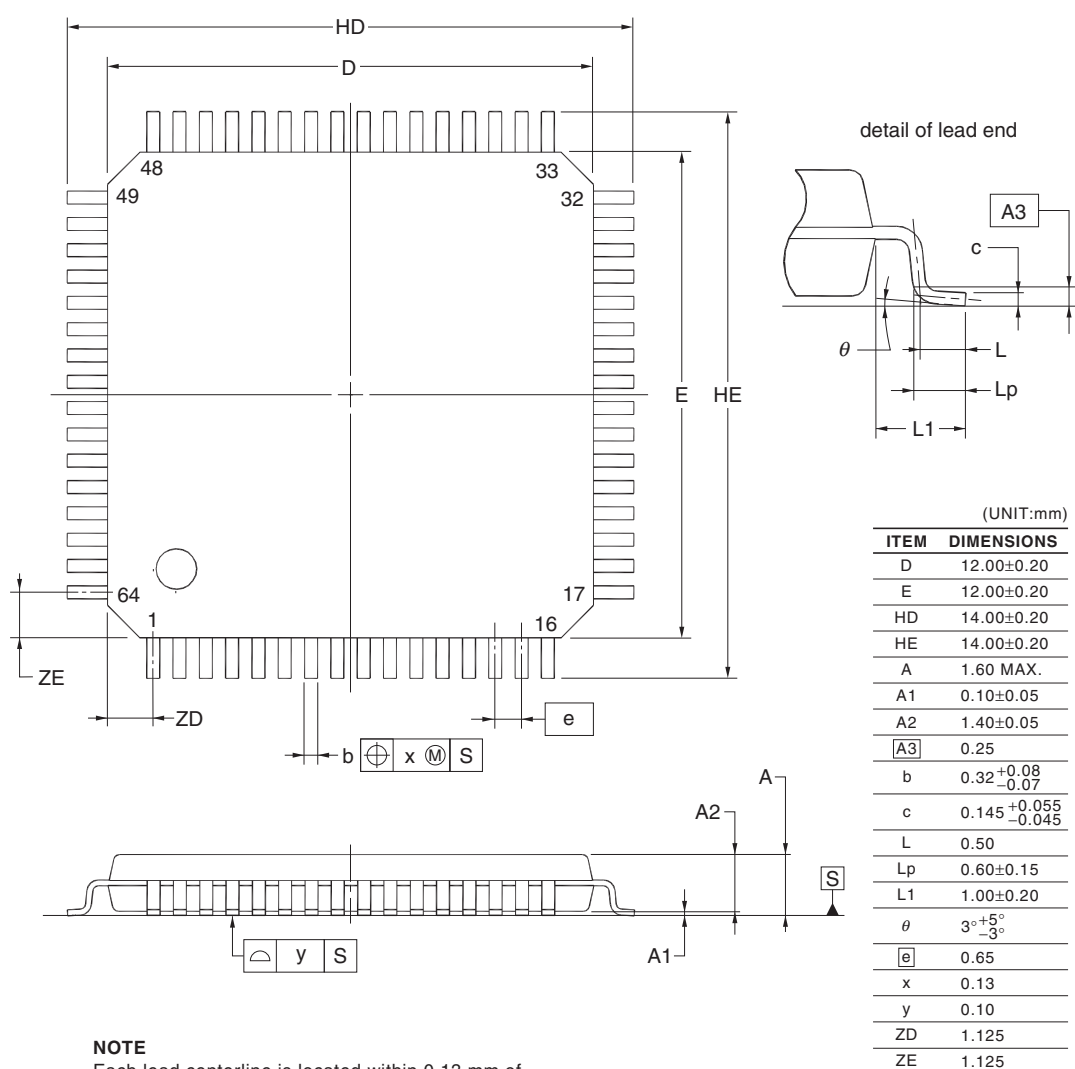


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4.11 64-pin Products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJAF, A,
R5F100LKAFA, R5F100LLAFA
R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJAF, A,
R5F101LKAFA, R5F101LLAFA
R5F100LCDFA, R5F100LDDFA, R5F100LEDFA, R5F100LFDFA, R5F100LG DFA, R5F100LH DFA, R5F100LJ DFA,
R5F100LK DFA, R5F100LL DFA
R5F101LCDFA, R5F101LDDFA, R5F101LEDFA, R5F101LFDFA, R5F101LG DFA, R5F101LH DFA, R5F101LJ DFA,
R5F101LK DFA, R5F101LL DFA
R5F100LCGFA, R5F100LDGFA, R5F100LEGFA, R5F100LFGFA, R5F100LGGFA, R5F100LHGFA,
R5F100LJGFA

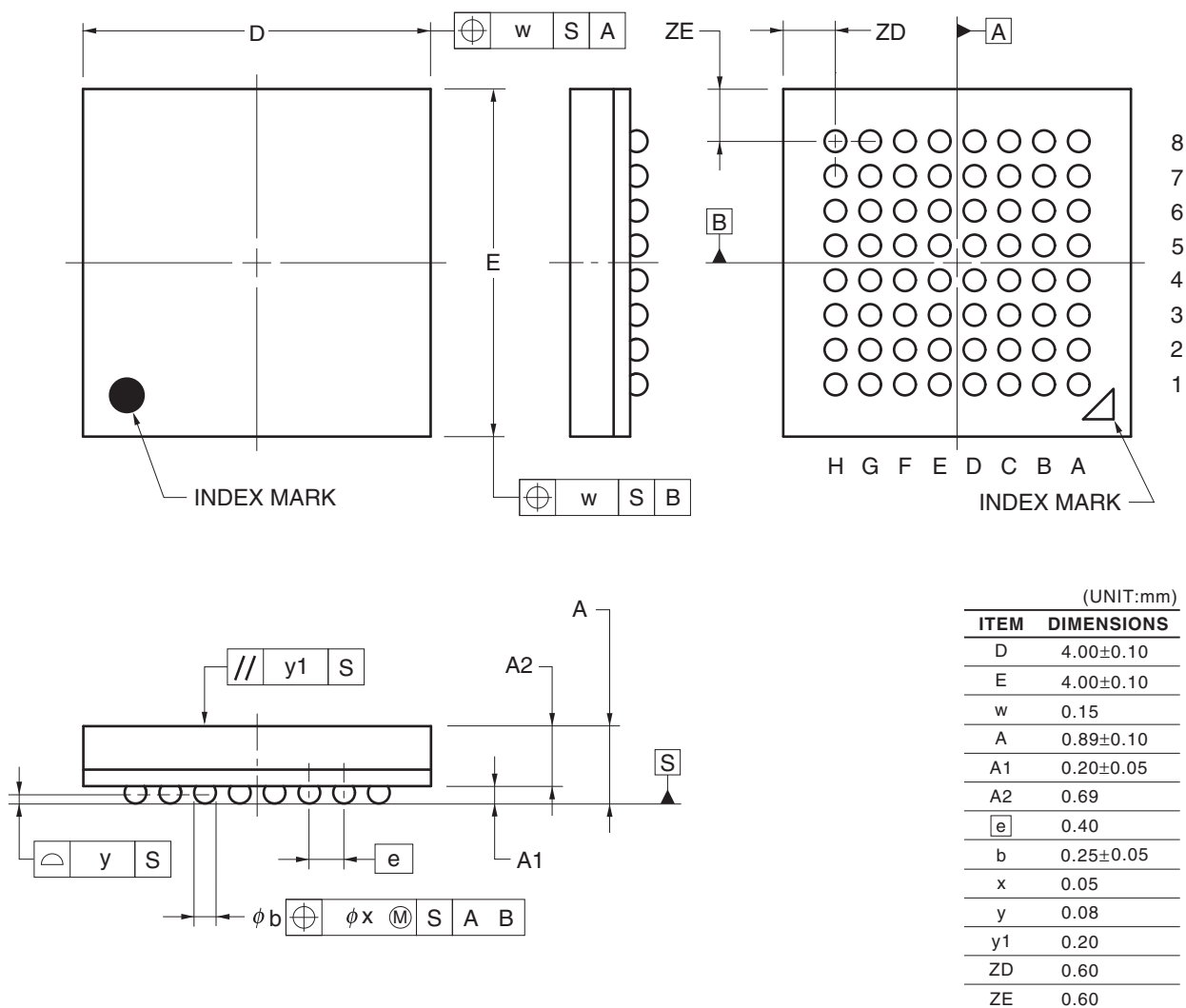
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

**NOTE**

Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,
 R5F100LJABG
 R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,
 R5F101LJABG
 R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,
 R5F100LJGBG

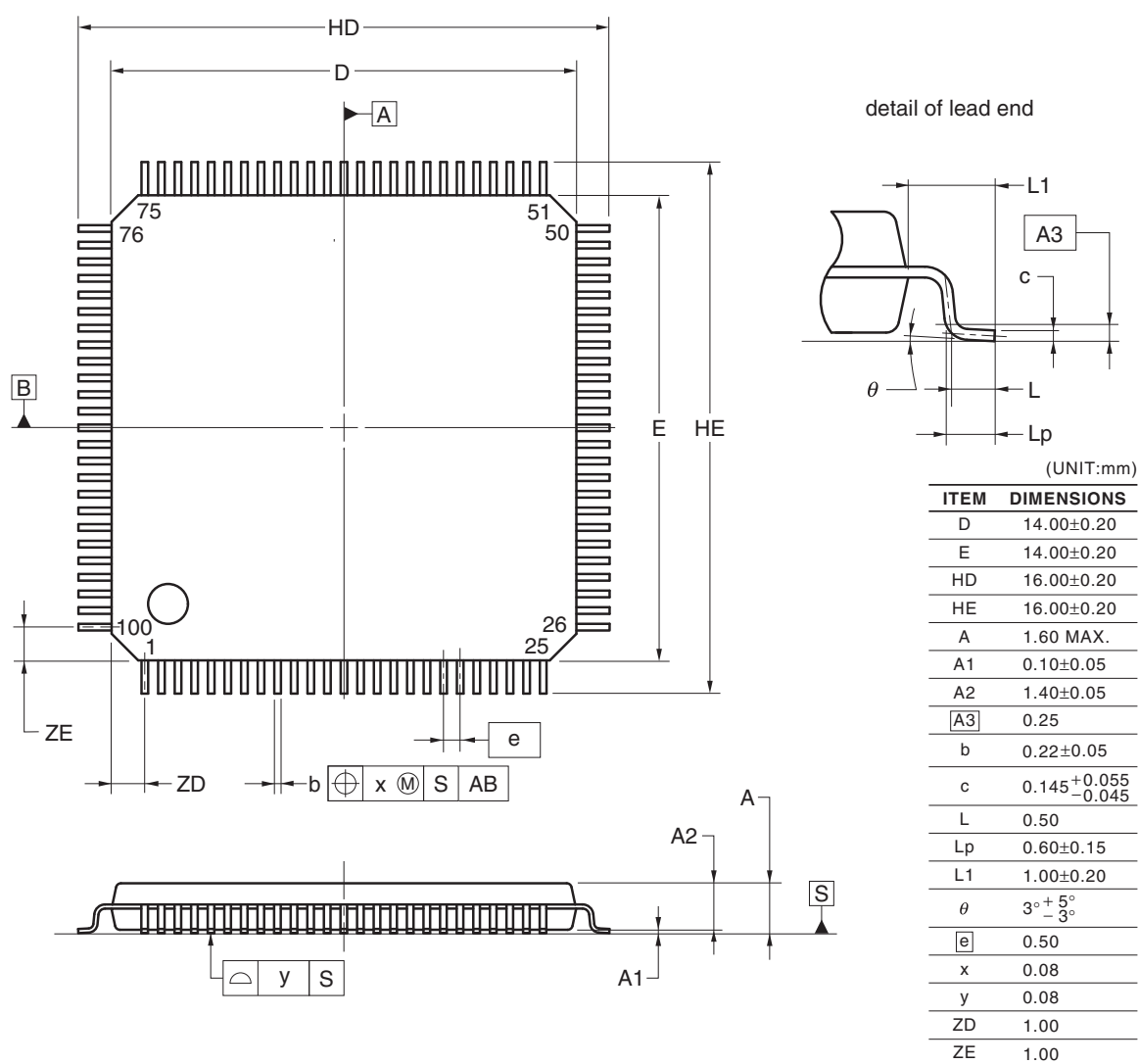
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03



4.13 100-pin Products

R5F100PFAFB, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	81	Modification of figure of AC Timing Test Points
		81	Modification of description and note 3 in (1) During communication at same potential (UART mode)
		83	Modification of description in (2) During communication at same potential (CSI mode)
		84	Modification of description in (3) During communication at same potential (CSI mode)
		85	Modification of description in (4) During communication at same potential (CSI mode) (1/2)
		86	Modification of description in (4) During communication at same potential (CSI mode) (2/2)
		88	Modification of table in (5) During communication at same potential (simplified I ² C mode) (1/2)
		89	Modification of table and caution in (5) During communication at same potential (simplified I ² C mode) (2/2)
		91	Modification of table and notes 1 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		92, 93	Modification of table and notes 2 to 7 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		94	Modification of remarks 1 to 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		95	Modification of table in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (1/2)
		96	Modification of table and caution in (7) Communication at different potential (2.5 V, 3 V) (CSI mode) (2/2)
		97	Modification of table in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		98	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		99	Modification of table, note 1, and caution in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		100	Modification of remarks 3 and 4 in (8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		102	Modification of table in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/2)
		103	Modification of table and caution in (9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/2)
		106	Modification of table in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (1/2)
		107	Modification of table, note 1, and caution in (10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I ² C mode) (2/2)
		109	Addition of (1) I ² C standard mode
		111	Addition of (2) I ² C fast mode
		112	Addition of (3) I ² C fast mode plus
		112	Modification of IICA serial transfer timing
		113	Addition of table in 2.6.1 A/D converter characteristics
		113	Modification of description in 2.6.1 (1)
		114	Modification of notes 3 to 5 in 2.6.1 (1)
		115	Modification of description and notes 2, 4, and 5 in 2.6.1 (2)
		116	Modification of description and notes 3 and 4 in 2.6.1 (3)
		117	Modification of description and notes 3 and 4 in 2.6.1 (4)

Rev.	Date	Description	
		Page	Summary
3.00	Aug 02, 2013	118	Modification of table in 2.6.2 Temperature sensor/internal reference voltage characteristics
		118	Modification of table and note in 2.6.3 POR circuit characteristics
		119	Modification of table in 2.6.4 LVD circuit characteristics
		120	Modification of table of LVD Detection Voltage of Interrupt & Reset Mode
		120	Renamed to 2.6.5 Power supply voltage rising slope characteristics
		122	Modification of table, figure, and remark in 2.10 Timing Specs for Switching Flash Memory Programming Modes
		123	Modification of caution 1 and description
		124	Modification of table and remark 3 in Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)
		126	Modification of table, note, caution, and remark in 3.2.1 X1, XT1 oscillator characteristics
		126	Modification of table in 3.2.2 On-chip oscillator characteristics
		127	Modification of note 3 in 3.3.1 Pin characteristics (1/5)
		128	Modification of note 3 in 3.3.1 Pin characteristics (2/5)
		133	Modification of notes 1 and 4 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (1/2)
		135	Modification of notes 1, 5, and 6 in (1) Flash ROM: 16 to 64 KB of 20- to 64-pin products (2/2)
		137	Modification of notes 1 and 4 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (1/2)
		139	Modification of notes 1, 5, and 6 in (2) Flash ROM: 96 to 256 KB of 30- to 100-pin products (2/2)
		140	Modification of (3) Peripheral Functions (Common to all products)
		142	Modification of table in 3.4 AC Characteristics
		143	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		143	Modification of figure of AC Timing Test Points
		143	Modification of figure of External System Clock Timing
		145	Modification of figure of AC Timing Test Points
		145	Modification of description, note 1, and caution in (1) During communication at same potential (UART mode)
		146	Modification of description in (2) During communication at same potential (CSI mode)
		147	Modification of description in (3) During communication at same potential (CSI mode)
		149	Modification of table, note 1, and caution in (4) During communication at same potential (simplified I ² C mode)
		151	Modification of table, note 1, and caution in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)
		152 to 154	Modification of table, notes 2 to 6, caution, and remarks 1 to 4 in (5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)
		155	Modification of table in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (1/3)
		156	Modification of table and caution in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (2/3)
		157, 158	Modification of table, caution, and remarks 3 and 4 in (6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (3/3)
		160, 161	Modification of table and caution in (7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode)