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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

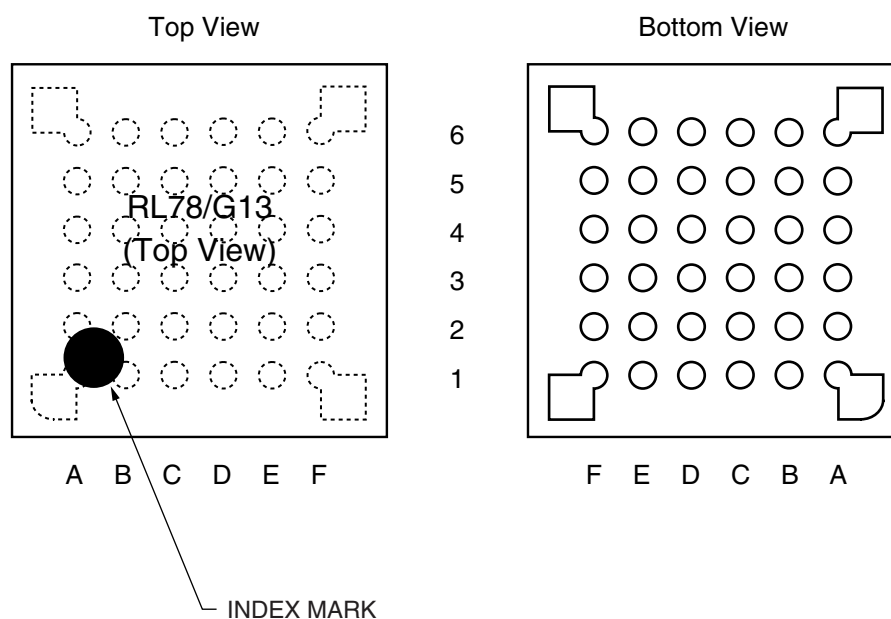| Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gedfb-50

Table 1-1. List of Ordering Part Numbers

(6/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
48 pins	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	Mounted	A	R5F100GAANA#U0, R5F100GCANA#U0, R5F100GDANA#U0, R5F100GEANA#U0, R5F100GFANA#U0, R5F100GGANA#U0, R5F100GHANA#U0, R5F100GJANA#U0, R5F100GKANA#U0, R5F100GLANA#U0 R5F100GAANA#W0, R5F100GCANA#W0, R5F100GDANA#W0, R5F100GEANA#W0, R5F100GFANA#W0, R5F100GGANA#W0, R5F100GHANA#W0, R5F100GJANA#W0, R5F100GKANA#W0, R5F100GLANA#W0
			D	R5F100GADNA#U0, R5F100GCDNA#U0, R5F100GDDNA#U0, R5F100GEDNA#U0, R5F100GFDNA#U0, R5F100GGDNA#U0, R5F100GHDNA#U0, R5F100GJDNA#U0, R5F100GKDNA#U0, R5F100GLDNA#U0 R5F100GADNA#W0, R5F100GCDNA#W0, R5F100GDDNA#W0, R5F100GEDNA#W0, R5F100GFDNA#W0, R5F100GGDNA#W0, R5F100GHDNA#W0, R5F100GJDNA#W0, R5F100GKDNA#W0, R5F100GLDNA#W0
			G	R5F100GAGNA#U0, R5F100GCGNA#U0, R5F100GDGNA#U0, R5F100GEGNA#U0, R5F100GFGNA#U0, R5F100GGGNA#U0, R5F100GHGNA#U0, R5F100GJGNA#U0 R5F100GAGNA#W0, R5F100GCGNA#W0, R5F100GDGNA#W0, R5F100GEGNA#W0, R5F100GFGNA#W0, R5F100GGGNA#W0, R5F100GHGNA#W0, R5F100GJGNA#W0
		Not mounted	A	R5F101GAANA#U0, R5F101GCANA#U0, R5F101GDANA#U0, R5F101GEANA#U0, R5F101GFANA#U0, R5F101GGANA#U0, R5F101GHANA#U0, R5F101GJANA#U0, R5F101GKANA#U0, R5F101GLANA#U0 R5F101GAANA#W0, R5F101GCANA#W0, R5F101GDANA#W0, R5F101GEANA#W0, R5F101GFANA#W0, R5F101GGANA#W0, R5F101GHANA#W0, R5F101GJANA#W0, R5F101GKANA#W0, R5F101GLANA#W0
			D	R5F101GADNA#U0, R5F101GCDNA#U0, R5F101GDDNA#U0, R5F101GEDNA#U0, R5F101GFDNA#U0, R5F101GGDNA#U0, R5F101GHDNA#U0, R5F101GJDNA#U0, R5F101GKDNA#U0, R5F101GLDNA#U0 R5F101GADNA#W0, R5F101GCDNA#W0, R5F101GDDNA#W0, R5F101GEDNA#W0, R5F101GFDNA#W0, R5F101GGDNA#W0, R5F101GHDNA#W0, R5F101GJDNA#W0, R5F101GKDNA#W0, R5F101GLDNA#W0

Note　For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution　The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.6 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)

Top View   Bottom View

INDEX MARK

	A	B	C	D	E	F	
6	P60/SCLA0	V_{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V_{SS}	REGC	$\overline{RESET}$	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV_{REFP}	P21/ANI1/ AV_{REFM}	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
　　　　　2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

3. When setting to PIOR = 1

(2/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin	
		R5F100Ex	R5F101Ex	R5F100Fx	R5F101Fx	R5F100Gx	R5F101Gx	R5F100Jx	R5F101Jx	R5F100Lx	R5F101Lx
Clock output/buzzer output		2		2		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)									
8/10-bit resolution A/D converter		9 channels		10 channels		10 channels		12 channels		12 channels	
Serial interface		[40-pin, 44-pin products] • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I^2C: 2 channels/UART (UART supporting LIN-bus): 1 channel									
	I^2C bus	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)									
DMA controller		2 channels									
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt		4		4		6		8		8	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access									
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)									
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)									
On-chip debug function		Provided									
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)									
<R> Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)									

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I$_{OH1}$	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			−10.0 [Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			−55.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			−10.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			−5.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			−2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70%[Note 3])	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			−80.0	mA
			2.7 V ≤ EV$_{DD0}$ < 4.0 V			−19.0	mA
			1.8 V ≤ EV$_{DD0}$ < 2.7 V			−10.0	mA
			1.6 V ≤ EV$_{DD0}$ < 1.8 V			−5.0	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			−135.0 [Note 4]	mA
	I$_{OH2}$	Per pin for P20 to P27, P150 to P156	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−0.1 [Note 2]	mA
		Total of all pins (When duty ≤ 70%[Note 3])	1.6 V ≤ V$_{DD}$ ≤ 5.5 V			−1.5	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV$_{DD0}$, EV$_{DD1}$, V$_{DD}$ pins to an output pin.

    2. However, do not exceed the total current value.

    3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I$_{OH}$ × 0.7)/(n × 0.01)

<Example> Where n = 80% and I$_{OH}$ = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(80 × 0.01) ≅ −8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

    4. The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx, R5F100xxGxx) is −100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

   2. During HALT instruction execution by flash memory.

   3. When high-speed on-chip oscillator and subsystem clock are stopped.

   4. When high-speed system clock and subsystem clock are stopped.

   5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

   6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

   7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 32 MHz

   2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 16 MHz

   LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 8 MHz

   LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 4 MHz

   8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

   2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

   3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

   4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

**(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	1.86	mA
					V$_{DD}$ = 3.0 V		0.62	1.86	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	1.45	mA
					V$_{DD}$ = 3.0 V		0.50	1.45	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.11	mA
					V$_{DD}$ = 3.0 V		0.44	1.11	mA
			LS (low-speed main) mode [Note 7]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		290	620	μA
					V$_{DD}$ = 2.0 V		290	620	μA
			LV (low-voltage main) mode [Note 7]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		440	680	μA
					V$_{DD}$ = 2.0 V		440	680	μA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
			LS (low-speed main) mode [Note 7]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.19	0.52	μA
			T$_A$ = +25°C				0.25	0.52	μA
			T$_A$ = +50°C				0.32	2.21	μA
			T$_A$ = +70°C				0.55	3.94	μA
			T$_A$ = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

    2. During HALT instruction execution by flash memory.

    3. When high-speed on-chip oscillator and subsystem clock are stopped.

    4. When high-speed system clock and subsystem clock are stopped.

    5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

    6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

    7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

        HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

                                     2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

        LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

        LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

    8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

    2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

    3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

    4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

UART mode connection diagram (during communication at same potential)
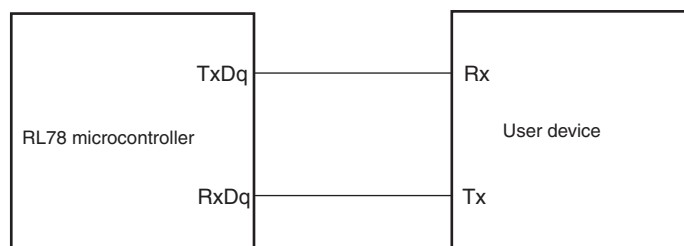
UART mode bit width (during communication at same potential) (reference)
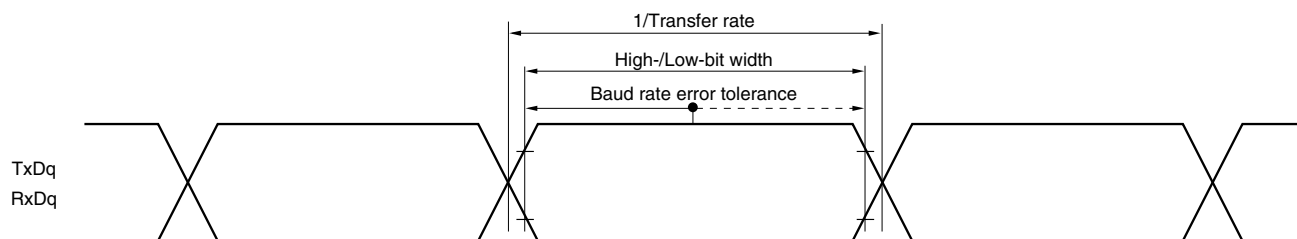
Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

   2. f$_{MCK}$: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

    n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (2/2)

$(T_A = -40$ to $+85°C$, 1.6 V $\le EV_{DD0} = EV_{DD1} \le V_{DD} \le 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V$)$

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↑) [Note 1]	t_{SIK2}	2.7 V $\le EV_{DD0} \le$ 5.5 V		$1/f_{MCK}+20$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		1.8 V $\le EV_{DD0} \le$ 5.5 V		$1/f_{MCK}+30$		$1/f_{MCK}+30$		$1/f_{MCK}+30$		ns
		1.7 V $\le EV_{DD0} \le$ 5.5 V		$1/f_{MCK}+40$		$1/f_{MCK}+40$		$1/f_{MCK}+40$		ns
		1.6 V $\le EV_{DD0} \le$ 5.5 V		—		$1/f_{MCK}+40$		$1/f_{MCK}+40$		ns
SIp hold time (from SCKp↑) [Note 2]	t_{KSI2}	1.8 V $\le EV_{DD0} \le$ 5.5 V		$1/f_{MCK}+31$		$1/f_{MCK}+31$		$1/f_{MCK}+31$		ns
		1.7 V $\le EV_{DD0} \le$ 5.5 V		$1/f_{MCK}+250$		$1/f_{MCK}+250$		$1/f_{MCK}+250$		ns
		1.6 V $\le EV_{DD0} \le$ 5.5 V		—		$1/f_{MCK}+250$		$1/f_{MCK}+250$		ns
Delay time from SCKp↓ to SOp output [Note 3]	t_{KSO2}	C = 30 pF [Note 4]	2.7 V $\le EV_{DD0} \le$ 5.5 V		$2/f_{MCK}+44$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			2.4 V $\le EV_{DD0} \le$ 5.5 V		$2/f_{MCK}+75$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			1.8 V $\le EV_{DD0} \le$ 5.5 V		$2/f_{MCK}+110$		$2/f_{MCK}+110$		$2/f_{MCK}+110$	ns
			1.7 V $\le EV_{DD0} \le$ 5.5 V		$2/f_{MCK}+220$		$2/f_{MCK}+220$		$2/f_{MCK}+220$	ns
			1.6 V $\le EV_{DD0} \le$ 5.5 V		—		$2/f_{MCK}+220$		$2/f_{MCK}+220$	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. C is the load capacitance of the SOp output lines.

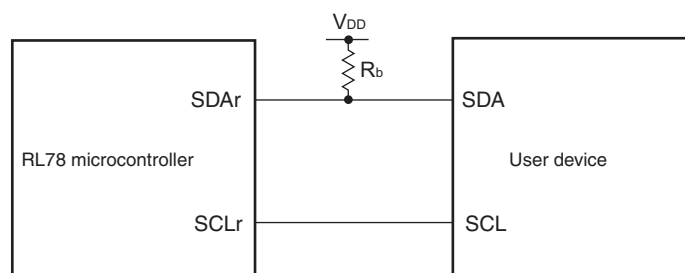   **5.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Caution   **Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),

    n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

    2. f_{MCK}: Serial array unit operation clock frequency

    (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

    n: Channel number (mn = 00 to 03, 10 to 13))

(5) During communication at same potential (simplified I²C mode) (1/2)

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1850		1850		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

Simplified I²C mode mode connection diagram (during communication at same potential)

V_{DD}

R_b

RL78 microcontroller

SDAr — SDA

SCLr — SCL

User device

Simplified I²C mode serial transfer timing (during communication at same potential)

$1/f_{SCL}$

t_{LOW} t_{HIGH}

SCLr

SDAr

$t_{HD:DAT}$ $t_{SU:DAT}$
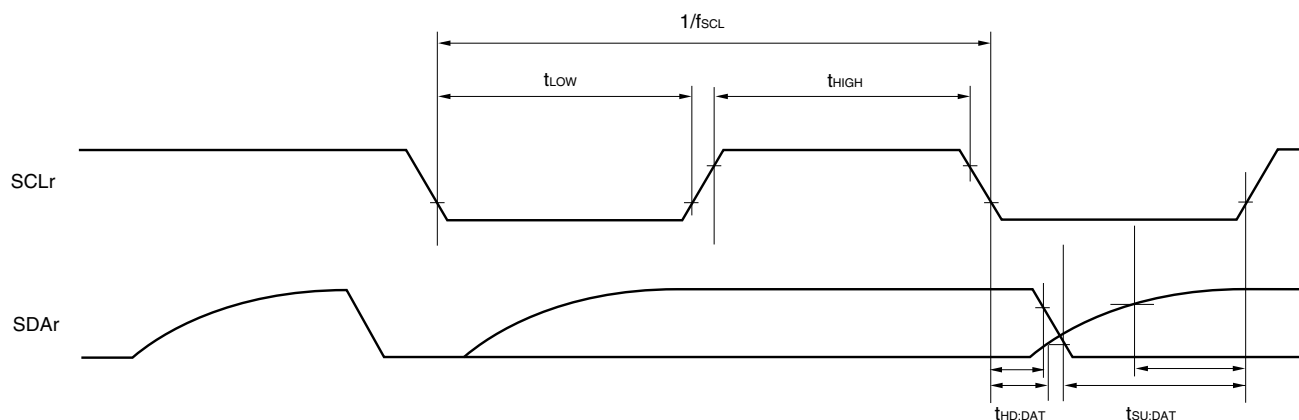
Remarks 1. $R_b[\Omega]$:Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance

    2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

    3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),

n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]		1.2	±10.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±6.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI14		0		V$_{DD}$	V
		ANI16 to ANI26		0		EV$_{DD0}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{TMPS25}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

　2. This value is indicated as a ratio (%FSR) to the full-scale value.

　3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

　4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V$_{LVD0}$	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V$_{LVD1}$	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V$_{LVD2}$	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V$_{LVD3}$	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V$_{LVD4}$	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V$_{LVD5}$	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V$_{LVD6}$	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V$_{LVD7}$	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V$_{LVD8}$	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V$_{LVD9}$	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V$_{LVD10}$	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V$_{LVD11}$	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V$_{LVD12}$	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V$_{LVD13}$	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t$_{LW}$		300			μs
Detection delay time						300	μs

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (5/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I$_{LIH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{DD0}$			1	μA
	I$_{LIH2}$	P20 to P27, P137, P150 to P156, $\overline{RESET}$	V$_I$ = V$_{DD}$			1	μA
	I$_{LIH3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{DD}$	In input port or external clock input			1	μA
				In resonator connection			10	μA
Input leakage current, low	I$_{LIL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$				−1	μA
	I$_{LIL2}$	P20 to P27, P137, P150 to P156, $\overline{RESET}$	V$_I$ = V$_{SS}$				−1	μA
	I$_{LIL3}$	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V$_I$ = V$_{SS}$	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
On-chip pll-up resistance	R$_U$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V$_I$ = EV$_{SS0}$, In input port	10	20	100	kΩ

Remark   Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(4) During communication at same potential (simplified I²C mode)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode MIN.	HS (high-speed main) Mode MAX.	Unit
SCLr clock frequency	f$_{SCL}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400[Note1]	kHz
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ		100[Note1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t$_{HIGH}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	4600		ns
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 220[Note2]		ns
		2.4 V ≤ EV$_{DD}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 580[Note2]		ns
Data hold time (transmission)	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	770	ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	1420	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

       2. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   **Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).**

(**Remarks** are listed on the next page.)

Simplified I^{2}C mode mode connection diagram (during communication at same potential)
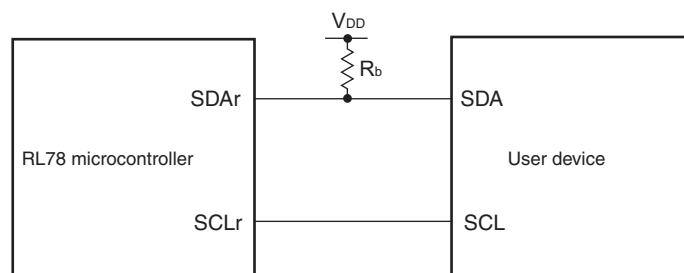
Simplified I^{2}C mode serial transfer timing (during communication at same potential)

Remarks 1. R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

   2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
   h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

   3. f$_{MCK}$: Serial array unit operation clock frequency

   (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m
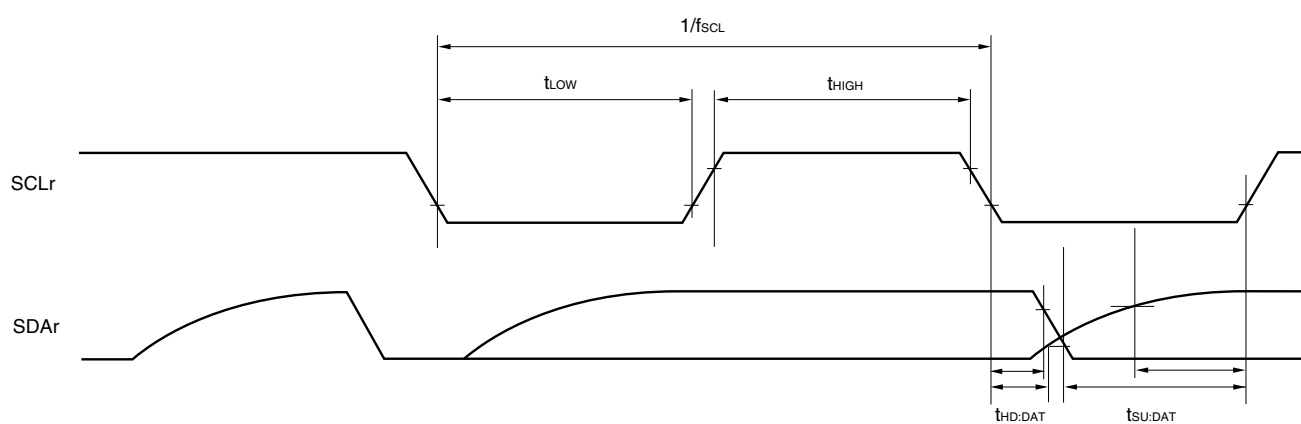
   = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) [Note]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	162		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	354		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) [Note]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	38		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	38		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	38		ns
Delay time from SCKp↓ to SOp output [Note]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		200	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		390	ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		966	ns

Note   When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

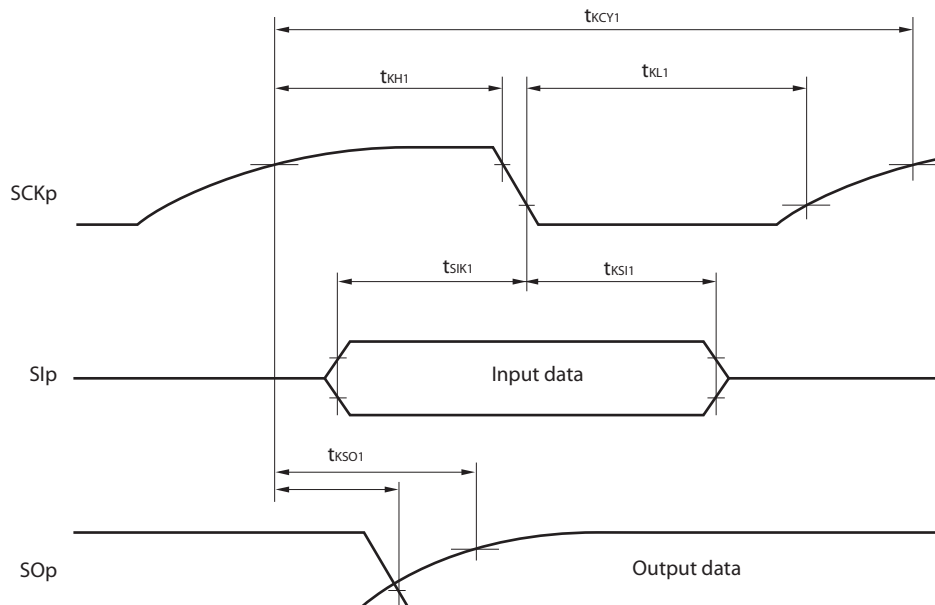**Caution**   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the page after the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
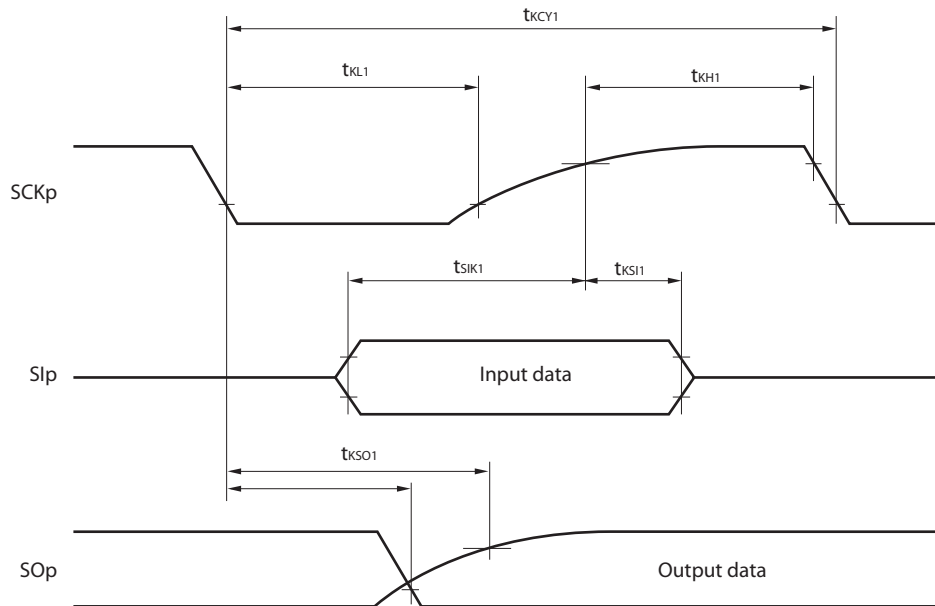
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
     2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Simplified I²C mode connection diagram (during communication at different potential)
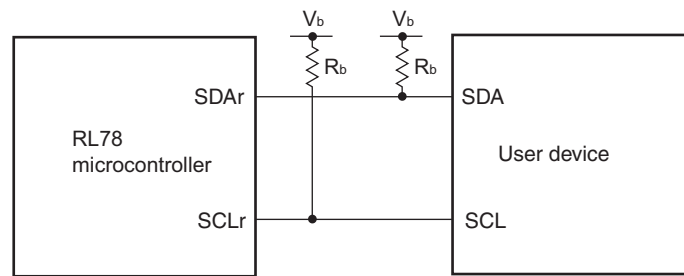
**Simplified I²C mode serial transfer timing (during communication at different potential)**
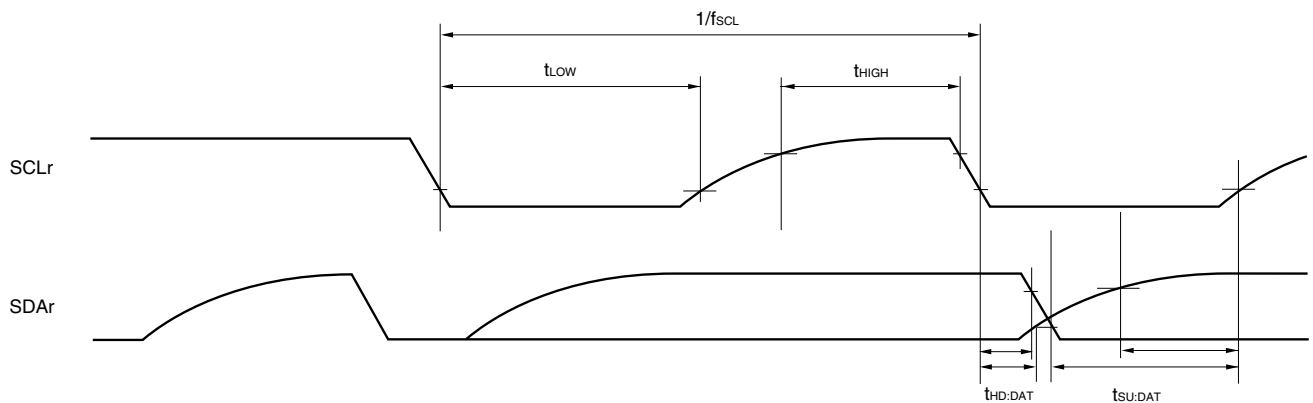
Caution Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1. R$_b$[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance, V$_b$[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00, 01, 02, 10, 12, 13)

4.14 128-pin Products

R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB
R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB
R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92
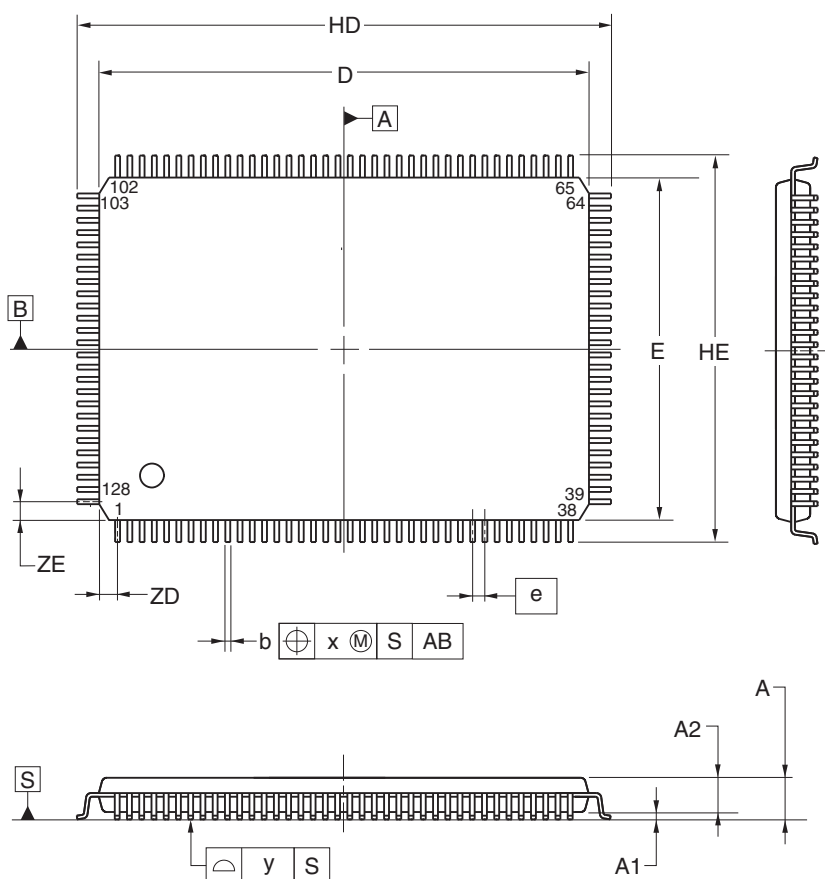
detail of lead end
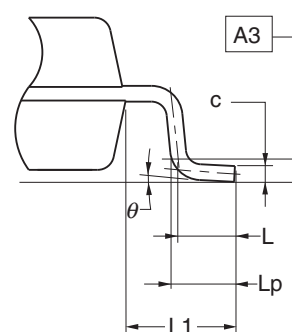
(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75