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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gfana-u0

Table 1-1. List of Ordering Part Numbers

(1/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
20 pins	20-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	Mounted	A	R5F1006AASP#V0, R5F1006CASP#V0, R5F1006DASP#V0, R5F1006EASP#V0
				R5F1006AASP#X0, R5F1006CASP#X0, R5F1006DASP#X0, R5F1006EASP#X0
			D	R5F1006ADSP#V0, R5F1006CDSP#V0, R5F1006DDSP#V0, R5F1006EDSP#V0
				R5F1006ADSP#X0, R5F1006CDSP#X0, R5F1006DDSP#X0, R5F1006EDSP#X0
			G	R5F1006AGSP#V0, R5F1006CGSP#V0, R5F1006DGSP#V0, R5F1006EGSP#V0
				R5F1006AGSP#X0, R5F1006CGSP#X0, R5F1006DGSP#X0, R5F1006EGSP#X0
		Not mounted	A	R5F1016AASP#V0, R5F1016CASP#V0, R5F1016DASP#V0, R5F1016EASP#V0
				R5F1016AASP#X0, R5F1016CASP#X0, R5F1016DASP#X0, R5F1016EASP#X0
			D	R5F1016ADSP#V0, R5F1016CDSP#V0, R5F1016DDSP#V0, R5F1016EDSP#V0
				R5F1016ADSP#X0, R5F1016CDSP#X0, R5F1016DDSP#X0, R5F1016EDSP#X0
24 pins	24-pin plastic HWQFN (4 × 4mm, 0.5 mm pitch)	Mounted	A	R5F1007AANA#U0, R5F1007CANA#U0, R5F1007DANA#U0, R5F1007EANA#U0
				R5F1007AANA#W0, R5F1007CANA#W0, R5F1007DANA#W0, R5F1007EANA#W0
			D	R5F1007ADNA#U0, R5F1007CDNA#U0, R5F1007DDNA#U0, R5F1007EDNA#U0
				R5F1007ADNA#W0, R5F1007CDNA#W0, R5F1007DDNA#W0, R5F1007EDNA#W0
			G	R5F1007AGNA#U0, R5F1007CGNA#U0, R5F1007DGNA#U0, R5F1007EGNA#U0
				R5F1007AGNA#W0, R5F1007CGNA#W0, R5F1007DGNA#W0, R5F1007EGNA#W0
		Not mounted	A	R5F1017AANA#U0, R5F1017CANA#U0, R5F1017DANA#U0, R5F1017EANA#U0
				R5F1017AANA#W0, R5F1017CANA#W0, R5F1017DANA#W0, R5F1017EANA#W0
			D	R5F1017ADNA#U0, R5F1017CDNA#U0, R5F1017DDNA#U0, R5F1017EDNA#U0
				R5F1017ADNA#W0, R5F1017CDNA#W0, R5F1017DDNA#W0, R5F1017EDNA#W0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(12/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
128 pins	128-pin plastic LFQFP (14 × 20 mm, 0.5 mm pitch)	Mounted	A	R5F100SHAFB#V0, R5F100SJAFB#V0, R5F100SKAFB#V0, R5F100SLAFB#V0 R5F100SHAFB#X0, R5F100SJAFB#X0, R5F100SKAFB#X0, R5F100SLAFB#X0
			D	R5F100SHDFB#V0, R5F100SJDFB#V0, R5F100SKDFB#V0, R5F100SLDFB#V0 R5F100SHDFB#X0, R5F100SJDFB#X0, R5F100SKDFB#X0, R5F100SLDFB#X0
		Not mounted	A	R5F101SHAFB#V0, R5F101SJAFB#V0, R5F101SKAFB#V0, R5F101SLAFB#V0 R5F101SHAFB#X0, R5F101SJAFB#X0, R5F101SKAFB#X0, R5F101SLAFB#X0
			D	R5F101SHDFB#V0, R5F101SJDFB#V0, R5F101SKDFB#V0, R5F101SLDFB#V0 R5F101SHDFB#X0, R5F101SJDFB#X0, R5F101SKDFB#X0, R5F101SLDFB#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.13 100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)
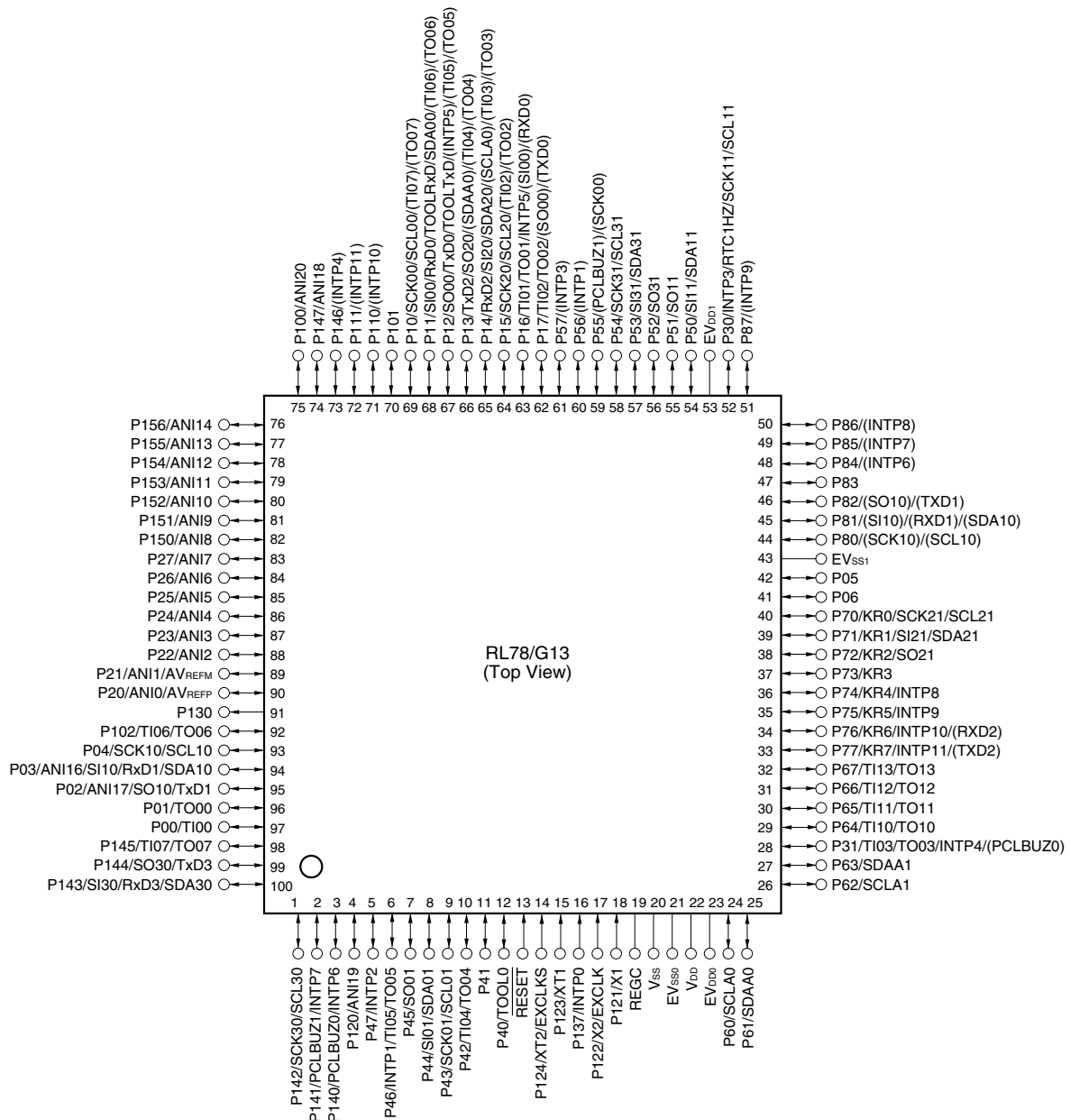
Cautions 1. Make EVss0, EVss1 pins the same potential as Vss pin.

2. Make Vdd pin the potential that is higher than EVdd0, EVdd1 pins (EVdd0 = EVdd1).

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the Vdd, EVdd0 and EVdd1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

2. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves) (see **6.9.3 Operation as multiple PWM output function** in the RL78/G13 User's Manual).

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Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output		2		2		2	
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)					
8/10-bit resolution A/D converter		17 channels		20 channels		26 channels	
Serial interface		[80-pin, 100-pin, 128-pin products] • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel					
	I²C bus	2 channels		2 channels		2 channels	
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)					
DMA controller		4 channels					
Vectored interrupt sources	Internal	37		37		41	
	External	13		13		13	
Key interrupt		8		8		8	
Reset		• Reset by $\overline{RESET}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access					
Power-on-reset circuit		• Power-on-reset: 1.51 V (TYP.) • Power-down-reset: 1.50 V (TYP.)					
Voltage detector		• Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages)					
On-chip debug function		Provided					
Power supply voltage		V_{DD} = 1.6 to 5.5 V (T_A = -40 to +85°C) V_{DD} = 2.4 to 5.5 V (T_A = -40 to +105°C)					
Operating ambient temperature		T_A = 40 to +85°C (A: Consumer applications, D: Industrial applications) T_A = 40 to +105°C (G: Industrial applications)					

<R>

Note   The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$: High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T$_A$ = 25°C

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	1.89	mA
					V$_{DD}$ = 3.0 V		0.62	1.89	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	1.48	mA
					V$_{DD}$ = 3.0 V		0.50	1.48	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.12	mA
					V$_{DD}$ = 3.0 V		0.44	1.12	mA
			LS (low-speed main) mode [Note 7]	f$_{IH}$ = 8 MHz [Note 4]	V$_{DD}$ = 3.0 V		290	620	μA
					V$_{DD}$ = 2.0 V		290	620	μA
			LV (low-voltage main) mode [Note 7]	f$_{IH}$ = 4 MHz [Note 4]	V$_{DD}$ = 3.0 V		460	700	μA
					V$_{DD}$ = 2.0 V		460	700	μA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	1.14	mA
					Resonator connection		0.48	1.34	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	1.14	mA
					Resonator connection		0.48	1.34	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	0.68	mA
					Resonator connection		0.28	0.76	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	0.68	mA
					Resonator connection		0.28	0.76	mA
			LS (low-speed main) mode [Note 7]	f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		110	390	μA
					Resonator connection		160	450	μA
				f$_{MX}$ = 8 MHz [Note 3], V$_{DD}$ = 2.0 V	Square wave input		110	390	μA
					Resonator connection		160	450	μA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.31	0.66	μA
					Resonator connection		0.50	0.85	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.38	0.66	μA
					Resonator connection		0.57	0.85	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.47	3.49	μA
					Resonator connection		0.66	3.68	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.80	6.10	μA
					Resonator connection		0.99	6.29	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.52	10.46	μA
					Resonator connection		1.71	10.65	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]	T$_A$ = −40°C				0.19	0.54	μA
			T$_A$ = +25°C				0.26	0.54	μA
			T$_A$ = +50°C				0.35	3.37	μA
			T$_A$ = +70°C				0.68	5.98	μA
			T$_A$ = +85°C				1.40	10.34	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

　　HS (high-speed main) mode:　2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 32 MHz

　　　　　　　　　　　　　　　　　　2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 16 MHz

　　LS (low-speed main) mode:　　1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 8 MHz

　　LV (low-voltage main) mode:　1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @ 1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.


Remarks 1. f$_{MX}$:　High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:　High-speed on-chip oscillator clock frequency

3. f$_{SUB}$:　Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),

g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

2. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input) (1/2)

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time **Note 5**	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 20 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	8/f$_{MCK}$		—		—		ns
			f$_{MCK}$ ≤ 16 MHz	6/f$_{MCK}$		6/f$_{MCK}$		6/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		6/f$_{MCK}$ and 500		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		6/f$_{MCK}$ and 750		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		6/f$_{MCK}$ and 1500		6/f$_{MCK}$ and 1500		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		t$_{KCY2}$/2 − 7		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		t$_{KCY2}$/2 − 8		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		t$_{KCY2}$/2 − 18		ns
		1.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns
		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V		—		t$_{KCY2}$/2 − 66		t$_{KCY2}$/2 − 66		ns

(**Notes**, **Caution**, and **Remarks** are listed on the next page.)

UART mode bit width (during communication at different potential) (reference)
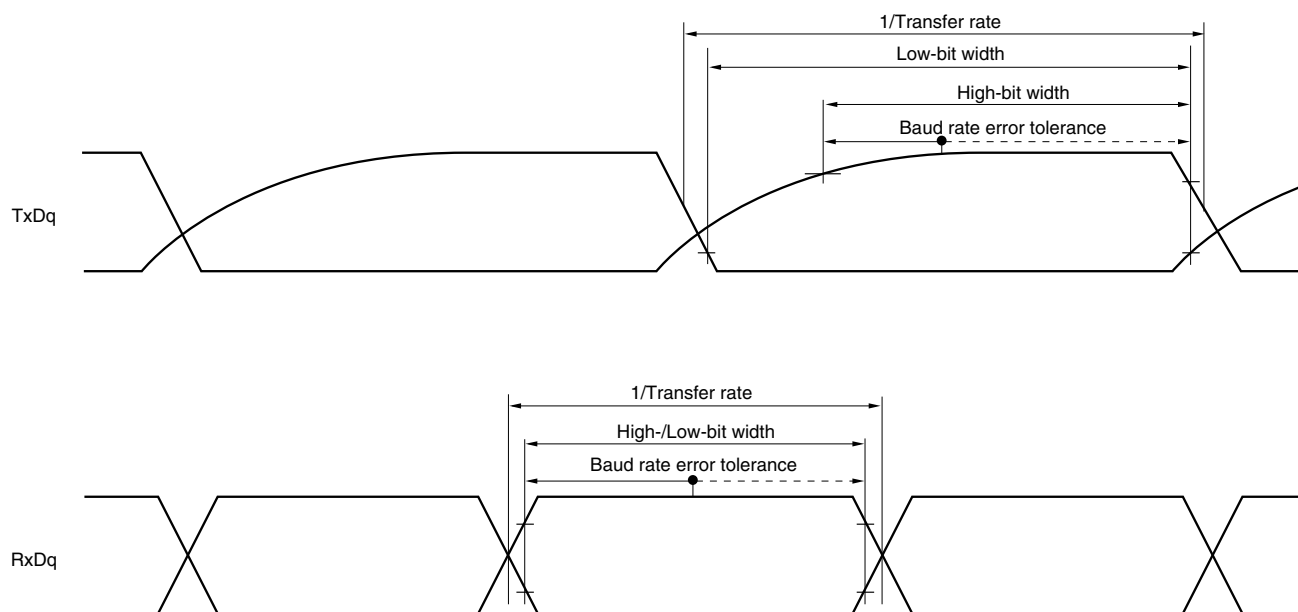
Remarks 1. R$_b$[Ω]:Communication line (TxDq) pull-up resistance,

C$_b$[F]: Communication line (TxDq) load capacitance, V$_b$[V]: Communication line voltage

    2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

    3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

    4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 1]	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) [Note 1]	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output [Note 1]	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V [Note 2], C_b = 30 pF, R_b = 5.5 kΩ		25		25		25	ns

Notes   **1.**   When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

        2.   Use it with EV_{DD0} ≥ V_b.

Caution   **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

2.6.5 Power supply voltage rising slope characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

| Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S$_{VDD}$				54	V/ms

Caution **Make sure to keep the internal reset state by the LVD circuit or an external reset until V$_{DD}$ reaches the operating voltage range shown in 2.4 AC Characteristics.**

2.7 RAM Data Retention Characteristics

(T$_A$ = –40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V$_{DDDR}$		1.46[Note]		5.5	V

Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.
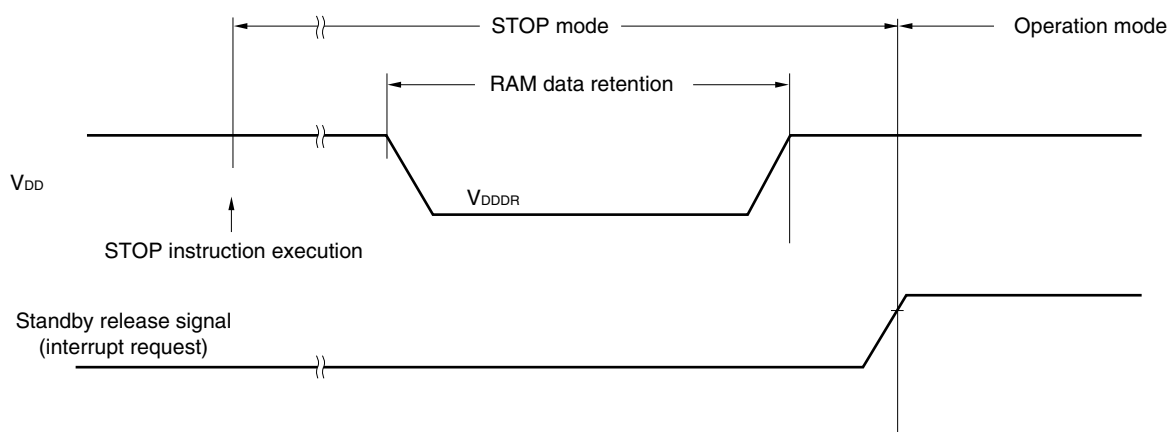
3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS T$_A$ = -40 to +105°C)

This chapter describes the following electrical specifications.

Target products G: Industrial applications T$_A$ = −40 to +105°C

R5F100xxGxx

Cautions 1.   The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

2.   With products not provided with an EV$_{DD0}$, EV$_{DD1}$, EV$_{SS0}$, or EV$_{SS1}$ pin, replace EV$_{DD0}$ and EV$_{DD1}$ with V$_{DD}$, or replace EV$_{SS0}$ and EV$_{SS1}$ with V$_{SS}$.

3.   The pins mounted depend on the product. Refer to 2.1 Port Function to 2.2.1 Functions for each product.

4.   Please contact Renesas Electronics sales office for derating of operation under T$_A$ = +85°C to +105°C. Derating is the systematic reduction of load for the sake of improved reliability.

Remark   When RL78/G13 is used in the range of T$_A$ = −40 to +85°C, see **CHAPTER 2 ELECTRICAL SPECIFICATIONS (T$_A$ = −40 to +85°C)**.

There are following differences between the products "G: Industrial applications (T$_A$ = −40 to +105°C)" and the products "A: Consumer applications, and D: Industrial applications".

| Parameter	Application	
	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	T$_A$ = -40 to +85°C	T$_A$ = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V$_{DD}$ ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V$_{DD}$ ≤ 5.5 V ±1.0%@ T$_A$ = -20 to +85°C ±1.5%@ T$_A$ = -40 to -20°C 1.6 V ≤ V$_{DD}$ < 1.8 V ±5.0%@ T$_A$ = -20 to +85°C ±5.5%@ T$_A$ = -40 to -20°C	2.4 V ≤ V$_{DD}$ ≤ 5.5 V ±2.0%@ T$_A$ = +85 to +105°C ±1.0%@ T$_A$ = -20 to +85°C ±1.5%@ T$_A$ = -40 to -20°C
Serial array unit	UART CSI: f$_{CLK}$/2 (supporting 16 Mbps), f$_{CLK}$/4 Simplified I^{2}C communication	UART CSI: f$_{CLK}$/4 Simplified I^{2}C communication
IICA	Normal mode Fast mode Fast mode plus	Normal mode Fast mode
Voltage detector	Rise detection voltage: 1.67 V to 4.06 V (14 levels) Fall detection voltage: 1.63 V to 3.98 V (14 levels)	Rise detection voltage: 2.61 V to 4.06 V (8 levels) Fall detection voltage: 2.55 V to 3.98 V (8 levels)

(**Remark** is listed on the next page.)

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (4/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V$_{OH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −3.0 mA	EV$_{DD0}$ − 0.7			V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −2.0 mA	EV$_{DD0}$ − 0.6			V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OH1}$ = −1.5 mA	EV$_{DD0}$ − 0.5			V
	V$_{OH2}$	P20 to P27, P150 to P156	2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OH2}$ = −100 μA	V$_{DD}$ − 0.5			V
Output voltage, low	V$_{OL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 8.5 mA			0.7	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 3.0 mA			0.6	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 1.5 mA			0.4	V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL1}$ = 0.6 mA			0.4	V
	V$_{OL2}$	P20 to P27, P150 to P156	2.4 V ≤ V$_{DD}$ ≤ 5.5 V, I$_{OL2}$ = 400 μA			0.4	V
	V$_{OL3}$	P60 to P63	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 15.0 mA			2.0	V
			4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 5.0 mA			0.4	V
			2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 3.0 mA			0.4	V
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V, I$_{OL3}$ = 2.0 mA			0.4	V

Caution **P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Simplified I^{2}C mode mode connection diagram (during communication at same potential)
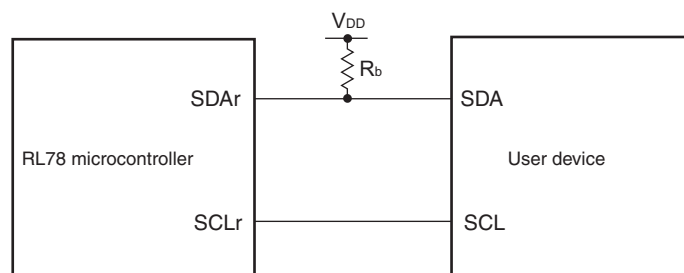
Simplified I^{2}C mode serial transfer timing (during communication at same potential)
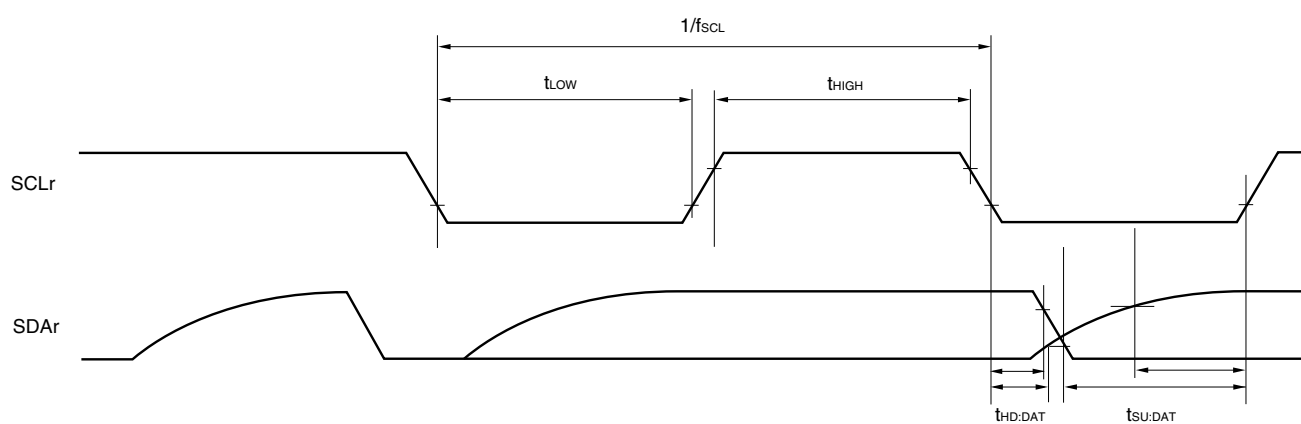
Remarks 1. R$_b$[Ω]:Communication line (SDAr) pull-up resistance, C$_b$[F]: Communication line (SDAr, SCLr) load capacitance

      2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)

      3. f$_{MCK}$: Serial array unit operation clock frequency

        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T_A = –40 to +105°C, 2.4 V $\leq$ EV_{DD0} = EV_{DD1} $\leq$ V_{DD} $\leq$ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Reception	4.0 V $\leq$ EV_{DD0} $\leq$ 5.5 V, 2.7 V $\leq$ V_b $\leq$ 4.0 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps
			2.7 V $\leq$ EV_{DD0} < 4.0 V, 2.3 V $\leq$ V_b $\leq$ 2.7 V			f_{MCK}/12 [Note 1]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps
			2.4 V $\leq$ EV_{DD0} < 3.3 V, 1.6 V $\leq$ V_b $\leq$ 2.0 V			f_{MCK}/12 [Notes 1,2]	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}		2.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V $\leq$ EV_{DD0} < 2.7 V : MAX. 1.3 Mbps

Caution **Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.**

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

**3.** f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
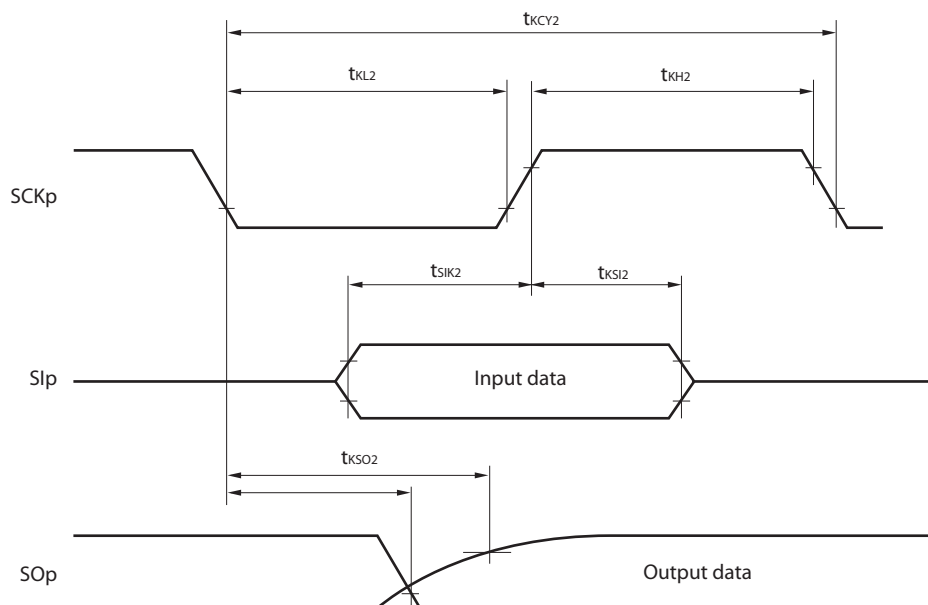
CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
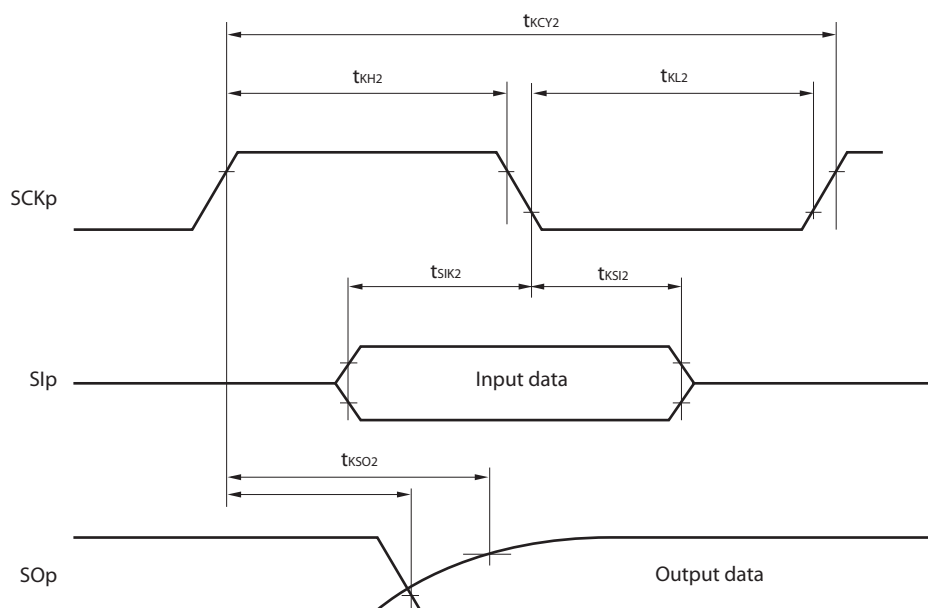
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,

n: Channel number (mn = 00, 01, 02, 10. 12. 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.

Use other CSI for communication at different potential.

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV$_{REFP}$ Reference voltage (−) = AV$_{REFM}$	Reference voltage (+) = V$_{DD}$ Reference voltage (−) = V$_{SS}$	Reference voltage (+) = V$_{BGR}$ Reference voltage (−) = AV$_{REFM}$
ANI0 to ANI14	Refer to **3.6.1 (1)**.	Refer to **3.6.1 (3)**.	Refer to **3.6.1 (4)**.
ANI16 to ANI26	Refer to **3.6.1 (2)**.		
Internal reference voltage Temperature sensor output voltage	Refer to **3.6.1 (1)**.		−

(1) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(T$_A$ = −40 to +105°C, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.25	%FSR
Integral linearity error [Note 1]	ILE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution AV$_{REFP}$ = V$_{DD}$ [Note 3]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±1.5	LSB
Analog input voltage	V$_{AIN}$	ANI2 to ANI14		0		AV$_{REFP}$	V
		Internal reference voltage output (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{BGR}$ [Note 4]		V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)			V$_{TMPS25}$ [Note 4]		V

(**Notes** are listed on the next page.)

(2) When reference voltage (+) = AV$_{REFP}$/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (−) = AV$_{REFM}$/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, 2.4 V ≤ AV$_{REFP}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = AV$_{REFP}$, Reference voltage (−) = AV$_{REFM}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin : ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	µs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	µs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	µs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±0.35	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±3.5	LSB
Differential linearity error [Note 1]	DLE	10-bit resolution EV$_{DD0}$ ≤ AV$_{REFP}$ = V$_{DD}$ [Notes 3, 4]	2.4 V ≤ AV$_{REFP}$ ≤ 5.5 V			±2.0	LSB
Analog input voltage	V$_{AIN}$	ANI16 to ANI26		0		AV$_{REFP}$ and EV$_{DD0}$	V

Notes 1. Excludes quantization error (±1/2 LSB).
   2. This value is indicated as a ratio (%FSR) to the full-scale value.
   3. When AV$_{REFP}$ < V$_{DD}$, the MAX. values are as follows.
   Overall error: Add ±1.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
   Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
   Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
   4. When AV$_{REFP}$ < EV$_{DD0}$ ≤ V$_{DD}$, the MAX. values are as follows.
   Overall error: Add ±4.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
   Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV$_{REFP}$ = V$_{DD}$.
   Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV$_{REFP}$ = V$_{DD}$.

3.8 Flash Memory Programming Characteristics

(T$_A$ = –40 to +105°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f$_{CLK}$	2.4 V ≤ V$_{DD}$ ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1,2,3	C$_{erwr}$	Retained for 20 years T$_A$ = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1,2,3		Retained for 1 years T$_A$ = 25°C		1,000,000		
		Retained for 5 years T$_A$ = 85°C Note 4	100,000			
		Retained for 20 years T$_A$ = 85°C Note 4	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.The retaining years are until next rewrite after the rewrite.
    2. When using flash memory programmer and Renesas Electronics self programming library.
    3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
    4. This temperature is the average value at which data are retained.

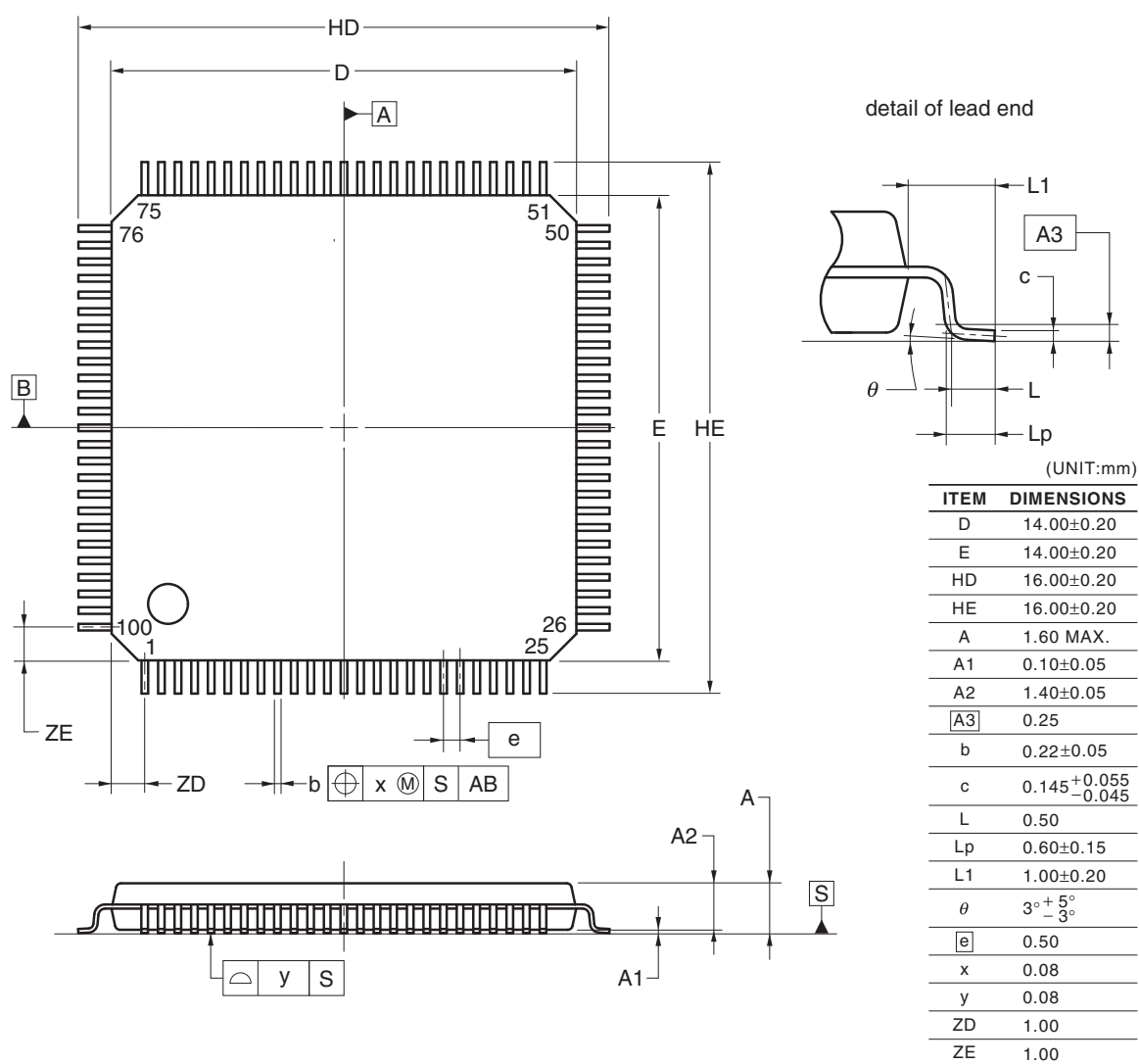## 3.9 Dedicated Flash Memory Programmer Communication (UART)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00