Details

Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gfdfb-50

1.3.5 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)
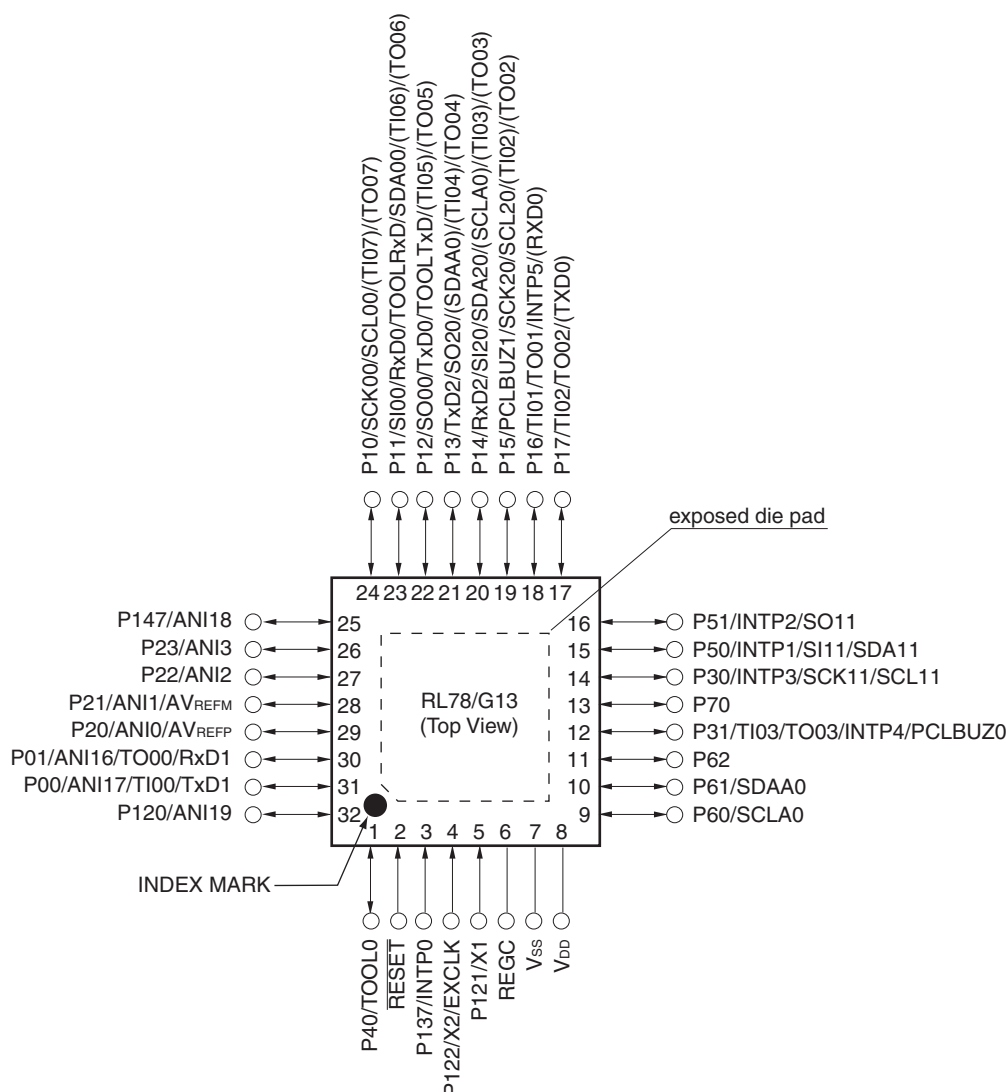
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

    2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

    3. It is recommended to connect an exposed die pad to Vss.

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)

Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5 Block Diagram

1.5.1 20-pin products

1.5.8 44-pin products

TIMER ARRAY UNIT (8ch)
- ch0 — TI00/P00, TO00/P01
- ch1 — TI01/TO01/P16
- ch2 — TI02/TO02/P17 (TI02/TO02/P15)
- ch3 — TI03/TO03/P31 (TI03/TO03/P14)
- ch4 — (TI04/TO04/P13)
- ch5 — (TI05/TO05/P12)
- ch6 — (TI06/TO06/P11)
- ch7 — TI07/TO07/P41 (TI07/TO07/P10), RxD2/P14

WINDOW WATCHDOG TIMER

12-BIT INTERVAL TIMER — LOW-SPEED ON-CHIP OSCILLATOR

REAL-TIME CLOCK — RTC1HZ/P30

SERIAL ARRAY UNIT0 (4ch)
- UART0 — RxD0/P11(RxD0/P16), TxD0/P12(TxD0/P17)
- UART1 — RxD1/P01, TxD1/P00
- CSI00 — SCK00/P10, SI00/P11, SO00/P12
- CSI11 — SCK11/P30, SI11/P50, SO11/P51
- IIC00 — SCL00/P10, SDA00/P11
- IIC11 — SCL11/P30, SDA11/P50

SERIAL ARRAY UNIT1 (2ch)
- UART2 (LINSEL) — RxD2/P14, TxD2/P13
- CSI20 — SCK20/P15, SI20/P14, SO20/P13
- CSI21 — SCK21/P70, SI21/P71, SO21/P72
- IIC20 — SCL20/P15, SDA20/P14
- IIC21 — SCL21/P70, SDA21/P71

RL78 CPU CORE
- CODE FLASH MEMORY
- DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13), SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT / CLOCK OUTPUT CONTROL — PCLBUZ0/P31, PCLBUZ1/P15

MULTIPLIER & DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — P00, P01
PORT 1 — P10 to P17
PORT 2 — P20 to P27
PORT 3 — P30, P31
PORT 4 — P40, P41
PORT 5 — P50, P51
PORT 6 — P60 to P63
PORT 7 — P70 to P73
PORT 12 — P120, P121 to P124
PORT 13 — P137
PORT 14 — P146, P147

A/D CONVERTER — ANI0/P20 to ANI7/P27, ANI18/P147, ANI19/P120, AV_{REFP}/P20, AV_{REFM}/P21

KEY RETURN — KR0/P70 to KR3/P73

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL / HIGH-SPEED ON-CHIP OSCILLATOR — RESET, X1/P121, X2/EXCLK/P122, XT1/P123, XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

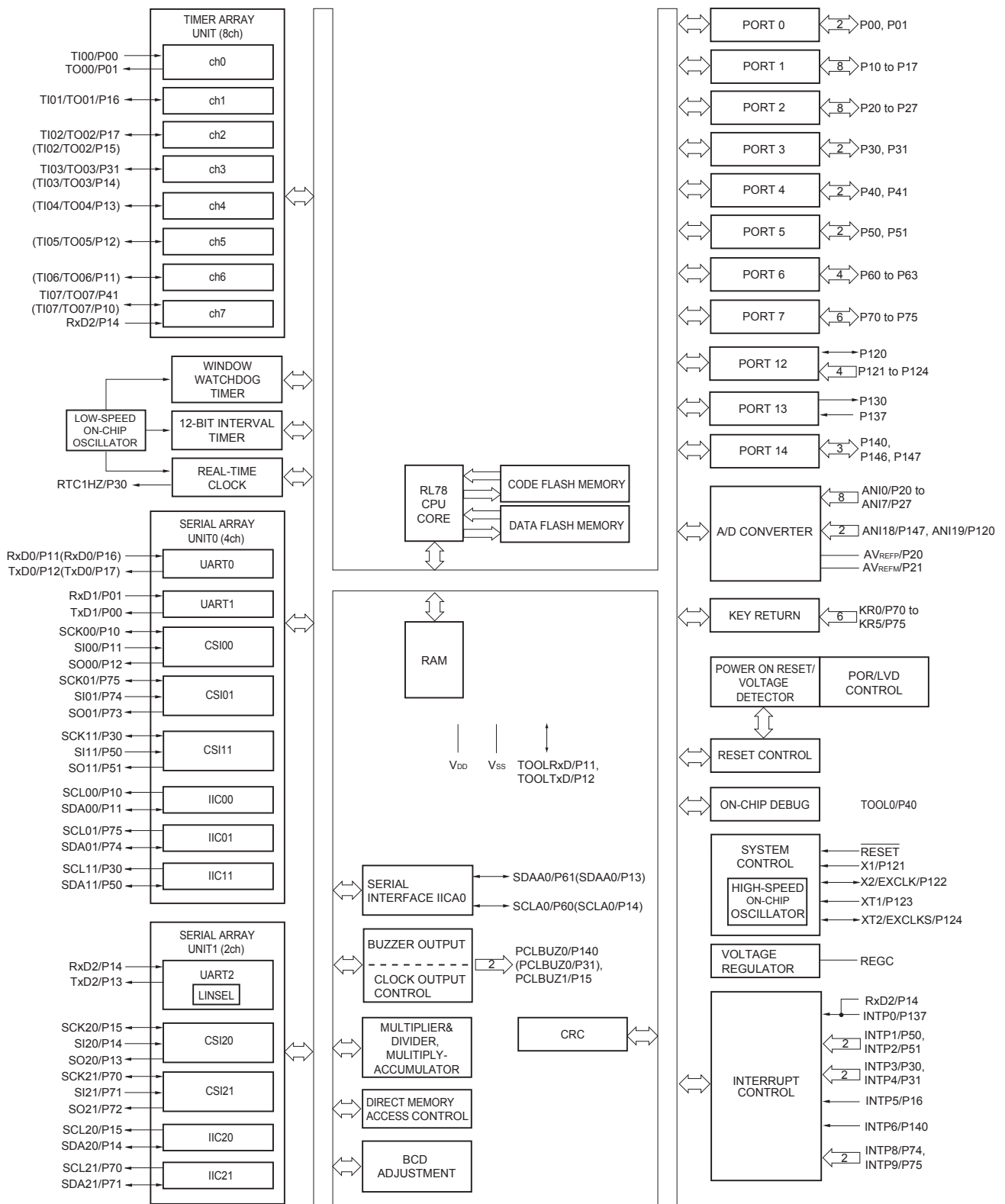INTERRUPT CONTROL — RxD2/P14, INTP0/P137, INTP1/P50, INTP2/P51, INTP3/P30, INTP4/P31, INTP5/P16
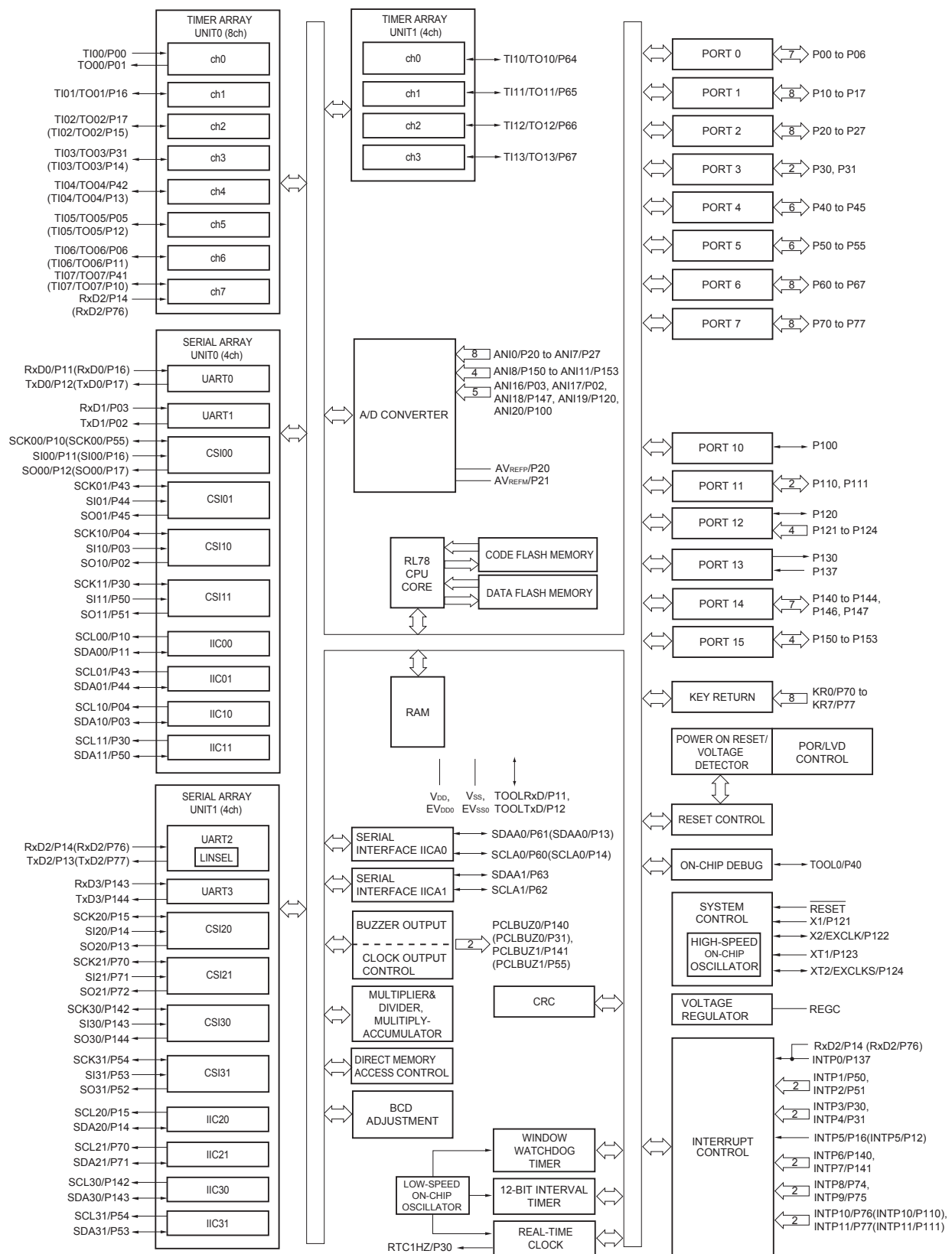
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.9 48-pin products

TIMER ARRAY UNIT (8ch)

TI00/P00 — ch0
TO00/P01

TI01/TO01/P16 — ch1

TI02/TO02/P17 — ch2
(TI02/TO02/P15)

TI03/TO03/P31 — ch3
(TI03/TO03/P14)

(TI04/TO04/P13) — ch4

(TI05/TO05/P12) — ch5

(TI06/TO06/P11) — ch6

TI07/TO07/P41 — ch7
(TI07/TO07/P10)
RxD2/P14

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR

12-BIT INTERVAL TIMER

RTC1HZ/P30 — REAL-TIME CLOCK

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16) — UART0
TxD0/P12(TxD0/P17)

RxD1/P01 — UART1
TxD1/P00

SCK00/P10 — CSI00
SI00/P11
SO00/P12

SCK01/P75 — CSI01
SI01/P74
SO01/P73

SCK11/P30 — CSI11
SI11/P50
SO11/P51

SCL00/P10 — IIC00
SDA00/P11

SCL01/P75 — IIC01
SDA01/P74

SCL11/P30 — IIC11
SDA11/P50

SERIAL ARRAY UNIT1 (2ch)

RxD2/P14 — UART2
TxD2/P13
LINSEL

SCK20/P15 — CSI20
SI20/P14
SO20/P13

SCK21/P70 — CSI21
SI21/P71
SO21/P72

SCL20/P15 — IIC20
SDA20/P14

SCL21/P70 — IIC21
SDA21/P71

RL78 CPU CORE
CODE FLASH MEMORY
DATA FLASH MEMORY

RAM

V_{DD} V_{SS} TOOLRxD/P11, TOOLTxD/P12

SERIAL INTERFACE IICA0 — SDAA0/P61(SDAA0/P13)
— SCLA0/P60(SCLA0/P14)

BUZZER OUTPUT
CLOCK OUTPUT CONTROL — 2 — PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P15

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

PORT 0 — 2 — P00, P01
PORT 1 — 8 — P10 to P17
PORT 2 — 8 — P20 to P27
PORT 3 — 2 — P30, P31
PORT 4 — 2 — P40, P41
PORT 5 — 2 — P50, P51
PORT 6 — 4 — P60 to P63
PORT 7 — 6 — P70 to P75
PORT 12 — P120 / 4 — P121 to P124
PORT 13 — P130 / P137
PORT 14 — 3 — P140, P146, P147

A/D CONVERTER — 8 — ANI0/P20 to ANI7/P27
— 2 — ANI18/P147, ANI19/P120
— AV_REFP/P20
— AV_REFM/P21

KEY RETURN — 6 — KR0/P70 to KR5/P75

POWER ON RESET/ VOLTAGE DETECTOR — POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG — TOOL0/P40

SYSTEM CONTROL — RESET
— X1/P121
HIGH-SPEED ON-CHIP OSCILLATOR — X2/EXCLK/P122
— XT1/P123
— XT2/EXCLKS/P124

VOLTAGE REGULATOR — REGC

INTERRUPT CONTROL
— RxD2/P14
— INTP0/P137
— 2 — INTP1/P50, INTP2/P51
— 2 — INTP3/P30, INTP4/P31
— INTP5/P16
— INTP6/P140
— 2 — INTP8/P74, INTP9/P75

Remark　Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.12 80-pin products

TIMER ARRAY UNIT0 (8ch)

TI00/P00
TO00/P01 → ch0

TI01/TO01/P16 → ch1

TI02/TO02/P17
(TI02/TO02/P15) → ch2

TI03/TO03/P31
(TI03/TO03/P14) → ch3

TI04/TO04/P42
(TI04/TO04/P13) → ch4

TI05/TO05/P05
(TI05/TO05/P12) → ch5

TI06/TO06/P06
(TI06/TO06/P11) → ch6

TI07/TO07/P41
(TI07/TO07/P10)
RxD2/P14
(RxD2/P76) → ch7

TIMER ARRAY UNIT1 (4ch)

ch0 → TI10/TO10/P64
ch1 → TI11/TO11/P65
ch2 → TI12/TO12/P66
ch3 → TI13/TO13/P67

SERIAL ARRAY UNIT0 (4ch)

RxD0/P11(RxD0/P16)
TxD0/P12(TxD0/P17) → UART0

RxD1/P03
TxD1/P02 → UART1

SCK00/P10(SCK00/P55)
SI00/P11(SI00/P16)
SO00/P12(SO00/P17) → CSI00

SCK01/P43
SI01/P44
SO01/P45 → CSI01

SCK10/P04
SI10/P03
SO10/P02 → CSI10

SCK11/P30
SI11/P50
SO11/P51 → CSI11

SCL00/P10
SDA00/P11 → IIC00

SCL01/P43
SDA01/P44 → IIC01

SCL10/P04
SDA10/P03 → IIC10

SCL11/P30
SDA11/P50 → IIC11

SERIAL ARRAY UNIT1 (4ch)

RxD2/P14(RxD2/P76)
TxD2/P13(TxD2/P77) → UART2 LINSEL

RxD3/P143
TxD3/P144 → UART3

SCK20/P15
SI20/P14
SO20/P13 → CSI20

SCK21/P70
SI21/P71
SO21/P72 → CSI21

SCK30/P142
SI30/P143
SO30/P144 → CSI30

SCK31/P54
SI31/P53
SO31/P52 → CSI31

SCL20/P15
SDA20/P14 → IIC20

SCL21/P70
SDA21/P71 → IIC21

SCL30/P142
SDA30/P143 → IIC30

SCL31/P54
SDA31/P53 → IIC31

A/D CONVERTER
8 ANI0/P20 to ANI7/P27
4 ANI8/P150 to ANI11/P153
5 ANI16/P03, ANI17/P02, ANI18/P147, ANI19/P120, ANI20/P100
AV$_{REFP}$/P20
AV$_{REFM}$/P21

RL78 CPU CORE
CODE FLASH MEMORY
DATA FLASH MEMORY

RAM

V$_{DD}$, V$_{SS}$, TOOLRxD/P11,
EV$_{DD0}$ EV$_{SS0}$ TOOLTxD/P12

SERIAL INTERFACE IICA0 → SDAA0/P61(SDAA0/P13)
SCLA0/P60(SCLA0/P14)

SERIAL INTERFACE IICA1 → SDAA1/P63
SCLA1/P62

BUZZER OUTPUT
- - - - - - -
CLOCK OUTPUT CONTROL → 2 PCLBUZ0/P140 (PCLBUZ0/P31), PCLBUZ1/P141 (PCLBUZ1/P55)

MULTIPLIER& DIVIDER, MULITIPLY-ACCUMULATOR

CRC

DIRECT MEMORY ACCESS CONTROL

BCD ADJUSTMENT

WINDOW WATCHDOG TIMER

LOW-SPEED ON-CHIP OSCILLATOR → 12-BIT INTERVAL TIMER

RTC1HZ/P30 ← REAL-TIME CLOCK

PORT 0 → 7 P00 to P06
PORT 1 → 8 P10 to P17
PORT 2 → 8 P20 to P27
PORT 3 → 2 P30, P31
PORT 4 → 6 P40 to P45
PORT 5 → 6 P50 to P55
PORT 6 → 8 P60 to P67
PORT 7 → 8 P70 to P77

PORT 10 → P100
PORT 11 → 2 P110, P111
PORT 12 → P120 / 4 P121 to P124
PORT 13 → P130 / P137
PORT 14 → 7 P140 to P144, P146, P147
PORT 15 → 4 P150 to P153

KEY RETURN → 8 KR0/P70 to KR7/P77

POWER ON RESET/ VOLTAGE DETECTOR   POR/LVD CONTROL

RESET CONTROL

ON-CHIP DEBUG → TOOL0/P40

SYSTEM CONTROL
HIGH-SPEED ON-CHIP OSCILLATOR
RESET
X1/P121
X2/EXCLK/P122
XT1/P123
XT2/EXCLKS/P124

VOLTAGE REGULATOR → REGC

INTERRUPT CONTROL
RxD2/P14 (RxD2/P76)
INTP0/P137
2 INTP1/P50, INTP2/P51
2 INTP3/P30, INTP4/P31
INTP5/P16(INTP5/P12)
2 INTP6/P140, INTP7/P141
2 INTP8/P74, INTP9/P75
2 INTP10/P76(INTP10/P110), INTP11/P77(INTP11/P111)

Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

Notes 1. Total current flowing into V$_{DD}$ and EV$_{DD0}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$ or V$_{SS}$, EV$_{SS0}$. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

 2. During HALT instruction execution by flash memory.

 3. When high-speed on-chip oscillator and subsystem clock are stopped.

 4. When high-speed system clock and subsystem clock are stopped.

 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

 6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

  HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 32 MHz

             2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 16 MHz

  LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 8 MHz

  LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 4 MHz

 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

 2. f$_{IH}$: High-speed on-chip oscillator clock frequency

 3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = −40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fIH = 32 MHz Note 4	VDD = 5.0 V		0.62	1.86	mA
					VDD = 3.0 V		0.62	1.86	mA
				fIH = 24 MHz Note 4	VDD = 5.0 V		0.50	1.45	mA
					VDD = 3.0 V		0.50	1.45	mA
				fIH = 16 MHz Note 4	VDD = 5.0 V		0.44	1.11	mA
					VDD = 3.0 V		0.44	1.11	mA
			LS (low-speed main) mode Note 7	fIH = 8 MHz Note 4	VDD = 3.0 V		290	620	μA
					VDD = 2.0 V		290	620	μA
			LV (low-voltage main) mode Note 7	fIH = 4 MHz Note 4	VDD = 3.0 V		440	680	μA
					VDD = 2.0 V		440	680	μA
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.21	0.63	mA
					Resonator connection		0.28	0.71	mA
			LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
				fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	fSUB = 32.768 kHz Note 5, TA = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
	IDD3 Note 6	STOP mode Note 8	TA = −40°C				0.19	0.52	μA
			TA = +25°C				0.25	0.52	μA
			TA = +50°C				0.32	2.21	μA
			TA = +70°C				0.55	3.94	μA
			TA = +85°C				1.00	7.95	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, including the input leakage current flowing when the level of the input pin is fixed to V$_{DD}$, EV$_{DD0}$, and EV$_{DD1}$, or V$_{SS}$, EV$_{SS0}$, and EV$_{SS1}$. The values below the MAX. column include the peripheral operation current . However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.

6. Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

> HS (high-speed main) mode: 2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 32 MHz
>
> 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 16 MHz
>
> LS (low-speed main) mode: 1.8 V $\leq$ V$_{DD}$ $\leq$ 5.5 V @1 MHz to 8 MHz
>
> LV (low-voltage main) mode: 1.6 V $\leq$ V$_{DD}$ $\leq$ 5.5 V@1 MHz to 4 MHz

8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

Remarks 1. f$_{MX}$: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f$_{IH}$:   High-speed on-chip oscillator clock frequency

3. f$_{SUB}$: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T$_A$ = 25°C

(4) Peripheral Functions (Common to all products)

(T$_A$ = −40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I$_{FIL}$[Note 1]				0.20		µA
RTC operating current	I$_{RTC}$ [Notes 1, 2, 3]				0.02		µA
12-bit interval timer operating current	I$_{IT}$ [Notes 1, 2, 4]				0.02		µA
Watchdog timer operating current	I$_{WDT}$ [Notes 1, 2, 5]	f$_{IL}$ = 15 kHz			0.22		µA
A/D converter operating current	I$_{ADC}$ [Notes 1, 6]	When conversion at maximum speed	Normal mode, AV$_{REFP}$ = V$_{DD}$ = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I$_{ADREF}$ [Note 1]				75.0		µA
Temperature sensor operating current	I$_{TMPS}$ [Note 1]				75.0		µA
LVD operating current	I$_{LVI}$ [Notes 1, 7]				0.08		µA
Self-programming operating current	I$_{FSP}$ [Notes 1, 9]				2.50	12.20	mA
BGO operating current	I$_{BGO}$ [Notes 1, 8]				2.50	12.20	mA
SNOOZE operating current	I$_{SNOZ}$ [Note 1]	ADC operation	The mode is performed[Note 10]		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AV$_{REFP}$ = V$_{DD}$ = 3.0 V		1.20	1.44	mA
		CSI/UART operation			0.70	0.84	mA

Notes 1. Current flowing to V$_{DD}$.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{RTC}$, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added. I$_{DD2}$ subsystem clock operation includes the operational current of the real-time clock.

4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I$_{DD1}$ or I$_{DD2}$, and I$_{IT}$, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I$_{FIL}$ should be added.

5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I$_{DD1}$, I$_{DD2}$ or I$_{DD3}$ and I$_{WDT}$ when the watchdog timer is in operation.

(5) During communication at same potential (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 85 Note2		1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		1/f$_{MCK}$ + 145 Note2		ns
		1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 230 Note2		1/f$_{MCK}$ + 230 Note2		1/f$_{MCK}$ + 230 Note2		ns
		1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		ns
		1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		1/f$_{MCK}$ + 290 Note2		1/f$_{MCK}$ + 290 Note2		ns
Data hold time (transmission)	t$_{HD:DAT}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V, C$_b$ = 100 pF, R$_b$ = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV$_{DD0}$ < 2.7 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV$_{DD0}$ < 1.8 V, C$_b$ = 100 pF, R$_b$ = 5 kΩ	—		0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

**2.** Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   Select the normal input buffer and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(**Remarks** are listed on the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (1/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
					MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate		Reception	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V			f$_{MCK}$/6 Note 1		f$_{MCK}$/6 Note 1		f$_{MCK}$/6 Note 1	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$Note 4		5.3		1.3		0.6	Mbps
			2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V			f$_{MCK}$/6 Note 1		f$_{MCK}$/6 Note 1		f$_{MCK}$/6 Note 1	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$Note 4		5.3		1.3		0.6	Mbps
			1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V			f$_{MCK}$/6 Notes 1 to 3		f$_{MCK}$/6 Notes 1, 2		f$_{MCK}$/6 Notes 1, 2	bps
				Theoretical value of the maximum transfer rate f$_{MCK}$ = f$_{CLK}$Note 4		5.3		1.3		0.6	Mbps

Notes 1. Transfer rate in the SNOOZE mode is 4800 bps only.

2. Use it with EV$_{DD0}$≥V$_b$.

3. The following conditions are required for low voltage interface when E$_{VDD0}$ < V$_{DD}$.

2.4 V ≤ EV$_{DD0}$ < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ EV$_{DD0}$ < 2.4 V : MAX. 1.3 Mbps

4. The maximum operating frequencies of the CPU/peripheral hardware clock (f$_{CLK}$) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ V$_{DD}$ ≤ 5.5 V)

16 MHz (2.4 V ≤ V$_{DD}$ ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ V$_{DD}$ ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ V$_{DD}$ ≤ 5.5 V)

Caution   Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.

Remarks 1. V$_b$[V]: Communication line voltage

2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

3. f$_{MCK}$: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

4. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
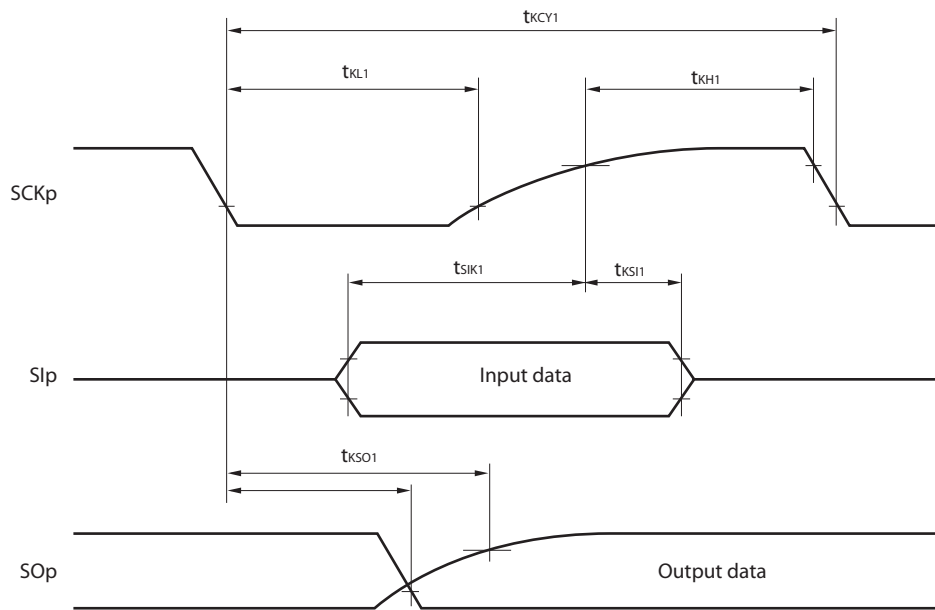
CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)
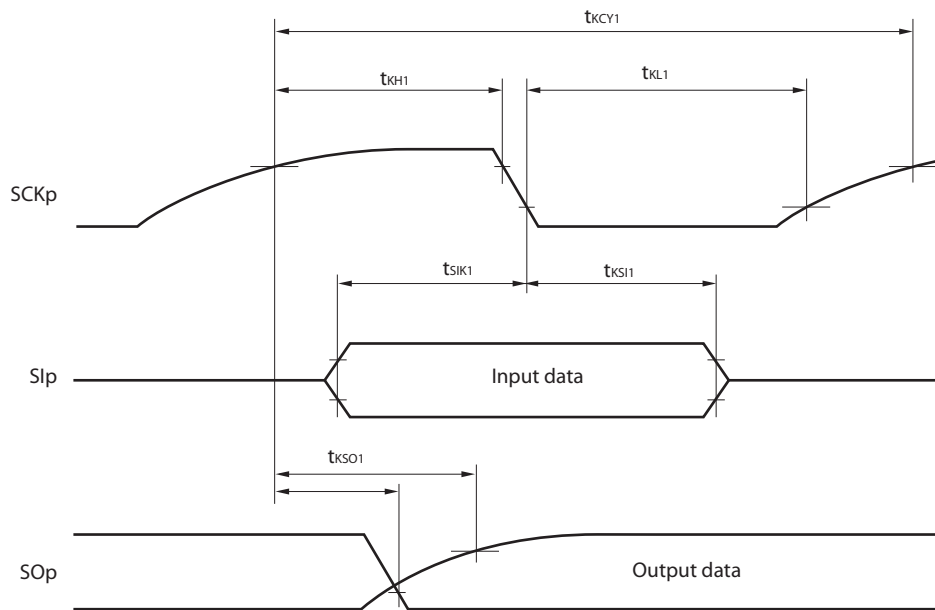
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

    2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (2/2)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	t$_{SU:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 135 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		1/f$_{MCK}$ + 190 [Note 3]		kHz
Data hold time (transmission)	t$_{HD:DAT}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	0	405	0	405	0	405	ns

Notes 1. The value must also be equal to or less than f$_{MCK}$/4.

    2. Use it with EV$_{DD0}$ ≥ V$_b$.

    3. Set the f$_{MCK}$ value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution   **Select the TTL input buffer and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(**Remarks** are listed on the next page.)

2.6.2 Temperature sensor/internal reference voltage characteristics

(T$_A$ = −40 to +85°C, 2.4 V ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V$_{TMPS25}$	Setting ADS register = 80H, T$_A$ = +25°C		1.05		V
Internal reference voltage	V$_{BGR}$	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F$_{VTMPS}$	Temperature sensor that depends on the temperature		−3.6		mV/°C
Operation stabilization wait time	t$_{AMP}$		5			μs

2.6.3 POR circuit characteristics

(T$_A$ = −40 to +85°C, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V$_{POR}$	Power supply rise time	1.47	1.51	1.55	V
	V$_{PDR}$	Power supply fall time	1.46	1.50	1.54	V
Minimum pulse width[Note]	T$_{PW}$		300			μs

Note Minimum time required for a POR reset when V$_{DD}$ exceeds below V$_{PDR}$. This is also the minimum time required for a POR reset from when V$_{DD}$ exceeds below 0.7 V to when V$_{DD}$ exceeds V$_{POR}$ while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).
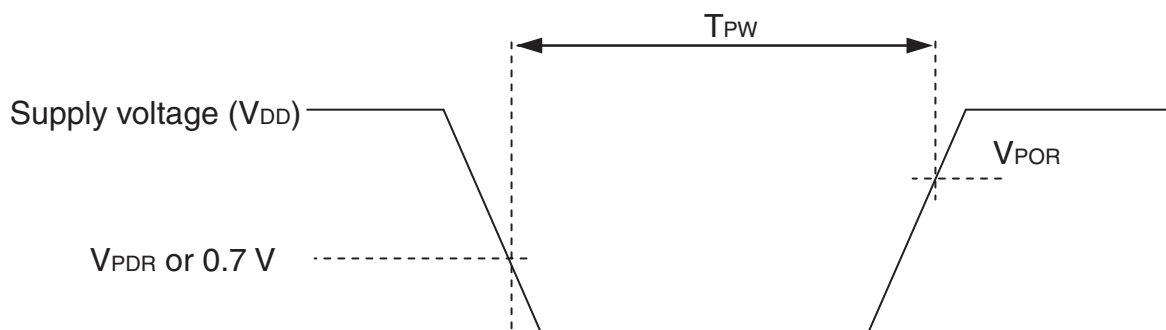
3.2 Oscillator Characteristics

3.2.1 X1, XT1 oscillator characteristics

(T$_A$ = –40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f$_X$)^{Note}	Ceramic resonator/ crystal resonator	2.7 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	1.0		20.0	MHz
		2.4 V $\leq$ V$_{DD}$ < 2.7 V	1.0		16.0	MHz
XT1 clock oscillation frequency (f$_X$)^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to AC Characteristics for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution **Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.**

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator**.

3.2.2 On-chip oscillator characteristics

(T$_A$ = –40 to +105°C, 2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V, V$_{SS}$ = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency $^{Notes 1, 2}$	f$_{IH}$			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		−20 to +85 °C	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	−1.0		+1.0	%
		−40 to −20 °C	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	−1.5		+1.5	%
		+85 to +105 °C	2.4 V $\leq$ V$_{DD}$ $\leq$ 5.5 V	−2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f$_{IL}$				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				−15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.
2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(T$_A$ = −40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (2/2)

| Parameter	Symbol			Conditions		MIN.	TYP.	MAX.	Unit
Supply current [Note 1]	I$_{DD2}$ [Note 2]	HALT mode	HS (high-speed main) mode [Note 7]	f$_{IH}$ = 32 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.62	3.40	mA
					V$_{DD}$ = 3.0 V		0.62	3.40	mA
				f$_{IH}$ = 24 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.50	2.70	mA
					V$_{DD}$ = 3.0 V		0.50	2.70	mA
				f$_{IH}$ = 16 MHz [Note 4]	V$_{DD}$ = 5.0 V		0.44	1.90	mA
					V$_{DD}$ = 3.0 V		0.44	1.90	mA
			HS (high-speed main) mode [Note 7]	f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 20 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.31	2.10	mA
					Resonator connection		0.48	2.20	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 5.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
				f$_{MX}$ = 10 MHz [Note 3], V$_{DD}$ = 3.0 V	Square wave input		0.21	1.10	mA
					Resonator connection		0.28	1.20	mA
			Subsystem clock operation	f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = −40°C	Square wave input		0.28	0.61	μA
					Resonator connection		0.47	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +25°C	Square wave input		0.34	0.61	μA
					Resonator connection		0.53	0.80	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +50°C	Square wave input		0.41	2.30	μA
					Resonator connection		0.60	2.49	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +70°C	Square wave input		0.64	4.03	μA
					Resonator connection		0.83	4.22	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +85°C	Square wave input		1.09	8.04	μA
					Resonator connection		1.28	8.23	μA
				f$_{SUB}$ = 32.768 kHz [Note 5] T$_A$ = +105°C	Square wave input		5.50	41.00	μA
					Resonator connection		5.50	41.00	μA
	I$_{DD3}$ [Note 6]	STOP mode [Note 8]		T$_A$ = −40°C			0.19	0.52	μA
				T$_A$ = +25°C			0.25	0.52	μA
				T$_A$ = +50°C			0.32	2.21	μA
				T$_A$ = +70°C			0.55	3.94	μA
				T$_A$ = +85°C			1.00	7.95	μA
				T$_A$ = +105°C			5.00	40.00	μA

(**Notes** and **Remarks** are listed on the next page.)

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		Unit
				MIN.	MAX.	
SCKp cycle time [Note 5]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	20 MHz < f$_{MCK}$	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 20 MHz	12/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V	16 MHz < f$_{MCK}$	16/f$_{MCK}$		ns
			f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		16/f$_{MCK}$		ns
				12/f$_{MCK}$ and 1000		ns
SCKp high-/low-level width	t$_{KH2}$, t$_{KL2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 14		ns
		2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 16		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		t$_{KCY2}$/2 − 36		ns
SIp setup time (to SCKp↑) [Note 1]	t$_{SIK2}$	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+40		ns
		2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+60		ns
SIp hold time (from SCKp↑) [Note 2]	t$_{KSI2}$	2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		1/f$_{MCK}$+62		ns
Delay time from SCKp↓ to SOp output [Note 3]	t$_{KSO2}$	C = 30 pF [Note 4]	2.7 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+66	ns
			2.4 V ≤ EV$_{DD0}$ ≤ 5.5 V		2/f$_{MCK}$+113	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

    4. C is the load capacitance of the SOp output lines.

    5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the normal input buffer for the SIp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
        n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 4, 5, 8, 14)

    2. f$_{MCK}$: Serial array unit operation clock frequency

        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
   n: Channel number (mn = 00 to 03, 10 to 13))

CSI mode connection diagram (during communication at same potential)
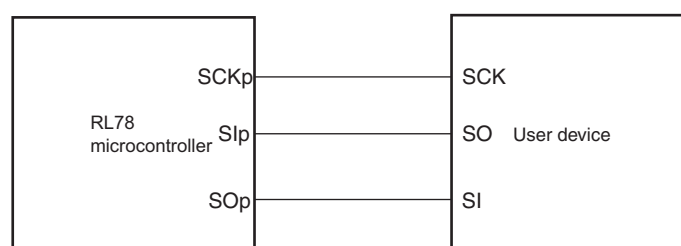
Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

  2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

  3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

  4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution **Select the TTL input buffer for the SIp pin and SCKp pin and the N-ch open drain output (V$_{DD}$ tolerance (for the 20- to 52-pin products)/EV$_{DD}$ tolerance (for the 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**
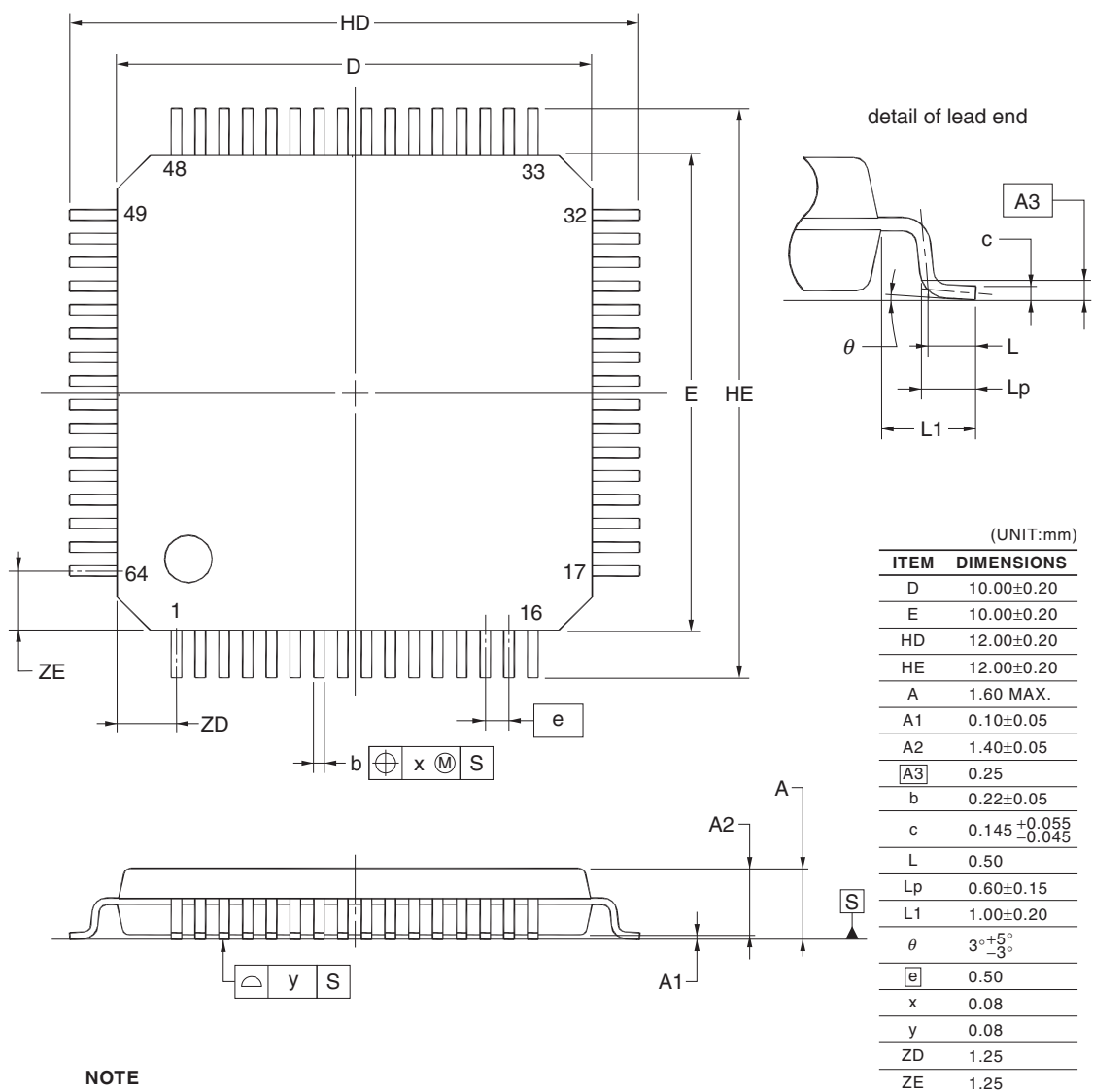
CSI mode connection diagram (during communication at different potential)
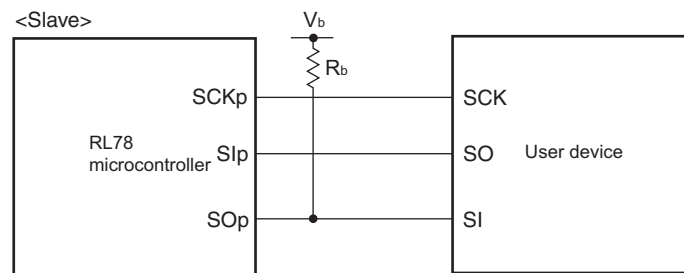
Remarks 1. R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load capacitance, V$_b$[V]: Communication line voltage

  2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02,

  10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

  3. f$_{MCK}$: Serial array unit operation clock frequency

  (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

  m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

  4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB

R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB

R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LFDFB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB, R5F100LKDFB, R5F100LLDFB

R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LFDFB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB, R5F101LKDFB, R5F101LLDFB

R5F100LCGFB, R5F100LDGFB, R5F100LEGFB, R5F100LFGFB, R5F100LGGFB, R5F100LHGFB, R5F100LJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35

detail of lead end

ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 {}^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° {}^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

(UNIT:mm)

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.