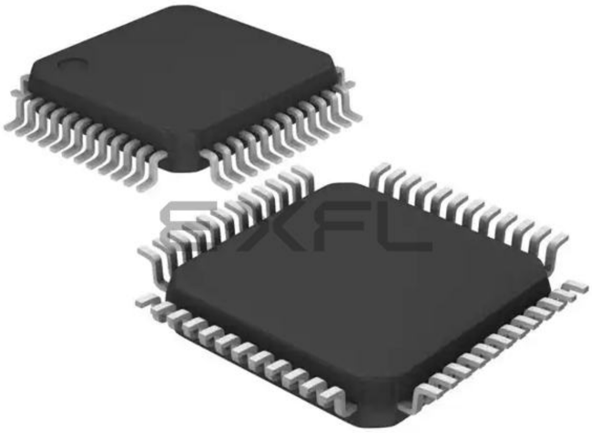
Renesas Electronics America Inc - R5F101GHDFB#30 Datasheet



What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	192KB (192K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LFQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101ghdfb-30

Table 1-1. List of Ordering Part Numbers

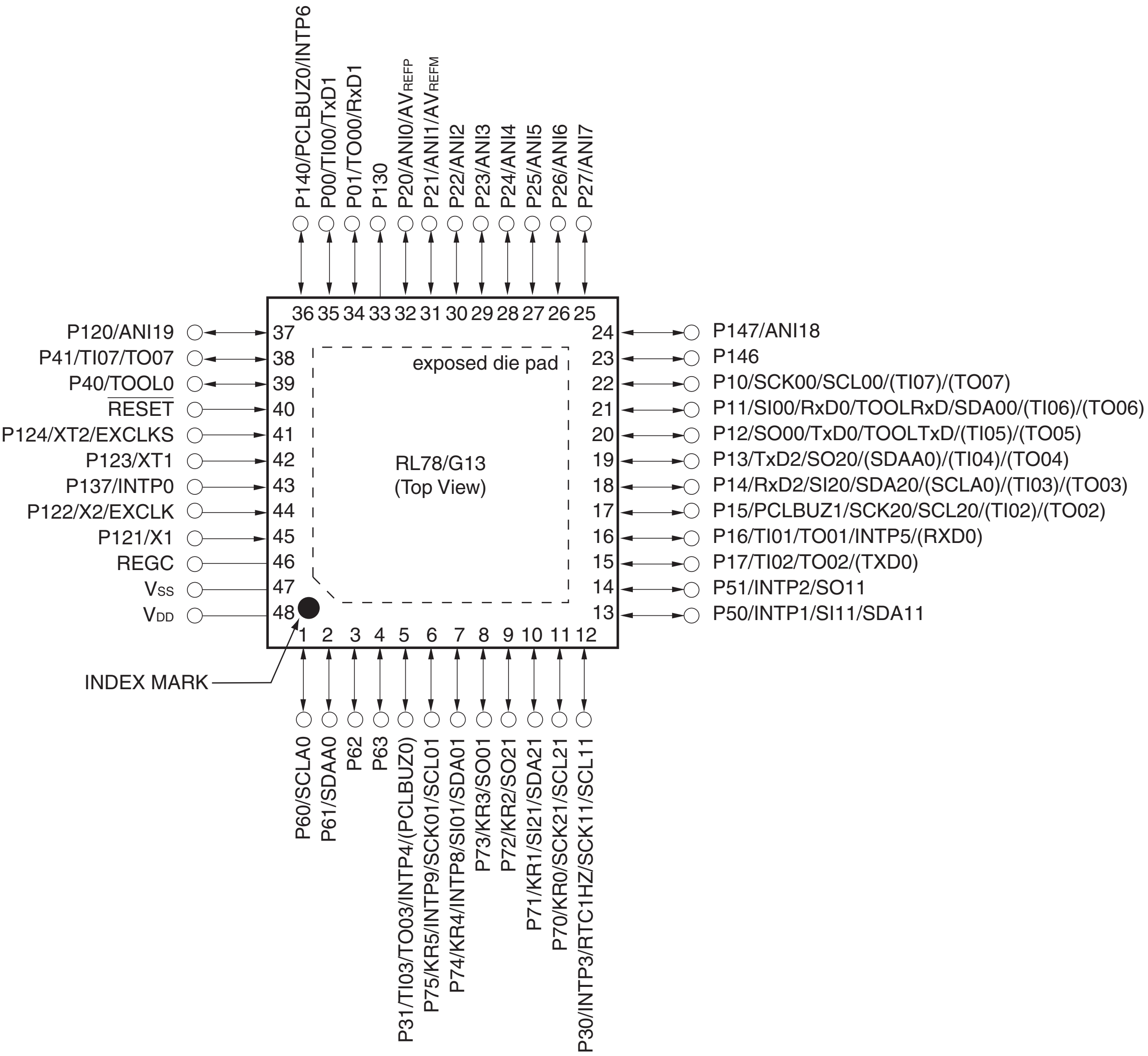
(4/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)	Mounted	A	R5F100FAAFP#V0, R5F100FCAFP#V0, R5F100FDAFP#V0, R5F100FEAFP#V0, R5F100FFAFP#V0, R5F100FGAFP#V0, R5F100FHAFP#V0, R5F100FJAFP#V0, R5F100FKAFP#V0, R5F100FLAFP#V0
				R5F100FAAFP#X0, R5F100FCAFP#X0, R5F100FDAFP#X0, R5F100FEAFP#X0, R5F100FFAFP#X0, R5F100FGAFP#X0, R5F100FHAFP#X0, R5F100FJAFP#X0, R5F100FKAFP#X0, R5F100FLAFP#X0
			D	R5F100FADFP#V0, R5F100FCDFP#V0, R5F100FDDFP#V0, R5F100FEDFP#V0, R5F100FFDFP#V0, R5F100FGDFP#V0, R5F100FHDFP#V0, R5F100FJDFP#V0, R5F100FKDFP#V0, R5F100FLDFP#V0
				R5F100FADFP#X0, R5F100FCDFP#X0, R5F100FDDFP#X0, R5F100FEDFP#X0, R5F100FFDFP#X0, R5F100FGDFP#X0, R5F100FHDFP#X0, R5F100FJDFP#X0, R5F100FKDFP#X0, R5F100FLDFP#X0
			G	R5F100FAGFP#V0, R5F100FCGFP#V0, R5F100FDGFP#V0, R5F100FEGFP#V0, R5F100FFGFP#V0, R5F100FGGFP#V0, R5F100FHGFP#V0, R5F100FJGFP#V0
				R5F100FAGFP#X0, R5F100FCGFP#X0, R5F100FDGFP#X0, R5F100FEGFP#X0, R5F100FFGFP#X0, R5F100FGGFP#X0, R5F100FHGFP#X0, R5F100FJGFP#X0
		Not mounted	A	R5F101FAAFP#V0, R5F101FCAFP#V0, R5F101FDAFP#V0, R5F101FEAFP#V0, R5F101FFAFP#V0, R5F101FGAFP#V0, R5F101FHAFP#V0, R5F101FJAFP#V0, R5F101FKAFP#V0, R5F101FLAFP#V0
				R5F101FAAFP#X0, R5F101FCAFP#X0, R5F101FDAFP#X0, R5F101FEAFP#X0, R5F101FFAFP#X0, R5F101FGAFP#X0, R5F101FHAFP#X0, R5F101FJAFP#X0, R5F101FKAFP#X0, R5F101FLAFP#X0
			D	R5F101FADFP#V0, R5F101FCDFP#V0, R5F101FDDFP#V0, R5F101FEDFP#V0, R5F101FFDFP#V0, R5F101FGDFP#V0, R5F101FHDFP#V0, R5F101FJDFP#V0, R5F101FKDFP#V0, R5F101FLDFP#V0
				R5F101FADFP#X0, R5F101FCDFP#X0, R5F101FDDFP#X0, R5F101FEDFP#X0, R5F101FFDFP#X0, R5F101FGDFP#X0, R5F101FHDFP#X0, R5F101FJDFP#X0, R5F101FKDFP#X0, R5F101FLDFP#X0

Note For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

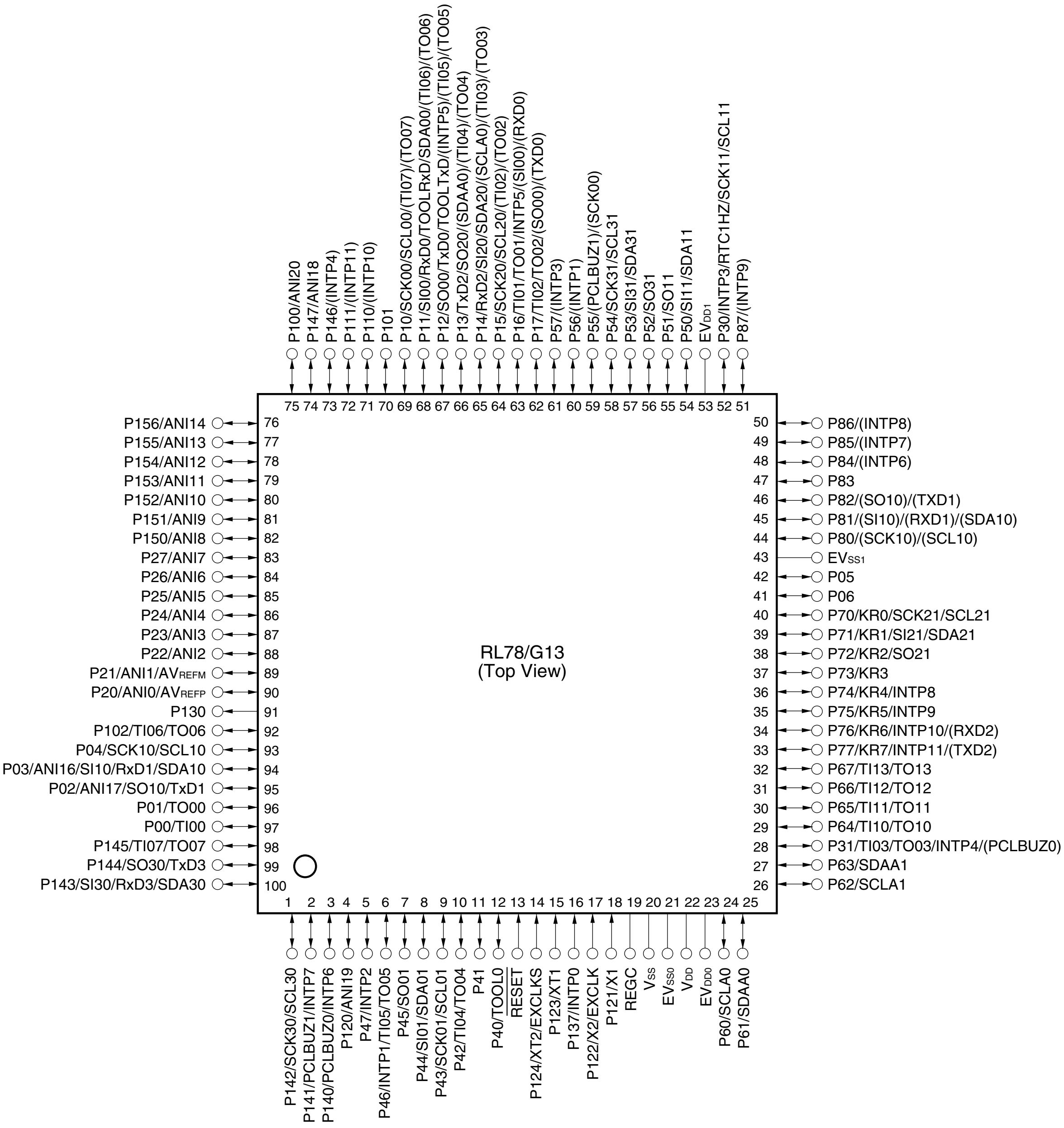
Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

3. It is recommended to connect an exposed die pad to V_{SS}.

1.3.13 100-pin products

- 100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)



Cautions 1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).

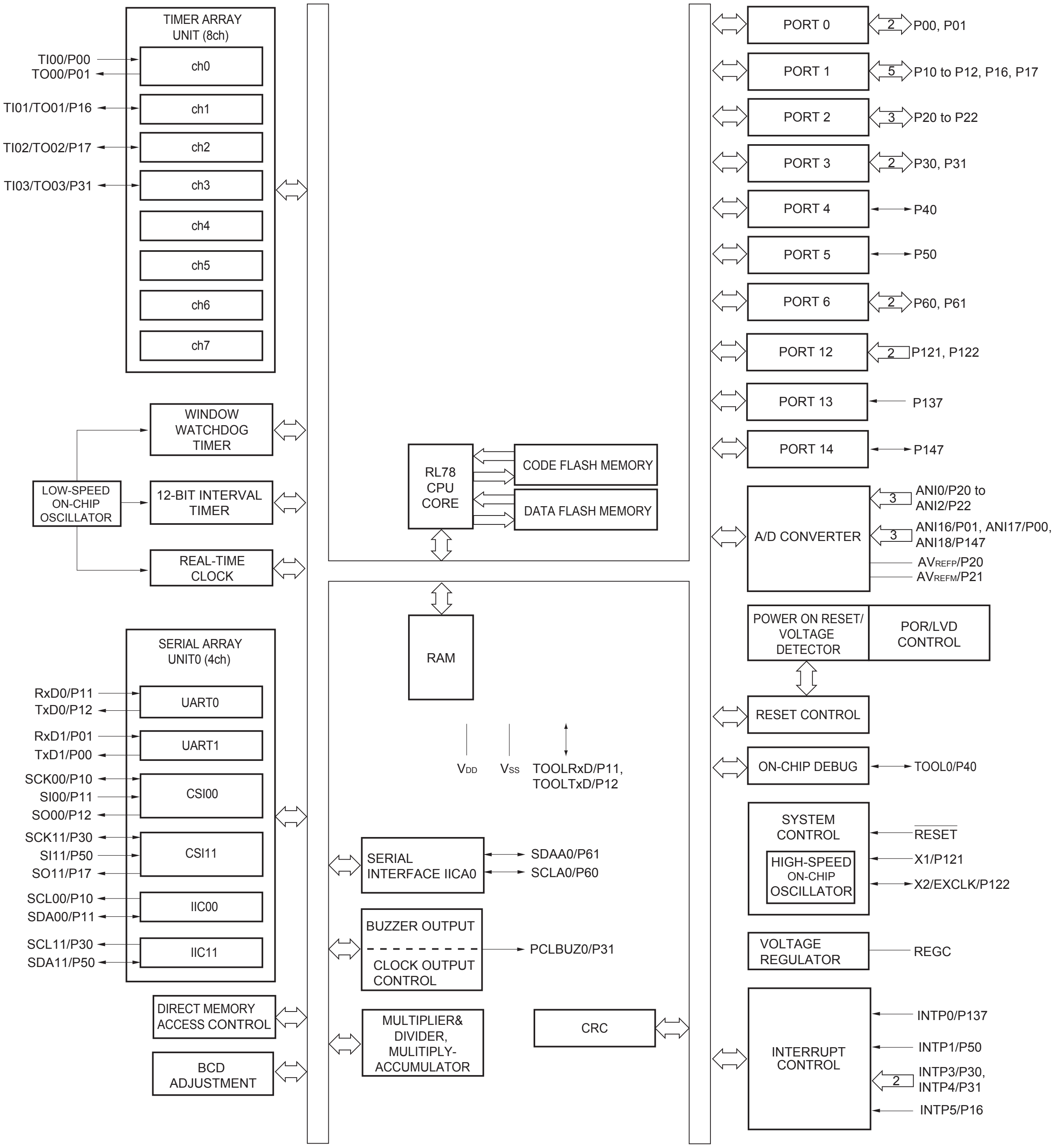
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.2 24-pin products



(T_A = –40 to +85°C, 1.6 V $\leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq$ 5.5 V, $V_{SS} = EV_{SS0} = EV_{SS1}$ = 0 V) (2/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low [Note 1]	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 [Note 2]	mA
		Per pin for P60 to P63				15.0 [Note 2]	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% [Note 3])	4.0 V $\leq EV_{DD0} \leq$ 5.5 V			70.0	mA
			2.7 V $\leq EV_{DD0} <$ 4.0 V			15.0	mA
			1.8 V $\leq EV_{DD0} <$ 2.7 V			9.0	mA
			1.6 V $\leq EV_{DD0} <$ 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% [Note 3])	4.0 V $\leq EV_{DD0} \leq$ 5.5 V			80.0	mA
			2.7 V $\leq EV_{DD0} <$ 4.0 V			35.0	mA
			1.8 V $\leq EV_{DD0} <$ 2.7 V			20.0	mA
			1.6 V $\leq EV_{DD0} <$ 1.8 V			10.0	mA
		Total of all pins (When duty ≤ 70% [Note 3])				150.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P156				0.4 [Note 2]	mA
		Total of all pins (When duty ≤ 70% [Note 3])	1.6 V $\leq V_{DD} \leq$ 5.5 V			5.0	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		mA
						V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 5.0 V		4.6	7.0	mA
						V_{DD} = 3.0 V		4.6	7.0	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.7	5.5	mA
						V_{DD} = 3.0 V		3.7	5.5	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.7	4.0	mA
						V_{DD} = 3.0 V		2.7	4.0	mA
			LS (low-speed main) mode Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	mA
			LV (low-voltage main) mode Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			LS (low-speed main) mode Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Notes 1. Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode:	2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
	2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode:	1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode:	1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (1/2)

(T_A = −40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		1150		1150		ns
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		$t_{KCY1}/2 - 120$		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		$t_{KCY1}/2 - 7$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		$t_{KCY1}/2 - 10$		$t_{KCY1}/2 - 50$		$t_{KCY1}/2 - 50$		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		479		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		10		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60		60	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130		130	ns

(**Notes, Caution,** and **Remarks** are listed on the next page.)

Notes **1.** Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When $AV_{REFP} < V_{DD}$, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

5. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

(2) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (–) = AV_{REFM}/ANI1 (ADREFM = 1), target pin : ANI16 to ANI26

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution EV_{DD0} = AV_{REFP} = V_{DD} [Notes 3, 4]	1.8 V ≤ AV_{REFP} ≤ 5.5 V		1.2	±5.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 5]		1.2	±8.5	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin : ANI16 to ANI26	3.6 V ≤ V_{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V_{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V_{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V_{DD} ≤ 5.5 V	57		95	μs
Zero-scale error[Notes 1, 2]	E_{ZS}	10-bit resolution EV_{DD0} = AV_{REFP} = V_{DD} [Notes 3, 4]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 5]			±0.60	%FSR
Full-scale error[Notes 1, 2]	E_{FS}	10-bit resolution EV_{DD0} = AV_{REFP} = V_{DD} [Notes 3, 4]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±0.35	%FSR
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 5]			±0.60	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution EV_{DD0} = AV_{REFP} = V_{DD} [Notes 3, 4]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±3.5	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 5]			±6.0	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution EV_{DD0} = AV_{REFP} = V_{DD} [Notes 3, 4]	1.8 V ≤ AV_{REFP} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ AV_{REFP} ≤ 5.5 V [Note 5]			±2.5	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI26		0		AV_{REFP} and EV_{DD0}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.
Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

4. When AV_{REFP} < EV_{DD0} ≤ V_{DD}, the MAX. values are as follows.
Overall error: Add ±4.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.
Zero-scale error/Full-scale error: Add ±0.20%FSR to the MAX. value when AV_{REFP} = V_{DD}.
Integral linearity error/ Differential linearity error: Add ±2.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 5.0 V		2.1		mA
						V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 5.0 V		4.6	7.5	mA
						V_{DD} = 3.0 V		4.6	7.5	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 5.0 V		3.7	5.8	mA
						V_{DD} = 3.0 V		3.7	5.8	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 5.0 V		2.7	4.2	mA
						V_{DD} = 3.0 V		2.7	4.2	mA
			HS (high-speed main) mode Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.9	mA
						Resonator connection		3.2	5.0	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 5.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.9	mA
						Resonator connection		1.9	2.9	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.3	6.3	μA
						Resonator connection		4.4	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.6	7.7	μA
						Resonator connection		4.7	7.8	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +105°C	Normal operation	Square wave input		6.9	19.7	μA
						Resonator connection		7.0	19.8	μA

(**Notes** and **Remarks** are listed on the next page.)

3.4 AC Characteristics

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
		Subsystem clock (f_{SUB}) operation		2.4 V ≤ V_{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V_{DD} ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
External system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V_{DD} < 2.7 V			1.0		16.0	MHz
	f_{EXS}				32		35	kHz
External system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 5.5 V			24			ns
		2.4 V ≤ V_{DD} < 2.7 V			30			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t_{TIH}, t_{TIL}				$1/f_{MCK}+10$			ns^{Note}
TO00 to TO07, TO10 to TO17 output frequency	f_{TO}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V				8	MHz
			2.4 V ≤ EV_{DD0} < 2.7 V				4	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	HS (high-speed main) mode	4.0 V ≤ EV_{DD0} ≤ 5.5 V				16	MHz
			2.7 V ≤ EV_{DD0} < 4.0 V				8	MHz
			2.4 V ≤ EV_{DD0} < 2.7 V				4	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0	2.4 V ≤ V_{DD} ≤ 5.5 V		1			μs
		INTP1 to INTP11	2.4 V ≤ EV_{DD0} ≤ 5.5 V		1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR7	2.4 V ≤ EV_{DD0} ≤ 5.5 V		250			ns
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

Note The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}
2.4V ≤ EV_{DD0} < 2.7 V : MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).
m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode) (2/2)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions			HS (high-speed main) Mode		Unit
					MIN.	MAX.	
Transfer rate		Transmission	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V			**Note 1**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 1.4 kΩ, V_b = 2.7 V		2.6 Note 2	Mbps
			2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V			**Note 3**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V		1.2 Note 4	Mbps
			2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V			**Note 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V		0.43 Note 6	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

2. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.

3. The smaller maximum transfer rate derived by using f_{MCK}/12 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.4 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln (1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

4. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 3 above to calculate the maximum transfer rate under conditions of the customer.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (2/3)

(T_A = −40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↑) Note	t_{SIK1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	162		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	354		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	958		ns
SIp hold time (from SCKp↑) Note	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
Delay time from SCKp↓ to SOp output Note	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		200	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		390	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the page after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T_A = –40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SIp setup time (to SCKp↓) Note	t_{SIK1}	4.0 V ≤ EV_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	88		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	88		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	220		ns
SIp hold time (from SCKp↓) Note	t_{KSI1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ	38		ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	38		ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output Note	t_{KSO1}	4.0 V ≤ EV_{DD0} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 30 pF, R_b = 1.4 kΩ		50	ns
		2.7 V ≤ EV_{DD0} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ		50	ns
		2.4 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

3.6.5 Power supply voltage rising slope characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

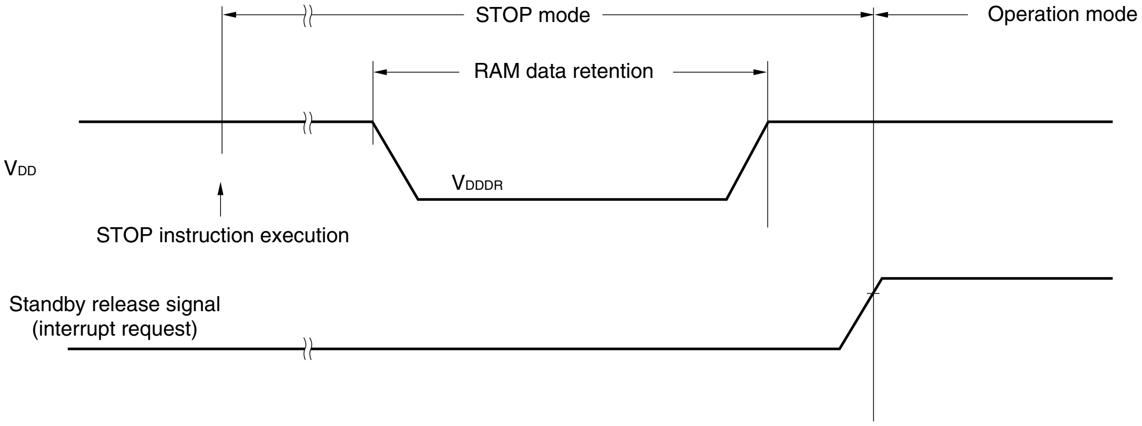
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until V_{DD} reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

(T_A = –40 to +105°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.44^{Note}		5.5	V

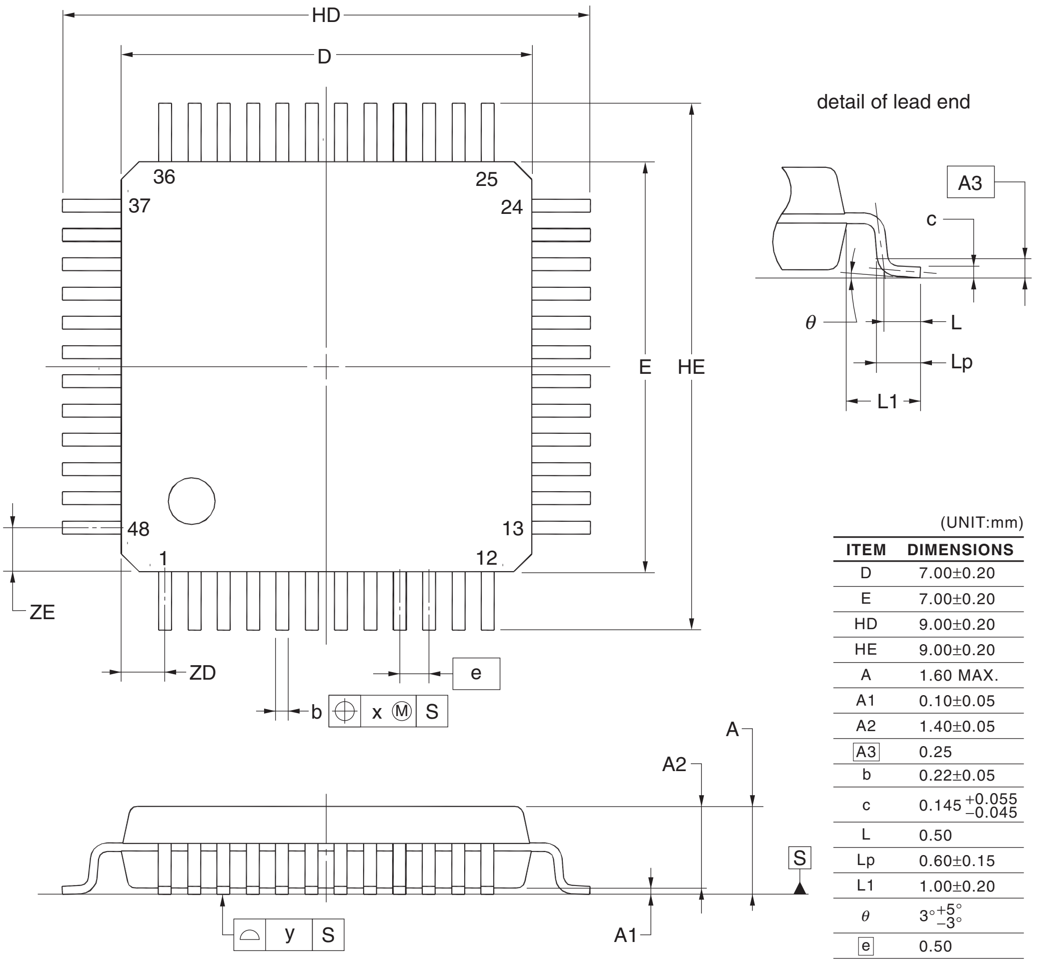
Note This depends on the POR detection voltage. For a falling voltage, data in RAM are retained until the voltage reaches the level that triggers a POR reset but not once it reaches the level at which a POR reset is generated.



4.9 48-pin Products

R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB,
R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB
R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB,
R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB
R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB,
R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB,
R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB
R5F100GAGFB, R5F100GCGFB, R5F100GDGFB, R5F100GEGFB, R5F100GFGFB, R5F100GGGFB,
R5F100GHGFB, R5F100GJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



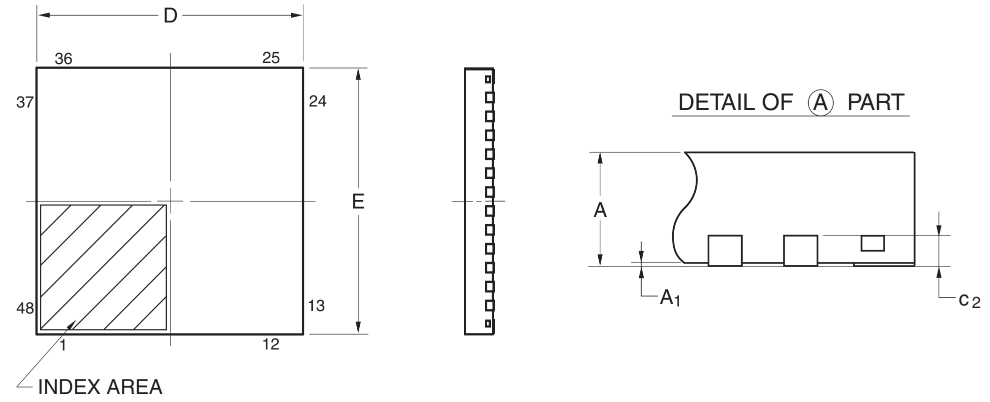
(UNIT:mm)

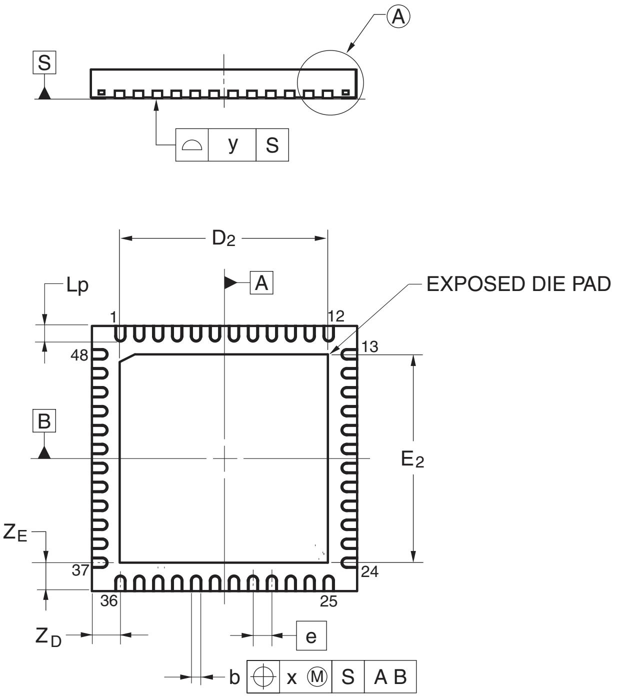
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
$\boxed{A3}$	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3°^{+5°}_{-3°}$
$\boxed{e}$	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA
R5F100GAGNA, R5F100GCGNA, R5F100GDGNA, R5F100GEGNA, R5F100GFGNA, R5F100GGGNA,
R5F100GHGNA, R5F100GJGNA

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-6	0.13

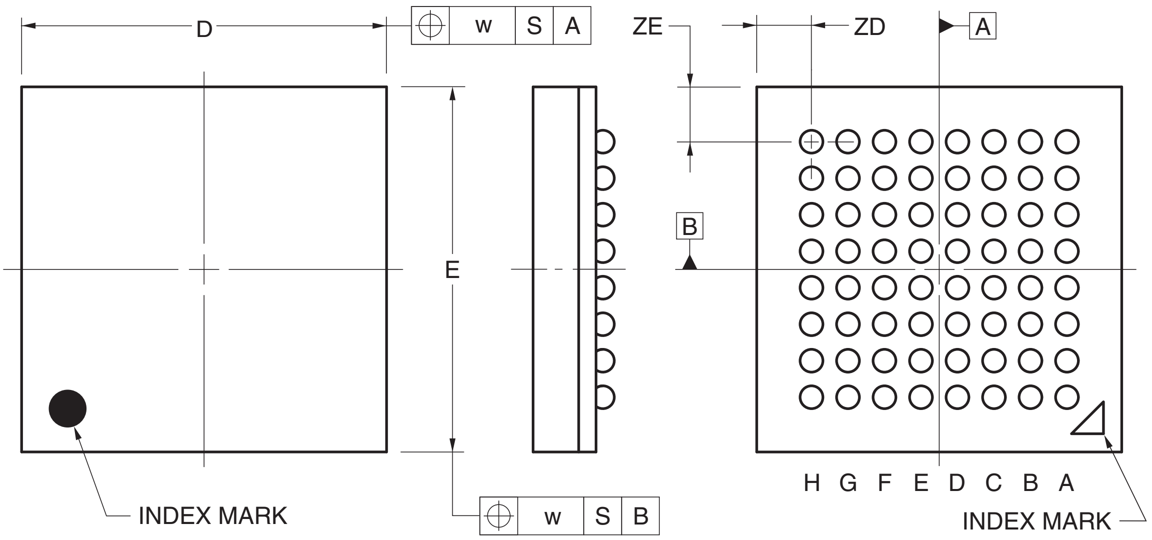


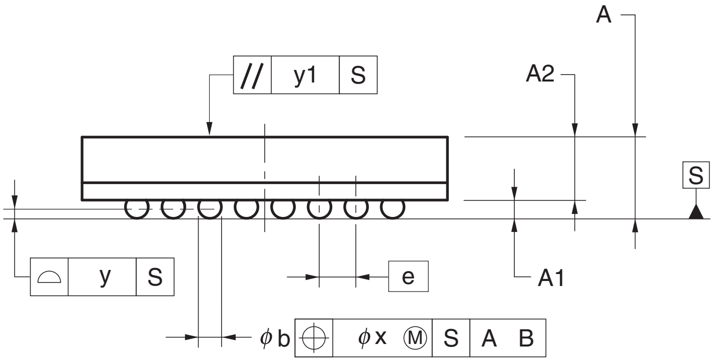


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	—	—	0.80
A_1	0.00	—	—
b	0.18	0.25	0.30
$\boxed{e}$	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05
Z_D	—	0.75	—
Z_E	—	0.75	—
c_2	0.15	0.20	0.25
D_2	—	5.50	—
E_2	—	5.50	—

R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG,
R5F100LJABG
R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG,
R5F101LJABG
R5F100LCGBG, R5F100LDGBG, R5F100LEGBG, R5F100LFGBG, R5F100LGGBG, R5F100LHGBG,
R5F100LJGBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
$\boxed{e}$	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

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