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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I ² C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 10x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-WFQFN Exposed Pad
Supplier Device Package	48-HWQFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101gkana-u0

Table 1-1. List of Ordering Part Numbers

(11/12)

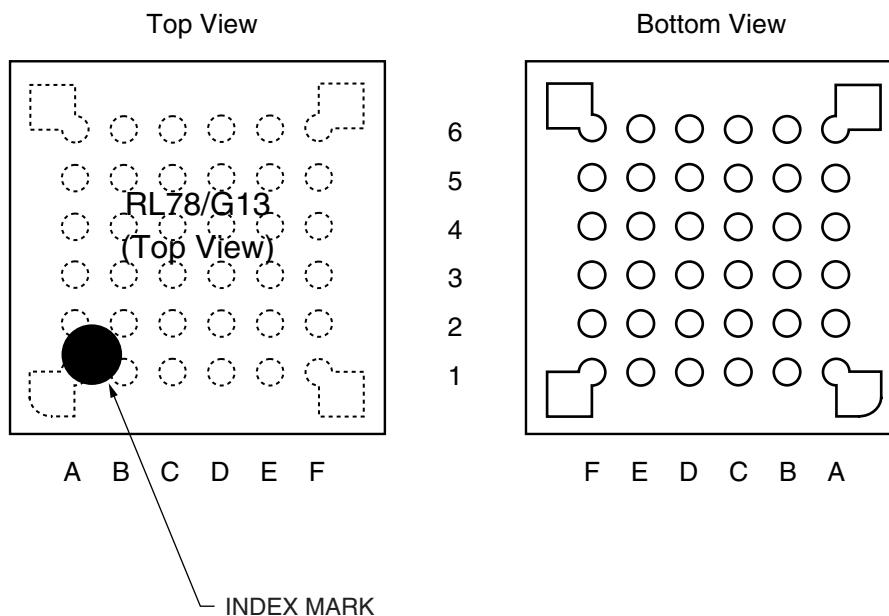
Pin count	Package	Data flash	Fields of Application <small>Note</small>	Ordering Part Number
100 pins	100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)	Mounted	A	R5F100PFAFB#V0, R5F100PGAFB#V0, R5F100PHAFB#V0, R5F100PJAFB#V0, R5F100PKAFB#V0, R5F100PLAFB#V0 R5F100PFAFB#X0, R5F100PGAFB#X0, R5F100PHAFB#X0, R5F100PJAFB#X0, R5F100PKAFB#X0, R5F100PLAFB#X0 R5F100PFDFB#V0, R5F100PGDFB#V0, R5F100PHDFB#V0, R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0 R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0, R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0 R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0, R5F100PJGFB#V0 R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0, R5F100PJGFB#X0
			D	R5F100PJDFB#V0, R5F100PKDFB#V0, R5F100PLDFB#V0 R5F100PFDFB#X0, R5F100PGDFB#X0, R5F100PHDFB#X0, R5F100PJDFB#X0, R5F100PKDFB#X0, R5F100PLDFB#X0 R5F100PFGFB#V0, R5F100PGGFB#V0, R5F100PHGFB#V0, R5F100PJGFB#V0 R5F100PFGFB#X0, R5F100PGGFB#X0, R5F100PHGFB#X0, R5F100PJGFB#X0
			G	R5F101PFAFB#V0, R5F101PGAFB#V0, R5F101PHAFB#V0, R5F101PJAFB#V0, R5F101PKAFB#V0, R5F101PLAFB#V0 R5F101PFAFB#X0, R5F101PGAFB#X0, R5F101PHAFB#X0, R5F101PJAFB#X0, R5F101PKAFB#X0, R5F101PLAFB#X0 R5F101PFDFB#V0, R5F101PGDFB#V0, R5F101PHDFB#V0, R5F101PJDFB#V0, R5F101PKDFB#V0, R5F101PLDFB#V0 R5F101PFDFB#X0, R5F101PGDFB#X0, R5F101PHDFB#X0, R5F101PJDFB#X0, R5F101PKDFB#X0, R5F101PLDFB#X0 R5F101PJDFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PJDFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0
		Not mounted	A	R5F101PFAFA#V0, R5F100PGAFA#V0, R5F100PHAFYA#V0, R5F100PJAFYA#V0, R5F100PKAFYA#V0, R5F100PLAFYA#V0 R5F100PFAFA#X0, R5F100PGAFA#X0, R5F100PHAFYA#X0, R5F100PJAFYA#X0, R5F100PKAFYA#X0, R5F100PLAFYA#X0 R5F100PF DFA#V0, R5F100PGDFA#V0, R5F100PHDFA#V0, R5F100PJ DFA#V0, R5F100PKDFA#V0, R5F100PLDFA#V0 R5F100PF DFA#X0, R5F100PGDFA#X0, R5F100PHDFA#X0, R5F100PJ DFA#X0, R5F100PKDFA#X0, R5F100PLDFA#X0 R5F100PFGFA#V0, R5F100PGGFA#V0, R5F100PHGFA#V0, R5F100PJGFA#V0 R5F100PFGFA#X0, R5F100PGGFA#X0, R5F100PHGFA#X0, R5F100PJGFA#X0
	100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)	Mounted	A	R5F101PFAFA#V0, R5F101PGAFYA#V0, R5F101PHAFYA#V0, R5F101PJAFYA#V0, R5F101PKAFYA#V0, R5F101PLAFYA#V0 R5F101PFAFA#X0, R5F101PGAFYA#X0, R5F101PHAFYA#X0, R5F101PJAFYA#X0, R5F101PKAFYA#X0, R5F101PLAFYA#X0 R5F101PF DFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJ DFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PF DFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJ DFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0 R5F101PFGFA#V0, R5F101PGGFA#V0, R5F101PHGFA#V0, R5F101PJGFA#V0 R5F101PFGFA#X0, R5F101PGGFA#X0, R5F101PHGFA#X0, R5F101PJGFA#X0
			D	R5F101PFAFA#V0, R5F101PGAFYA#V0, R5F101PHAFYA#V0, R5F101PJAFYA#V0, R5F101PKAFYA#V0, R5F101PLAFYA#V0 R5F101PFAFA#X0, R5F101PGAFYA#X0, R5F101PHAFYA#X0, R5F101PJAFYA#X0, R5F101PKAFYA#X0, R5F101PLAFYA#X0 R5F101PF DFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJ DFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PF DFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJ DFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0 R5F101PJDFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PJDFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0
			G	R5F101PFAFA#V0, R5F101PGAFYA#V0, R5F101PHAFYA#V0, R5F101PJAFYA#V0, R5F101PKAFYA#V0, R5F101PLAFYA#V0 R5F101PFAFA#X0, R5F101PGAFYA#X0, R5F101PHAFYA#X0, R5F101PJAFYA#X0, R5F101PKAFYA#X0, R5F101PLAFYA#X0 R5F101PF DFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJ DFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PF DFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJ DFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0 R5F101PFGFA#V0, R5F101PGGFA#V0, R5F101PHGFA#V0, R5F101PJGFA#V0 R5F101PFGFA#X0, R5F101PGGFA#X0, R5F101PHGFA#X0, R5F101PJGFA#X0
		Not mounted	A	R5F101PFAFA#V0, R5F101PGAFYA#V0, R5F101PHAFYA#V0, R5F101PJAFYA#V0, R5F101PKAFYA#V0, R5F101PLAFYA#V0 R5F101PFAFA#X0, R5F101PGAFYA#X0, R5F101PHAFYA#X0, R5F101PJAFYA#X0, R5F101PKAFYA#X0, R5F101PLAFYA#X0 R5F101PF DFA#V0, R5F101PGDFA#V0, R5F101PHDFA#V0, R5F101PJ DFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PF DFA#X0, R5F101PGDFA#X0, R5F101PHDFA#X0, R5F101PJ DFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0 R5F101PJDFA#V0, R5F101PKDFA#V0, R5F101PLDFA#V0 R5F101PJDFA#X0, R5F101PKDFA#X0, R5F101PLDFA#X0

Note For the fields of application, refer to Figure 1-1 Part Number, Memory Size, and Package of RL78/G13.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.6 36-pin products

- 36-pin plastic WFLGA (4×4 mm, 0.5 mm pitch)



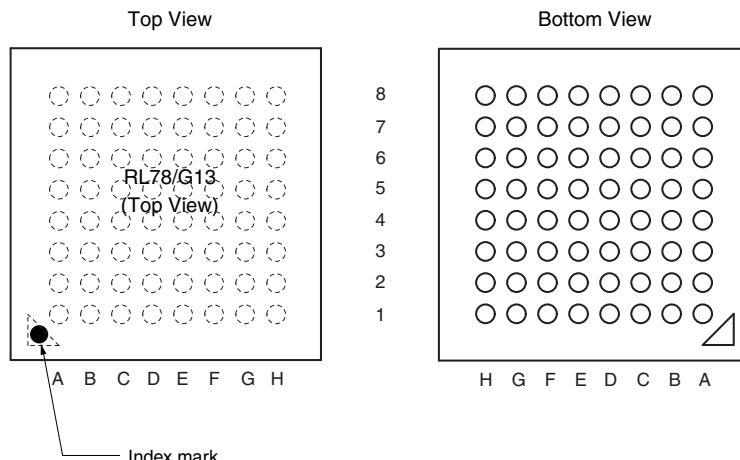
	A	B	C	D	E	F	
6	P60/SCLA0	V _{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V _{ss}	REGC	RESET	P120/ANI19	5
4	P72/SO21	P71/SI21/SDA21	P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)	P31/TI03/TO03/INTP4/PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/SI11/SDA11	P70/SCK21/SCL21	P15/PCLBUZ1/SCK20/SCL20/(TI02)/(TO02)	P22/ANI2	P20/ANI0/AV _{REFP}	P21/ANI1/AV _{REFM}	3
2	P30/INTP3/SCK11/SCL11	P16/TI01/TO01/INTP5/(RxD0)	P12/SO00/TxD0/TOOLTxD/(TI05)/(TO05)	P11/SI00/RxD0/TOOLRxDSDA0/(TI06)/(TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/SO11	P17/TI02/TO02/(TxD0)	P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)	P10/SCK00/SCL00/(TI07)/(TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

- 64-pin plastic VFBGA (4 × 4 mm, 0.4 mm pitch)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05	C1	P51/INTP2/SO11	E1	P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)	G1	P146
A2	P30/INTP3/RTC1HZ/SCK11/SCL11	C2	P71/KR1/SI21/SDA21	E2	P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)	G2	P25/ANI5
A3	P70/KR0/SCK21/SCL21	C3	P74/KR4/INTP8/SI01/SDA01	E3	P15/SCK20/SCL20/(TI02)/(TO02)	G3	P24/ANI4
A4	P75/KR5/INTP9/SCK01/SCL01	C4	P52/(INTP10)	E4	P16/TI01/TO01/INTP5/(SI00)/(RxD0)	G4	P22/ANI2
A5	P77/KR7/INTP11/(TxD2)	C5	P53/(INTP11)	E5	P03/ANI16/SI10/RxD1/SDA10	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/TI07/TO07	G6	P02/ANI17/SO10/TxD1
A7	P60/SCLA0	C7	V _{ss}	E7	RESET	G7	P00/TI00
A8	EV _{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/INTP1/SI11/SDA11	D1	P55/(PCLBUZ1)/(SCK00)	F1	P10/SCK00/SCL00/(TI07)/(TO07)	H1	P147/ANI18
B2	P72/KR2/SO21	D2	P06/TI06/TO06	F2	P11/SI00/RxD0/TOOLRxDSDA00/(TI06)/(TO06)	H2	P27/ANI7
B3	P73/KR3/SO01	D3	P17/TI02/TO02/(SO00)/(TxD0)	F3	P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)	H3	P26/ANI6
B4	P76/KR6/INTP10/(RxD2)	D4	P54	F4	P21/ANI1/AV _{REFM}	H4	P23/ANI3
B5	P31/TI03/TO03/INTP4/(PCLBUZ0)	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10	H5	P20/ANI0/AV _{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V _{DD}	D7	REGC	F7	P01/TO00	H7	P140/PCLBUZ0/INTP6
B8	EV _{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

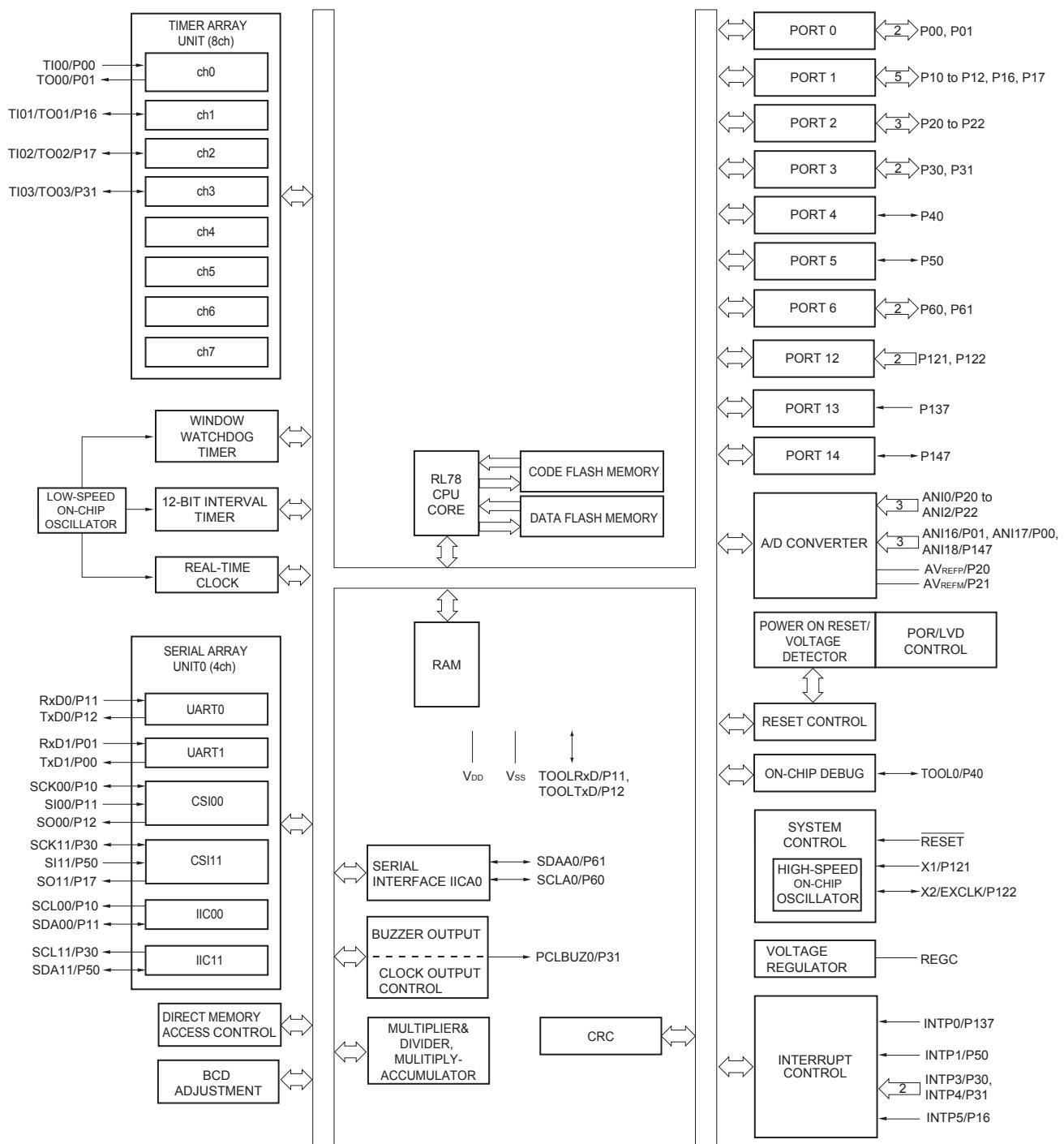
Cautions 1. Make EV_{SS0} pin the same potential as V_{ss} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
3. Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μ F).

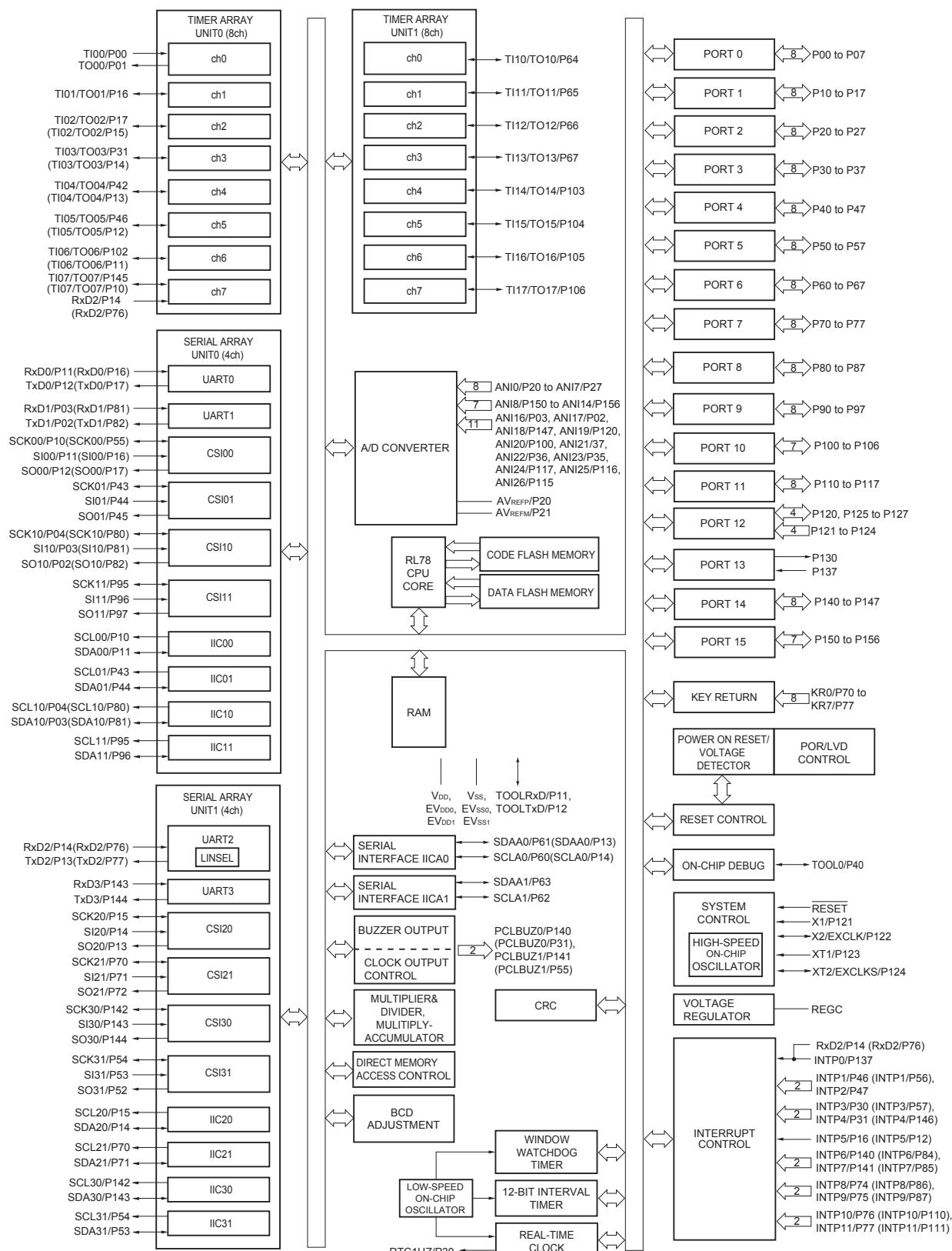
Remarks 1. For pin identification, see 1.4 Pin Identification.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{ss} and EV_{SS0} pins to separate ground lines.
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.5.2 24-pin products



1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(5) During communication at same potential (simplified I²C mode) (1/2) $(T_A = -40$ to $+85^\circ\text{C}$, $1.6 \text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0 \text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCL _r clock frequency	f _{SCL}	2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		250 Note 1		250 Note 1		kHz
Hold time when SCL _r = "L"	t _{LOW}	2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		1850		1850		ns
		1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1850		1850		ns
Hold time when SCL _r = "H"	t _{HIGH}	2.7 V \leq EV _{DD0} \leq 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		1150		1150		ns
		1.8 V \leq EV _{DD0} \leq 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		1150		1150		ns
		1.8 V \leq EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		1550		1550		ns
		1.7 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		1850		1850		ns
		1.6 V \leq EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only) (2/2)

($T_A = -40$ to $+85^\circ\text{C}$, $2.7 \text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0 \text{ V}$)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp \downarrow) ^{Note 2}	tsIK1	4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 20 pF, R _b = 1.4 k Ω	23		110		110		ns
		2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 20 pF, R _b = 2.7 k Ω	33		110		110		ns
Slp hold time (from SCKp \downarrow) ^{Note 2}	tKSI1	4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 20 pF, R _b = 1.4 k Ω	10		10		10		ns
		2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 20 pF, R _b = 2.7 k Ω	10		10		10		ns
Delay time from SCKp \uparrow to SO _p output ^{Note 2}	tKS01	4.0 V \leq EV _{DD0} \leq 5.5 V, 2.7 V \leq V _b \leq 4.0 V, C _b = 20 pF, R _b = 1.4 k Ω		10		10		10	ns
		2.7 V \leq EV _{DD0} < 4.0 V, 2.3 V \leq V _b \leq 2.7 V, C _b = 20 pF, R _b = 2.7 k Ω		10		10		10	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SO_p pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remarks 1. R_b[Ω]:Communication line (SCKp, SO_p) pull-up resistance, C_b[F]: Communication line (SCKp, SO_p) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM number (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

**(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)
(1/3)**

($T_A = -40$ to $+85^\circ\text{C}$, $1.8 \text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0 \text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t _{KCY1}	t _{KCY1} ≥ 4/f _{CLK}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note} , C _b = 30 pF, R _b = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	t _{Kh1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 75		t _{KCY1} /2 – 75		t _{KCY1} /2 – 75			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 170		t _{KCY1} /2 – 170		t _{KCY1} /2 – 170			ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 458		t _{KCY1} /2 – 458		t _{KCY1} /2 – 458			ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ	t _{KCY1} /2 – 12		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ	t _{KCY1} /2 – 18		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50			ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note} , C _b = 30 pF, R _b = 5.5 kΩ	t _{KCY1} /2 – 50		t _{KCY1} /2 – 50		t _{KCY1} /2 – 50			ns

Note Use it with $EV_{DD0} \geq V_b$.

Caution Select the TTL input buffer for the S_{Op} pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the S_{Op} pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage		
	Reference voltage (+) = AV_{REFP}	Reference voltage (+) = V_{DD}	Reference voltage (+) = V_{BGR}
Reference voltage (-) = AV_{REFM}	Reference voltage (-) = V_{SS}	Reference voltage (-) = AV_{REFM}	Reference voltage (-) = AV_{REFM}
ANI0 to ANI14	Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI26	Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage	Refer to 2.6.1 (1).		—

(1) When reference voltage (+) = AV_{REFP} /ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM} /ANI1 (ADREFM = 1), target pin : ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

($T_A = -40$ to $+85^\circ\text{C}$, $1.6 \text{ V} \leq \text{AV}_{\text{REFP}} \leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$, $\text{V}_{\text{SS}} = 0 \text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $\text{AV}_{\text{REFM}} = 0 \text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}}$ ^{Note 3}	1.8 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$		1.2	± 3.5	LSB
			1.6 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ ^{Note 4}		1.2	± 7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	2.125		39	μs
			2.7 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	3.1875		39	μs
			1.8 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	17		39	μs
			1.6 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	57		95	μs
	t _{CONV}	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	2.375		39	μs
			2.7 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	3.5625		39	μs
			2.4 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E _{zs}	10-bit resolution $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}}$ ^{Note 3}	1.8 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			± 0.25	%FSR
			1.6 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ ^{Note 4}			± 0.50	%FSR
Full-scale error ^{Notes 1, 2}	E _{fs}	10-bit resolution $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}}$ ^{Note 3}	1.8 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			± 0.25	%FSR
			1.6 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ ^{Note 4}			± 0.50	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}}$ ^{Note 3}	1.8 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			± 2.5	LSB
			1.6 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ ^{Note 4}			± 5.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}}$ ^{Note 3}	1.8 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$			± 1.5	LSB
			1.6 V $\leq \text{AV}_{\text{REFP}} \leq 5.5 \text{ V}$ ^{Note 4}			± 2.0	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI14		0		AV_{REFP}	V
		Internal reference voltage (2.4 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$, HS (high-speed main) mode)			V_{BGR} ^{Note 5}		V
		Temperature sensor output voltage (2.4 V $\leq \text{V}_{\text{DD}} \leq 5.5 \text{ V}$, HS (high-speed main) mode)			V_{TMPS25} ^{Note 5}		V

(Notes are listed on the next page.)

- (4) When reference voltage (+) = Internal reference voltage ($\text{ADREFP1} = 1$, $\text{ADREFP0} = 0$), reference voltage (-) = $\text{AV}_{\text{REFM}}/\text{ANI1}$ ($\text{ADREFM} = 1$), target pin : ANI0, ANI2 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $2.4 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$, $1.6 \text{ V} \leq EV_{\text{DD0}} = EV_{\text{DD1}} \leq V_{\text{DD}}$, $V_{\text{SS}} = EV_{\text{SS0}} = EV_{\text{SS1}} = 0 \text{ V}$, Reference voltage (+) = $\text{VBGR}^{\text{Note 3}}$, Reference voltage (-) = $\text{AV}_{\text{REFM}} = 0 \text{ V}^{\text{Note 4}}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		bit	
Conversion time	tconv	8-bit resolution	$2.4 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	$2.4 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4 \text{ V} \leq V_{\text{DD}} \leq 5.5 \text{ V}$			± 1.0	LSB
Analog input voltage	V _{Ain}			0		$\text{VBGR}^{\text{Note 3}}$	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

3. Refer to 2.6.2 Temperature sensor/internal reference voltage characteristics.

4. When reference voltage (-) = V_{SS} , the MAX. values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the MAX. value when reference voltage (-) = AV_{REFM} .

Integral linearity error: Add ± 0.5 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Differential linearity error: Add ± 0.2 LSB to the MAX. value when reference voltage (-) = AV_{REFM} .

Remark The electrical characteristics of the products G: Industrial applications ($T_A = -40$ to $+105^\circ\text{C}$) are different from those of the products "A: Consumer applications, and D: Industrial applications". For details, refer to **3.1 to 3.10**.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		-0.5 to +6.5	V
	EV_{DD0}, EV_{DD1}	$EV_{DD0} = EV_{DD1}$	-0.5 to +6.5	V
	EV_{SS0}, EV_{SS1}	$EV_{SS0} = EV_{SS1}$	-0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	-0.3 to +2.8 and -0.3 to $V_{DD} + 0.3^{\text{Note 1}}$	V
Input voltage	V_{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3^{\text{Note 2}}$	V
	V_{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V_{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, RESET	-0.3 to $V_{DD} + 0.3^{\text{Note 2}}$	V
Output voltage	V_{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $V_{DD} + 0.3^{\text{Note 2}}$	V
	V_{O2}	P20 to P27, P150 to P156	-0.3 to $V_{DD} + 0.3^{\text{Note 2}}$	V
Analog input voltage	V_{AI1}	ANI16 to ANI26	-0.3 to $EV_{DD0} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3^{\text{Notes 2, 3}}$	V
	V_{AI2}	ANIO to ANI14	-0.3 to $V_{DD} + 0.3$ and -0.3 to $AV_{REF}(+) + 0.3^{\text{Notes 2, 3}}$	V

- Notes 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.
2. Must be 6.5 V or lower.
 3. Do not exceed $AV_{REF}(+) + 0.3$ V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

- Remarks**
1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
 2. $AV_{REF}(+)$: + side reference voltage of the A/D converter.
 3. V_{ss} : Reference voltage

(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			8.5 ^{Note 2}	mA
		Per pin for P60 to P63			15.0 ^{Note 2}	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		40.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		15.0	mA
			2.4 V ≤ EV _{DD0} < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EV _{DD0} ≤ 5.5 V		40.0	mA
			2.7 V ≤ EV _{DD0} < 4.0 V		35.0	mA
			2.4 V ≤ EV _{DD0} < 2.7 V		20.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})			80.0	mA
		I _{OL2}	Per pin for P20 to P27, P150 to P156		0.4 ^{Note 2}	mA
			Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ V _{DD} ≤ 5.5 V	5.0	mA

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.
 - Do not exceed the total current value.
 - Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \geq 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

 $(T_A = -40$ to $+105^\circ\text{C}$, $2.4 \text{ V} \leq EV_{DD0} \leq V_{DD} \leq 5.5 \text{ V}$, $V_{SS} = EV_{SS0} = 0 \text{ V}$) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current <small>Note 1</small>	I_{DD2} <small>Note 2</small>	HALT mode	HS (high-speed main) mode <small>Note 7</small>	$f_{IH} = 32 \text{ MHz}$ <small>Note 4</small>	$V_{DD} = 5.0 \text{ V}$		0.54	2.90	mA	
					$V_{DD} = 3.0 \text{ V}$		0.54	2.90	mA	
				$f_{IH} = 24 \text{ MHz}$ <small>Note 4</small>	$V_{DD} = 5.0 \text{ V}$		0.44	2.30	mA	
					$V_{DD} = 3.0 \text{ V}$		0.44	2.30	mA	
				$f_{IH} = 16 \text{ MHz}$ <small>Note 4</small>	$V_{DD} = 5.0 \text{ V}$		0.40	1.70	mA	
					$V_{DD} = 3.0 \text{ V}$		0.40	1.70	mA	
		HS (high-speed main) mode <small>Note 7</small>	$f_{MX} = 20 \text{ MHz}$ <small>Note 3</small> , $V_{DD} = 5.0 \text{ V}$	Square wave input		0.28	1.90	mA		
				Resonator connection		0.45	2.00	mA		
			$f_{MX} = 20 \text{ MHz}$ <small>Note 3</small> , $V_{DD} = 3.0 \text{ V}$	Square wave input		0.28	1.90	mA		
				Resonator connection		0.45	2.00	mA		
			$f_{MX} = 10 \text{ MHz}$ <small>Note 3</small> , $V_{DD} = 5.0 \text{ V}$	Square wave input		0.19	1.02	mA		
				Resonator connection		0.26	1.10	mA		
			$f_{MX} = 10 \text{ MHz}$ <small>Note 3</small> , $V_{DD} = 3.0 \text{ V}$	Square wave input		0.19	1.02	mA		
				Resonator connection		0.26	1.10	mA		
		Subsystem clock operation	$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = -40^\circ\text{C}$	Square wave input		0.25	0.57	μA		
				Resonator connection		0.44	0.76	μA		
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = +25^\circ\text{C}$	Square wave input		0.30	0.57	μA		
				Resonator connection		0.49	0.76	μA		
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = +50^\circ\text{C}$	Square wave input		0.37	1.17	μA		
				Resonator connection		0.56	1.36	μA		
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = +70^\circ\text{C}$	Square wave input		0.53	1.97	μA		
				Resonator connection		0.72	2.16	μA		
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = +85^\circ\text{C}$	Square wave input		0.82	3.37	μA		
				Resonator connection		1.01	3.56	μA		
			$f_{SUB} = 32.768 \text{ kHz}$ <small>Note 5</small> , $T_A = +105^\circ\text{C}$	Square wave input		3.01	15.37	μA		
				Resonator connection		3.20	15.56	μA		
I_{DD3} <small>Note 6</small>	STOP mode <small>Note 8</small>	$T_A = -40^\circ\text{C}$					0.18	0.50	μA	
		$T_A = +25^\circ\text{C}$					0.23	0.50	μA	
		$T_A = +50^\circ\text{C}$					0.30	1.10	μA	
		$T_A = +70^\circ\text{C}$					0.46	1.90	μA	
		$T_A = +85^\circ\text{C}$					0.75	3.30	μA	
		$T_A = +105^\circ\text{C}$					2.94	15.30	μA	

(Notes and Remarks are listed on the next page.)

(3) Peripheral Functions (Common to all products)(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

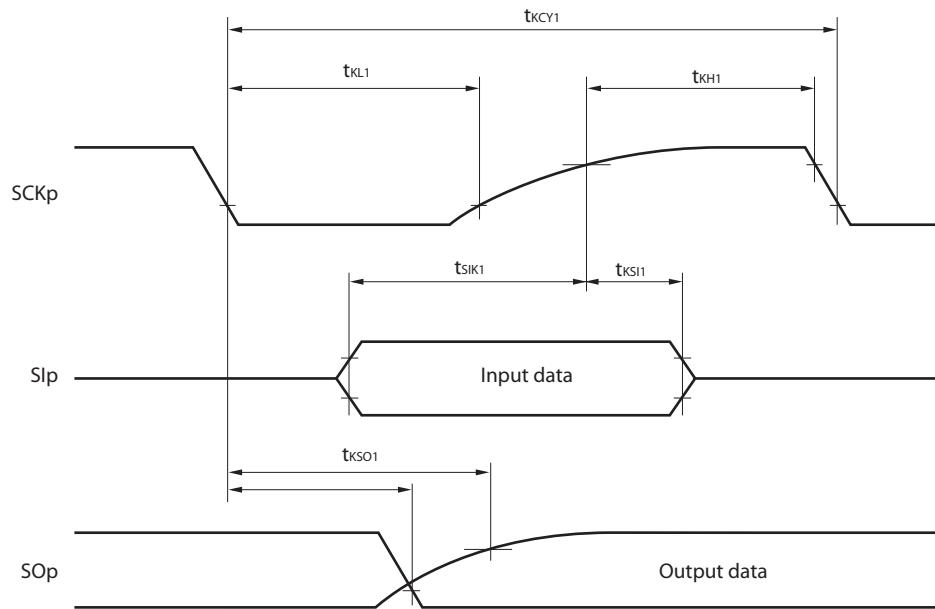
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	I _{FIL} Note 1				0.20		µA
RTC operating current	I _{RTC} Notes 1, 2, 3				0.02		µA
12-bit interval timer operating current	I _{IT} Notes 1, 2, 4				0.02		µA
Watchdog timer operating current	I _{WDT} Notes 1, 2, 5	f _{IL} = 15 kHz			0.22		µA
A/D converter operating current	I _{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	I _{ADREF} Note 1				75.0		µA
Temperature sensor operating current	I _{TMPS} Note 1				75.0		µA
LVD operating current	I _{LVD} Notes 1, 7				0.08		µA
Self programming operating current	I _{FSP} Notes 1, 9				2.50	12.20	mA
BGO operating current	I _{BGO} Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	I _{SNOZ} Note 1	ADC operation	The mode is performed ^{Note 10}		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		1.20	2.04	mA
		CSI/UART operation			0.70	1.54	mA

Notes 1. Current flowing to the V_{DD}.

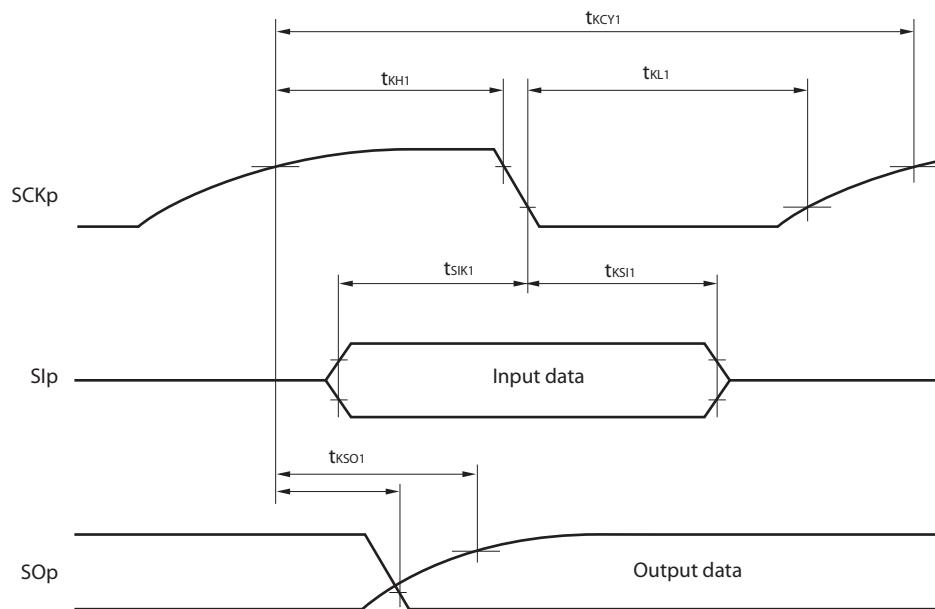
2. When high speed on-chip oscillator and high-speed system clock are stopped.
3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added. I_{DD2} subsystem clock operation includes the operational current of the real-time clock.
4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.
5. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

CSI mode serial transfer timing (master mode) (during communication at different potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

**CSI mode serial transfer timing (master mode) (during communication at different potential)**

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_b ≤ 5.5 V, V_{ss} = EV_{SS0} = EV_{SS1} = 0 V)

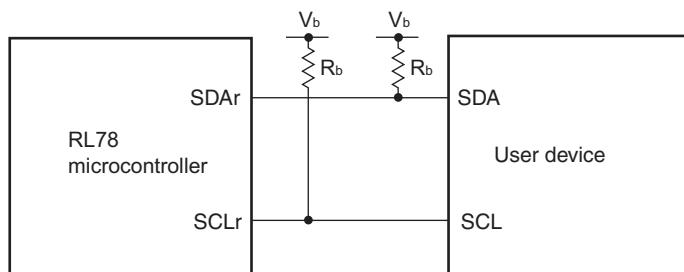
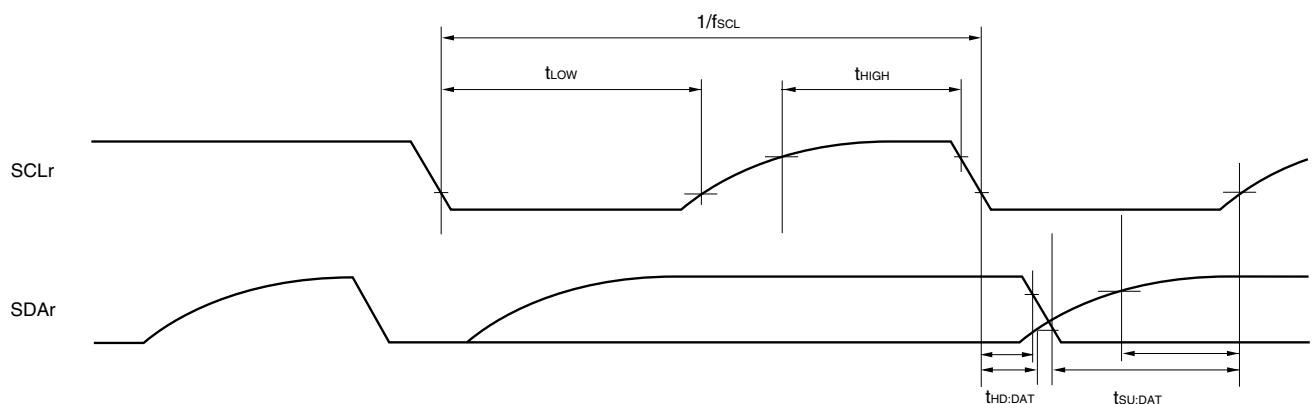
Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	28/f _{MCK}	ns
			20 MHz < f _{MCK} ≤ 24 MHz	24/f _{MCK}	ns
			8 MHz < f _{MCK} ≤ 20 MHz	20/f _{MCK}	ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}	ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	40/f _{MCK}	ns
			20 MHz < f _{MCK} ≤ 24 MHz	32/f _{MCK}	ns
			16 MHz < f _{MCK} ≤ 20 MHz	28/f _{MCK}	ns
			8 MHz < f _{MCK} ≤ 16 MHz	24/f _{MCK}	ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}	ns
			f _{MCK} ≤ 4 MHz	12/f _{MCK}	ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	24 MHz < f _{MCK}	96/f _{MCK}	ns
			20 MHz < f _{MCK} ≤ 24 MHz	72/f _{MCK}	ns
			16 MHz < f _{MCK} ≤ 20 MHz	64/f _{MCK}	ns
			8 MHz < f _{MCK} ≤ 16 MHz	52/f _{MCK}	ns
			4 MHz < f _{MCK} ≤ 8 MHz	32/f _{MCK}	ns
			f _{MCK} ≤ 4 MHz	20/f _{MCK}	ns
SCKp high-/low-level width	t _{Kh2} , t _{kl2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 - 24		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 - 36		ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 - 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	1/f _{MCK} + 40		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	1/f _{MCK} + 40		ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V	1/f _{MCK} + 60		ns
Slp hold time (from SCKp↑) ^{Note 3}	t _{KSI2}		1/f _{MCK} + 62		ns
Delay time from SCKp↓ to SOp output ^{Note 4}	t _{KSO2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ		2/f _{MCK} + 240	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ		2/f _{MCK} + 428	ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V C _b = 30 pF, R _b = 5.5 kΩ		2/f _{MCK} + 1146	ns

(Notes, Caution and Remarks are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCL _r clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		400 ^{Note 1}	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		400 ^{Note 1}	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		100 ^{Note 1}	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		100 ^{Note 1}	kHz
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ		100 ^{Note 1}	kHz
Hold time when SCL _r = "L"	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1200		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	4600		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	4600		ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	4650		ns
Hold time when SCL _r = "H"	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	620		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	500		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	2700		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	2400		ns
		2.4 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1830		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

Simplified I²C mode connection diagram (during communication at different potential)**Simplified I²C mode serial transfer timing (during communication at different potential)**

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 20- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

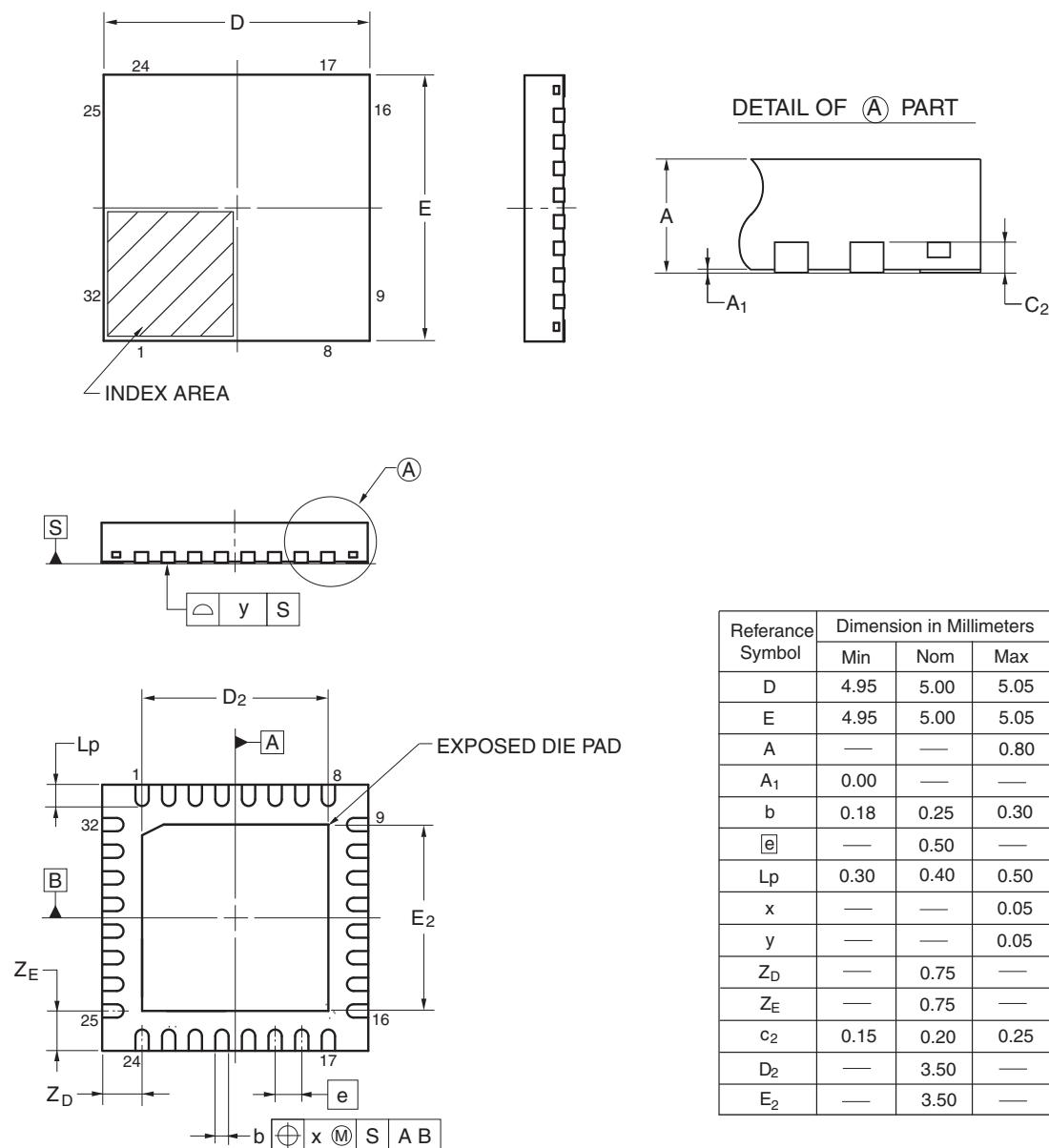
Remarks

1. $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
2. r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

4.5 32-pin Products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
 R5F100BAGNA, R5F100BCGNA, R5F100BDGNA, R5F100BEGNA, R5F100BFGNA, R5F100BGGNA

JEITA Package code	RENESAS code	Previous code	MASS (TYP.)[g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-5	0.06

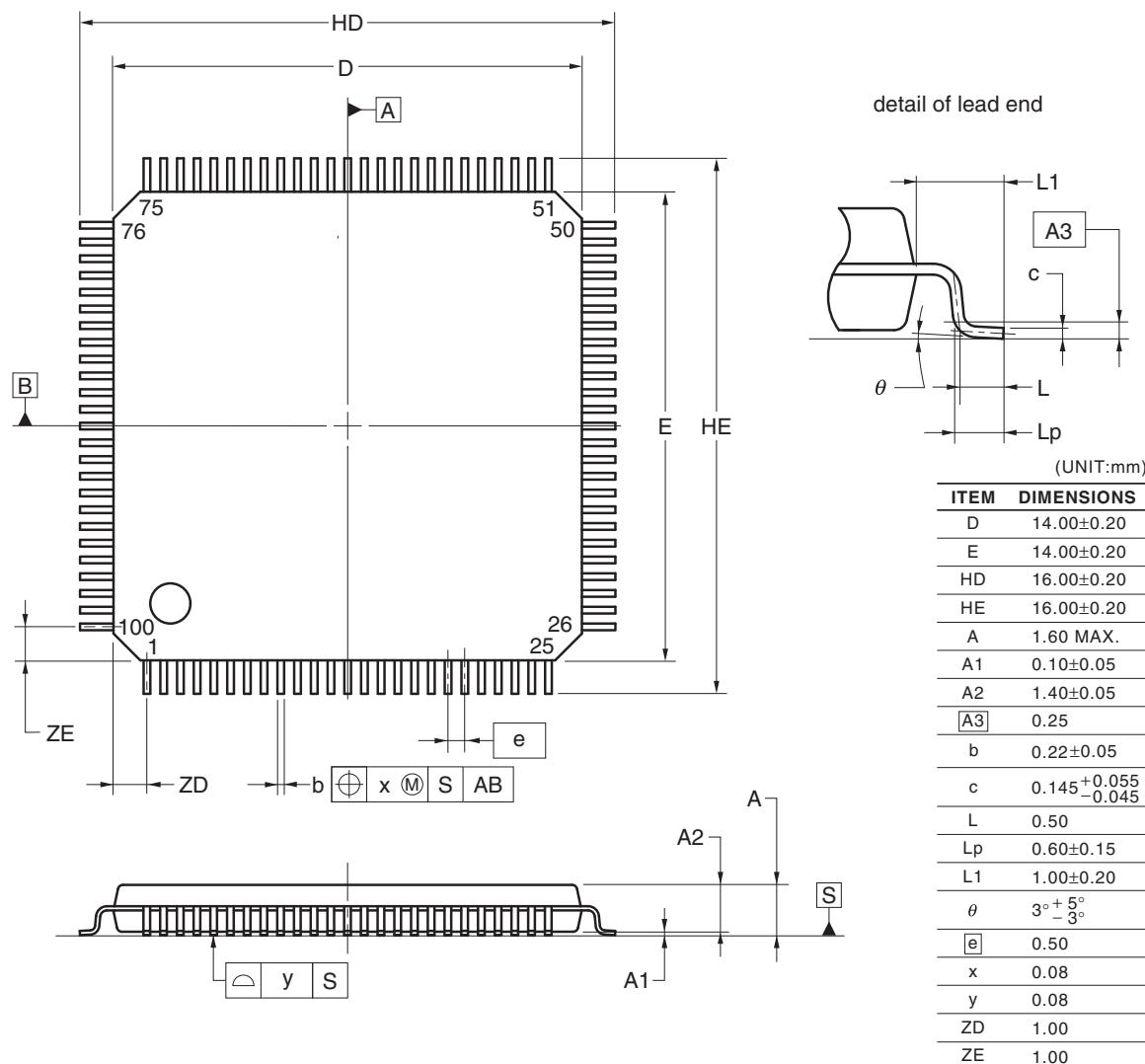


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4.13 100-pin Products

R5F100PFAFB, R5F100PGAFB, R5F100PHAFB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFB, R5F101PHAFB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
 R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
 R5F100PFGFB, R5F100PGGFB, R5F100PHGFB, R5F100PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



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