What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Obsolete
Core Processor	RL78
Core Size	16-Bit
Speed	32MHz
Connectivity	CSI, I²C, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 12x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	52-LQFP
Supplier Device Package	52-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f101jdafa-v0

Table 1-1. List of Ordering Part Numbers

(8/12)

Pin count	Package	Data flash	Fields of Application [Note]	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	Mounted	A	R5F100LCAFA#V0, R5F100LDAFA#V0, R5F100LEAFA#V0, R5F100LFAFA#V0, R5F100LGAFA#V0, R5F100LHAFA#V0, R5F100LJAFA#V0, R5F100LKAFA#V0, R5F100LLAFA#V0
				R5F100LCAFA#X0, R5F100LDAFA#X0, R5F100LEAFA#X0, R5F100LFAFA#X0,
			D	R5F100LGAFA#X0, R5F100LHAFA#X0, R5F100LJAFA#X0, R5F100LKAFA#X0, R5F100LLAFA#X0
				R5F100LCDFA#V0, R5F100LDDFA#V0, R5F100LEDFA#V0, R5F100LFDFA#V0, R5F100LGDFA#V0, R5F100LHDFA#V0, R5F100LJDFA#V0, R5F100LKDFA#V0, R5F100LLDFA#V0
			G	R5F100LCDFA#X0, R5F100LDDFA#X0, R5F100LEDFA#X0, R5F100LFDFA#X0, R5F100LGDFA#X0, R5F100LHDFA#X0, R5F100LJDFA#X0, R5F100LKDFA#X0, R5F100LLDFA#X0
				R5F100LCGFA#V0, R5F100LDGFA#V0, R5F100LEGFA#V0, R5F100LFGFA#V0
				R5F100LCGFA#X0, R5F100LDGFA#X0, R5F100LEGFA#X0, R5F100LFGFA#X0
				R5F100LGGFA#V0, R5F100LHGFA#V0, R5F100LJGFA#V0
				R5F100LGGFA#X0, R5F100LHGFA#X0, R5F100LJGFA#X0
		Not mounted	A	R5F101LCAFA#V0, R5F101LDAFA#V0, R5F101LEAFA#V0, R5F101LFAFA#V0, R5F101LGAFA#V0, R5F101LHAFA#V0, R5F101LJAFA#V0, R5F101LKAFA#V0, R5F101LLAFA#V0
				R5F101LCAFA#X0, R5F101LDAFA#X0, R5F101LEAFA#X0, R5F101LFAFA#X0,
			D	R5F101LGAFA#X0, R5F101LHAFA#X0, R5F101LJAFA#X0, R5F101LKAFA#X0, R5F101LLAFA#X0
				R5F101LCDFA#V0, R5F101LDDFA#V0, R5F101LEDFA#V0, R5F101LFDFA#V0, R5F101LGDFA#V0, R5F101LHDFA#V0, R5F101LJDFA#V0, R5F101LKDFA#V0, R5F101LLDFA#V0
				R5F101LCDFA#X0, R5F101LDDFA#X0, R5F101LEDFA#X0, R5F101LFDFA#X0, R5F101LGDFA#X0, R5F101LHDFA#X0, R5F101LJDFA#X0, R5F101LKDFA#X0, R5F101LLDFA#X0

Note   For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

Table 1-1. List of Ordering Part Numbers

(10/12)

Pin count	Package	Data flash	Fields of Application Note	Ordering Part Number
80 pins	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	Mounted	A	R5F100MFAFA#V0, R5F100MGAFA#V0, R5F100MHAFA#V0, R5F100MJAFA#V0, R5F100MKAFA#V0, R5F100MLAFA#V0 R5F100MFAFA#X0, R5F100MGAFA#X0, R5F100MHAFA#X0, R5F100MJAFA#X0, R5F100MKAFA#X0, R5F100MLAFA#X0
			D	R5F100MFDFA#V0, R5F100MGDFA#V0, R5F100MHDFA#V0, R5F100MJDFA#V0, R5F100MKDFA#V0, R5F100MLDFA#V0 R5F100MFDFA#X0, R5F100MGDFA#X0, R5F100MHDFA#X0, R5F100MJDFA#X0, R5F100MKDFA#X0, R5F100MLDFA#X0
			G	R5F100MFGFA#V0, R5F100MGGFA#V0, R5F100MHGFA#V0, R5F100MJGFA#V0 R5F100MFGFA#X0, R5F100MGGFA#X0, R5F100MHGFA#X0, R5F100MJGFA#X0
		Not mounted	A	R5F101MFAFA#V0, R5F101MGAFA#V0, R5F101MHAFA#V0, R5F101MJAFA#V0, R5F101MKAFA#V0, R5F101MLAFA#V0 R5F101MFAFA#X0, R5F101MGAFA#X0, R5F101MHAFA#X0, R5F101MJAFA#X0, R5F101MKAFA#X0, R5F101MLAFA#X0
			D	R5F101MFDFA#V0, R5F101MGDFA#V0, R5F101MHDFA#V0, R5F101MJDFA#V0, R5F101MKDFA#V0, R5F101MLDFA#V0 R5F101MFDFA#X0, R5F101MGDFA#X0, R5F101MHDFA#X0, R5F101MJDFA#X0, R5F101MKDFA#X0, R5F101MLDFA#X0
	80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)	Mounted	A	R5F100MFAFB#V0, R5F100MGAFB#V0, R5F100MHAFB#V0, R5F100MJAFB#V0, R5F100MKAFB#V0, R5F100MLAFB#V0 R5F100MFAFB#X0, R5F100MGAFB#X0, R5F100MHAFB#X0, R5F100MJAFB#X0, R5F100MKAFB#X0, R5F100MLAFB#X0
			D	R5F100MFDFB#V0, R5F100MGDFB#V0, R5F100MHDFB#V0, R5F100MJDFB#V0, R5F100MKDFB#V0, R5F100MLDFB#V0 R5F100MFDFB#X0, R5F100MGDFB#X0, R5F100MHDFB#X0, R5F100MJDFB#X0, R5F100MKDFB#X0, R5F100MLDFB#X0
			G	R5F100MFGFB#V0, R5F100MGGFB#V0, R5F100MHGFB#V0, R5F100MJGFB#V0 R5F100MFGFB#X0, R5F100MGGFB#X0, R5F100MHGFB#X0, R5F100MJGFB#X0
		Not mounted	A	R5F101MFAFB#V0, R5F101MGAFB#V0, R5F101MHAFB#V0, R5F101MJAFB#V0, R5F101MKAFB#V0, R5F101MLAFB#V0 R5F101MFAFB#X0, R5F101MGAFB#X0, R5F101MHAFB#X0, R5F101MJAFB#X0, R5F101MKAFB#X0, R5F101MLAFB#X0
			D	R5F101MFDFB#V0, R5F101MGDFB#V0, R5F101MHDFB#V0, R5F101MJDFB#V0, R5F101MKDFB#V0, R5F101MLDFB#V0 R5F101MFDFB#X0, R5F101MGDFB#X0, R5F101MHDFB#X0, R5F101MJDFB#X0, R5F101MKDFB#X0, R5F101MLDFB#X0

Note　　For the fields of application, refer to **Figure 1-1 Part Number, Memory Size, and Package of RL78/G13**.

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3.3 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.50 mm pitch)

<R>

Top View   Bottom View

INDEX MARK   INDEX MARK
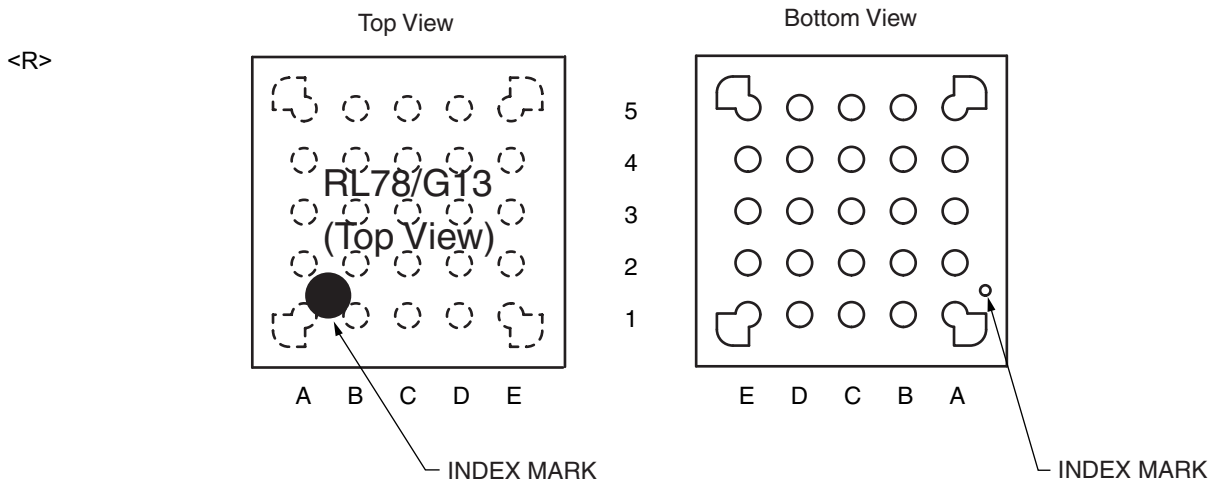
	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AV$_{REFM}$	P10/SCK00/ SCL00	4
3	P121/X1	V$_{DD}$	P20/ANI0/ AV$_{REFP}$	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V$_{SS}$	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark For pin identification, see **1.4 Pin Identification**.

1.3.8 44-pin products

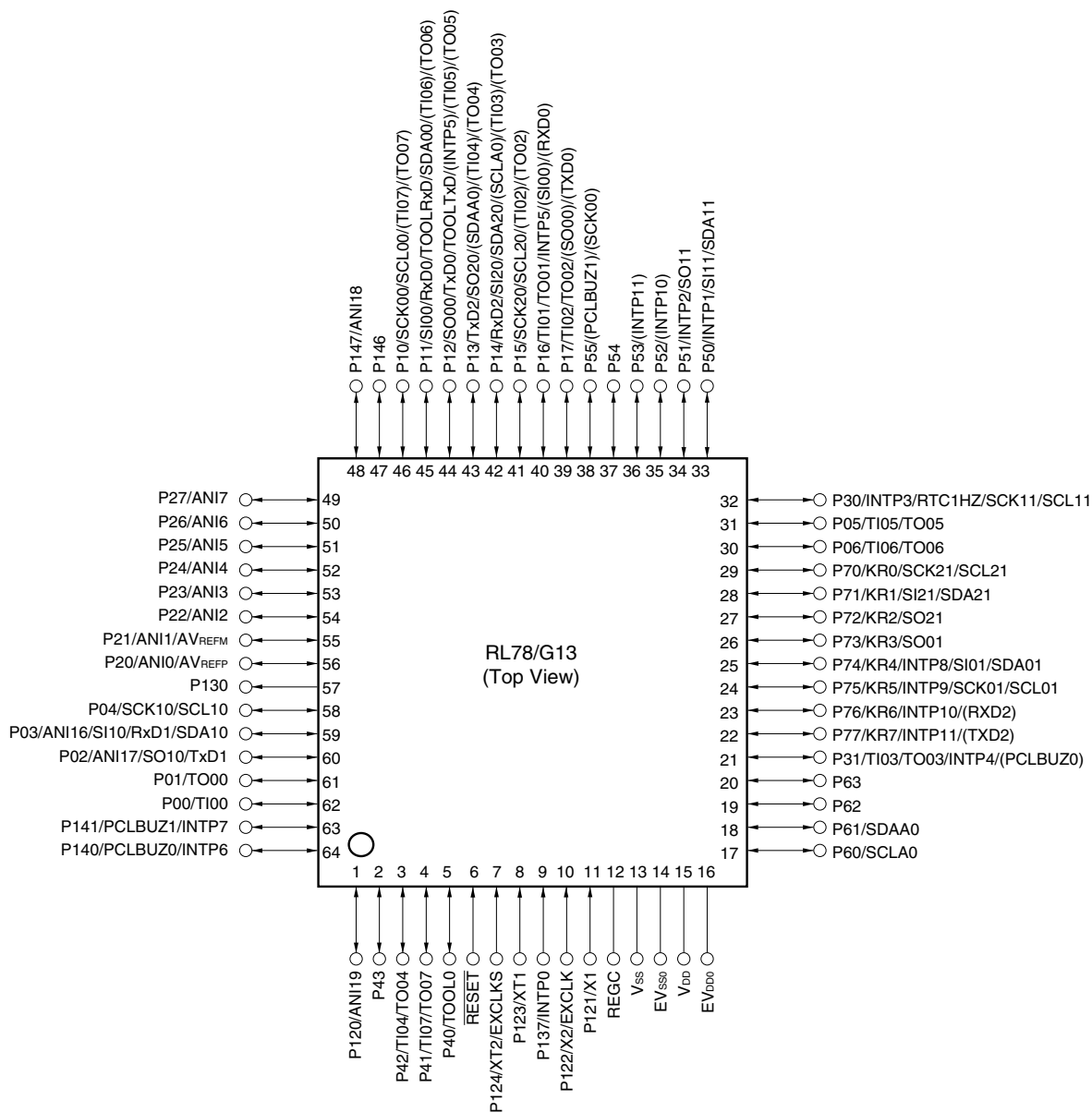- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)
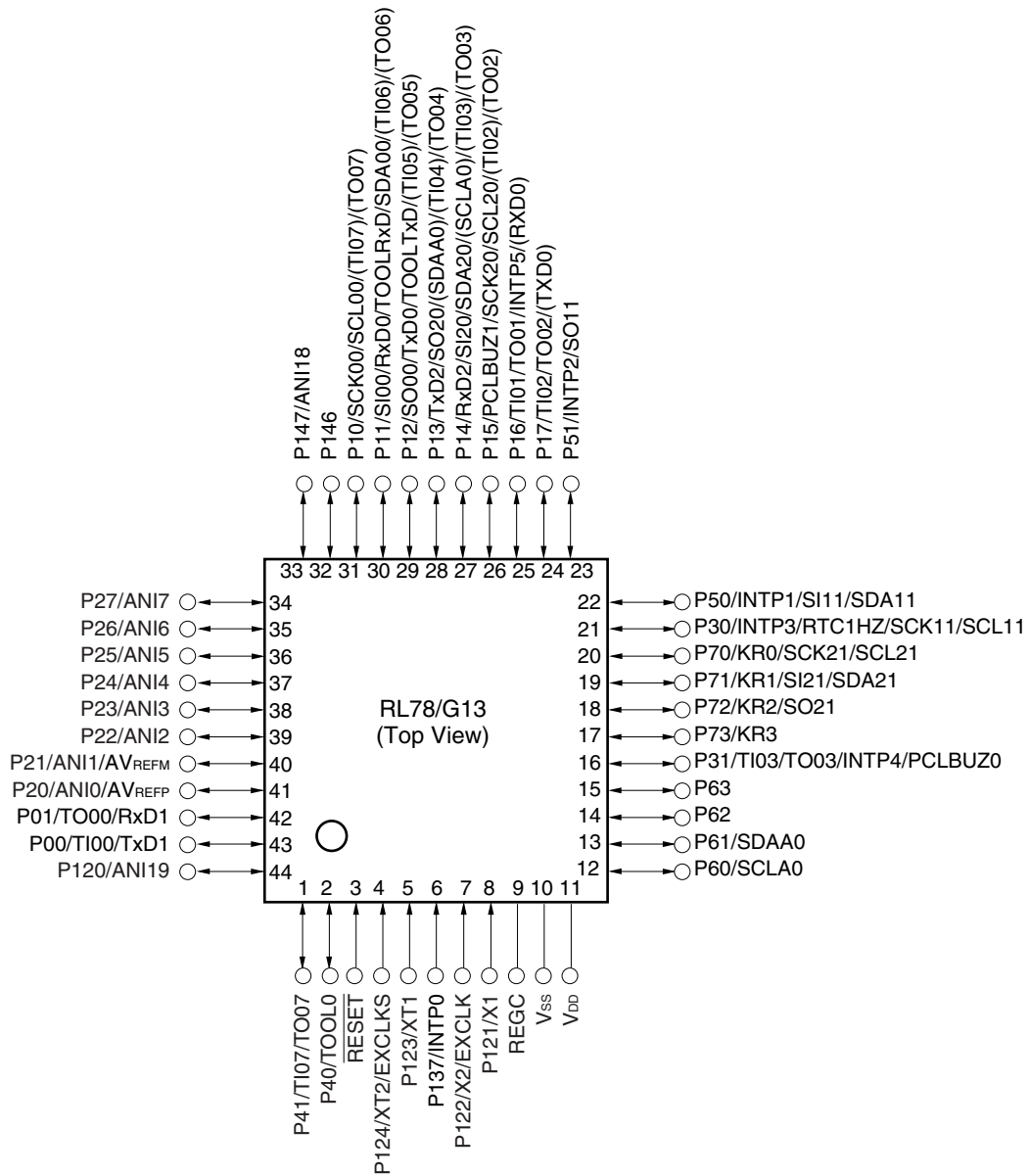
Caution   Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.
  2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

1.3.11 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)

Top pins (48–33):
- 48 P147/ANI18
- 47 P146
- 46 P10/SCK00/SCL00/(TI07)/(TO07)
- 45 P11/SI00/RxD0/TOOLRxD/SDA00/(TI06)/(TO06)
- 44 P12/SO00/TxD0/TOOLTxD/(INTP5)/(TI05)/(TO05)
- 43 P13/TxD2/SO20/(SDAA0)/(TI04)/(TO04)
- 42 P14/RxD2/SI20/SDA20/(SCLA0)/(TI03)/(TO03)
- 41 P15/SCK20/SCL20/(TI02)/(TO02)
- 40 P16/TI01/TO01/INTP5/(SI00)/(RXD0)
- 39 P17/TI02/TO02/(SO00)/(TXD0)
- 38 P55/(PCLBUZ1)/(SCK00)
- 37 P54
- 36 P53/(INTP11)
- 35 P52/(INTP10)
- 34 P51/INTP2/SO11
- 33 P50/INTP1/SI11/SDA11

Left pins (49–64):
- 49 P27/ANI7
- 50 P26/ANI6
- 51 P25/ANI5
- 52 P24/ANI4
- 53 P23/ANI3
- 54 P22/ANI2
- 55 P21/ANI1/AV_{REFM}
- 56 P20/ANI0/AV_{REFP}
- 57 P130
- 58 P04/SCK10/SCL10
- 59 P03/ANI16/SI10/RxD1/SDA10
- 60 P02/ANI17/SO10/TxD1
- 61 P01/TO00
- 62 P00/TI00
- 63 P141/PCLBUZ1/INTP7
- 64 P140/PCLBUZ0/INTP6

RL78/G13 (Top View)

Right pins (32–17):
- 32 P30/INTP3/RTC1HZ/SCK11/SCL11
- 31 P05/TI05/TO05
- 30 P06/TI06/TO06
- 29 P70/KR0/SCK21/SCL21
- 28 P71/KR1/SI21/SDA21
- 27 P72/KR2/SO21
- 26 P73/KR3/SO01
- 25 P74/KR4/INTP8/SI01/SDA01
- 24 P75/KR5/INTP9/SCK01/SCL01
- 23 P76/KR6/INTP10/(RXD2)
- 22 P77/KR7/INTP11/(TXD2)
- 21 P31/TI03/TO03/INTP4/(PCLBUZ0)
- 20 P63
- 19 P62
- 18 P61/SDAA0
- 17 P60/SCLA0

Bottom pins (1–16):
- 1 P120/ANI19
- 2 P43
- 3 P42/TI04/TO04
- 4 P41/TI07/TO07
- 5 P40/TOOL0
- 6 RESET
- 7 P124/XT2/EXCLKS
- 8 P123/XT1
- 9 P137/INTP0
- 10 P122/X2/EXCLK
- 11 P121/X1
- 12 REGC
- 13 V_{SS}
- 14 EV_{SS0}
- 15 V_{DD}
- 16 EV_{DD0}

Cautions 1. Make EV$_{SS0}$ pin the same potential as V$_{SS}$ pin.

2. Make V$_{DD}$ pin the potential that is higher than EV$_{DD0}$ pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V$_{DD}$ and EV$_{DD0}$ pins and connect the V$_{SS}$ and EV$_{SS0}$ pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4-8 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G13 User's Manual.

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (3/5)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV$_{DD0}$		EV$_{DD0}$	V
	V$_{IH2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	2.2		EV$_{DD0}$	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	2.0		EV$_{DD0}$	V
			TTL input buffer 1.6 V ≤ EV$_{DD0}$ < 3.3 V	1.5		EV$_{DD0}$	V
	V$_{IH3}$	P20 to P27, P150 to P156		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH4}$	P60 to P63		0.7EV$_{DD0}$		6.0	V
	V$_{IH5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
Input voltage, low	V$_{IL1}$	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV$_{DD0}$	V
	V$_{IL2}$	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV$_{DD0}$ < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV$_{DD0}$ < 3.3 V	0		0.32	V
	V$_{IL3}$	P20 to P27, P150 to P156		0		0.3V$_{DD}$	V
	V$_{IL4}$	P60 to P63		0		0.3EV$_{DD0}$	V
	V$_{IL5}$	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V

Caution The maximum value of V$_{IH}$ of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV$_{DD0}$, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4 AC Characteristics

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T$_{CY}$	Main system clock (f$_{MAIN}$) operation	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	µs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	µs
			LV (low-voltage main) mode	1.6 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	µs
		Subsystem clock (f$_{SUB}$) operation		1.8 V ≤ V$_{DD}$ ≤ 5.5 V	28.5	30.5	31.3	µs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V$_{DD}$ ≤ 5.5 V	0.03125		1	µs
				2.4 V ≤ V$_{DD}$ < 2.7 V	0.0625		1	µs
			LS (low-speed main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.125		1	µs
			LV (low-voltage main) mode	1.8 V ≤ V$_{DD}$ ≤ 5.5 V	0.25		1	µs
External system clock frequency	f$_{EX}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			1.0		20.0	MHz
		2.4 V ≤ V$_{DD}$ < 2.7 V			1.0		16.0	MHz
		1.8 V ≤ V$_{DD}$ < 2.4 V			1.0		8.0	MHz
		1.6 V ≤ V$_{DD}$ < 1.8 V			1.0		4.0	MHz
	f$_{EXS}$				32		35	kHz
External system clock input high-level width, low-level width	t$_{EXH}$, t$_{EXL}$	2.7 V ≤ V$_{DD}$ ≤ 5.5 V			24			ns
		2.4 V ≤ V$_{DD}$ < 2.7 V			30			ns
		1.8 V ≤ V$_{DD}$ < 2.4 V			60			ns
		1.6 V ≤ V$_{DD}$ < 1.8 V			120			ns
	t$_{EXHS}$, t$_{EXLS}$				13.7			µs
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	t$_{TIH}$, t$_{TIL}$				1/f$_{MCK}$+10			ns[Note]
TO00 to TO07, TO10 to TO17 output frequency	f$_{TO}$	HS (high-speed main) mode		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
				2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f$_{PCL}$	HS (high-speed main) mode		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V			16	MHz
				2.7 V ≤ EV$_{DD0}$ < 4.0 V			8	MHz
				1.8 V ≤ EV$_{DD0}$ < 2.7 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LS (low-speed main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
		LV (low-voltage main) mode		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V			4	MHz
				1.6 V ≤ EV$_{DD0}$ < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t$_{INTH}$, t$_{INTL}$	INTP0		1.6 V ≤ V$_{DD}$ ≤ 5.5 V	1			µs
		INTP1 to INTP11		1.6 V ≤ EV$_{DD0}$ ≤ 5.5 V	1			µs
Key interrupt input low-level width	t$_{KR}$	KR0 to KR7		1.8 V ≤ EV$_{DD0}$ ≤ 5.5 V	250			ns
				1.6 V ≤ EV$_{DD0}$ < 1.8 V	1			µs
RESET low-level width	t$_{RSL}$				10			µs

(**Note** and **Remark** are listed on the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output) (3/3)

(T$_A$ = −40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SIp setup time (to SCKp↓) [Note 1]	t$_{SIK1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	110		110		110		ns
SIp hold time (from SCKp↓) [Note 1]	t$_{KSI1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output [Note 1]	t$_{KSO1}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 30 pF, R$_b$ = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 30 pF, R$_b$ = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2], C$_b$ = 30 pF, R$_b$ = 5.5 kΩ		25		25		25	ns

Notes 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. Use it with EV$_{DD0}$ ≥ V$_b$.

Caution **Select the TTL input buffer for the SIp pin and the N-ch open drain output (V$_{DD}$ tolerance (When 20- to 52-pin products)/EV$_{DD}$ tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V$_{IH}$ and V$_{IL}$, see the DC characteristics with TTL input buffer selected.**

(Remarks are listed on the next page.)

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)
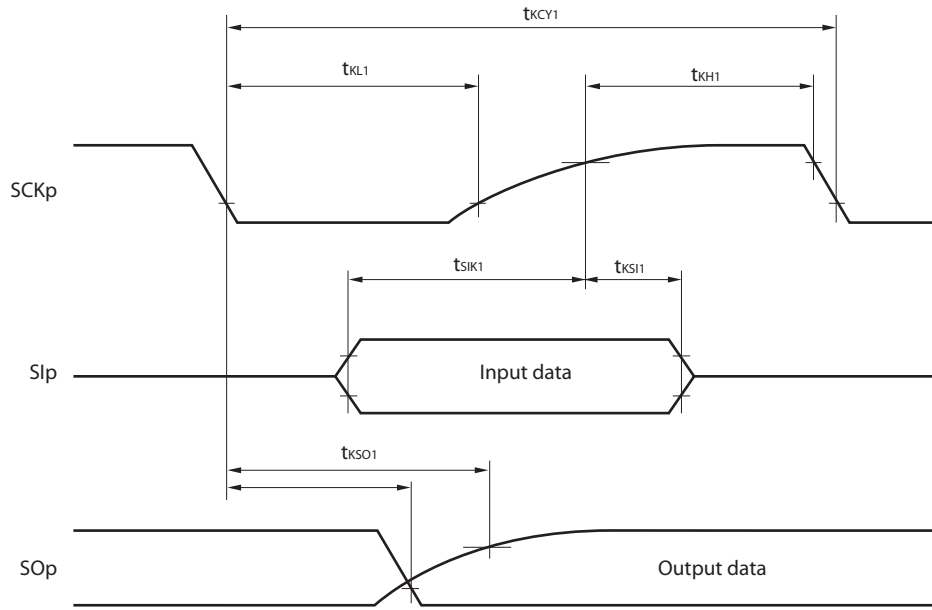
CSI mode serial transfer timing (master mode) (during communication at different potential)
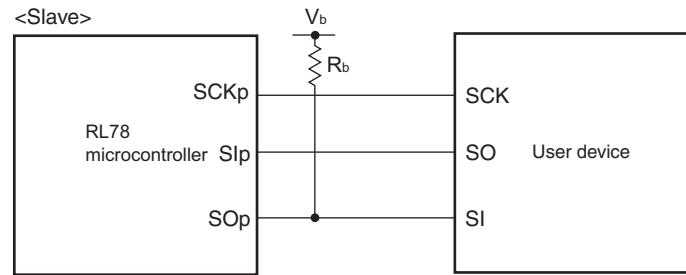**(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**
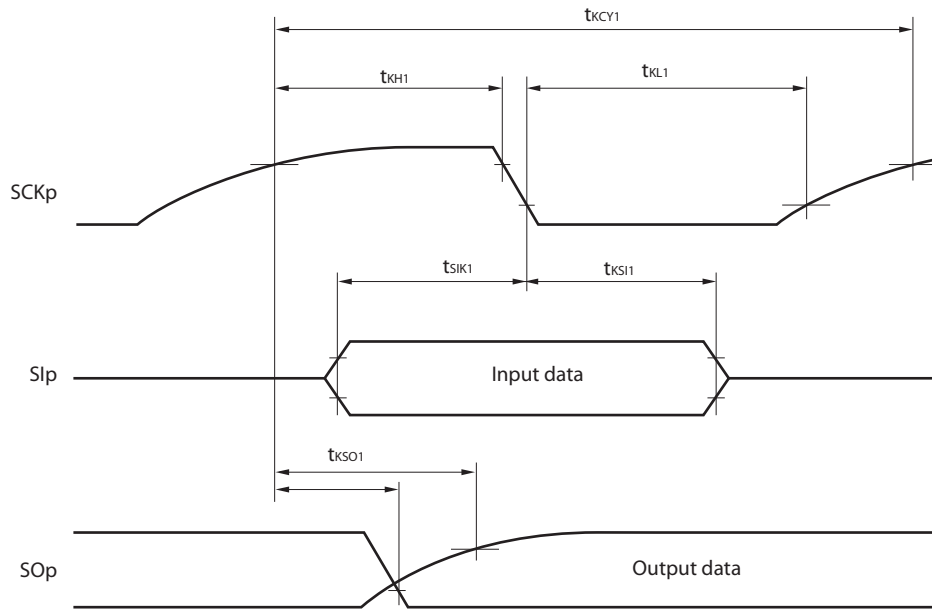
Remarks 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T$_A$ = –40 to +85°C, 1.8 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V) (1/2)

Parameter	Symbol	Conditions		HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time [Note 1]	t$_{KCY2}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V	24 MHz < f$_{MCK}$	14/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	12/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 20 MHz	10/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V	24 MHz < f$_{MCK}$	20/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	16/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	14/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	12/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	8/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	6/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns
		1.8 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V [Note 2]	24 MHz < f$_{MCK}$	48/f$_{MCK}$		—		—		ns
			20 MHz < f$_{MCK}$ ≤ 24 MHz	36/f$_{MCK}$		—		—		ns
			16 MHz < f$_{MCK}$ ≤ 20 MHz	32/f$_{MCK}$		—		—		ns
			8 MHz < f$_{MCK}$ ≤ 16 MHz	26/f$_{MCK}$		—		—		ns
			4 MHz < f$_{MCK}$ ≤ 8 MHz	16/f$_{MCK}$		16/f$_{MCK}$		—		ns
			f$_{MCK}$ ≤ 4 MHz	10/f$_{MCK}$		10/f$_{MCK}$		10/f$_{MCK}$		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

CSI mode connection diagram (during communication at different potential)

Remarks **1.** R$_b$[Ω]:Communication line (SOp) pull-up resistance, C$_b$[F]: Communication line (SOp) load
        capacitance, V$_b$[V]: Communication line voltage
     2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10,
        12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
     3. f$_{MCK}$: Serial array unit operation clock frequency
        (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
        m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
     4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
        Use other CSI for communication at different potential.

(3) When reference voltage (+) = V$_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), reference voltage (–) = V$_{SS}$ (ADREFM = 0), target pin : ANI0 to ANI14, ANI16 to ANI26, internal reference voltage, and temperature sensor output voltage

(T$_A$ = –40 to +85°C, 1.6 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V, Reference voltage (+) = V$_{DD}$, Reference voltage (–) = V$_{SS}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]		1.2	±10.5	LSB
Conversion time	t$_{CONV}$	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI26	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V	57		95	μs
Conversion time	t$_{CONV}$	10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V$_{DD}$ ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V$_{DD}$ ≤ 5.5 V	3.5625		39	μs
			2.4 V ≤ V$_{DD}$ ≤ 5.5 V	17		39	μs
Zero-scale error[Notes 1, 2]	E$_{ZS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Full-scale error[Notes 1, 2]	E$_{FS}$	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±0.85	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±6.5	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	1.8 V ≤ V$_{DD}$ ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V$_{DD}$ ≤ 5.5 V [Note 3]			±2.5	LSB
Analog input voltage	V$_{AIN}$	ANI0 to ANI14		0		V$_{DD}$	V
		ANI16 to ANI26		0		EV$_{DD0}$	V
		Internal reference voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{BGR}$ [Note 4]			V
		Temperature sensor output voltage (2.4 V ≤ V$_{DD}$ ≤ 5.5 V, HS (high-speed main) mode)		V$_{TMPS25}$ [Note 4]			V

Notes 1. Excludes quantization error (±1/2 LSB).

　　　2. This value is indicated as a ratio (%FSR) to the full-scale value.

　　　3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

　　　4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

LVD Detection Voltage of Interrupt & Reset Mode

(T$_A$ = –40 to +85°C, V$_{PDR}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V$_{LVDA0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 0, falling reset voltage		1.60	1.63	1.66	V
	V$_{LVDA1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V$_{LVDA2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V$_{LVDA3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V$_{LVDB0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 0, 1, falling reset voltage		1.80	1.84	1.87	V
	V$_{LVDB1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V$_{LVDB2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V$_{LVDB3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V$_{LVDC0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 0, falling reset voltage		2.40	2.45	2.50	V
	V$_{LVDC1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V$_{LVDC2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V$_{LVDC3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V
			Falling interrupt voltage	3.60	3.67	3.74	V
	V$_{LVDD0}$	V$_{POC2}$, V$_{POC1}$, V$_{POC0}$ = 0, 1, 1, falling reset voltage		2.70	2.75	2.81	V
	V$_{LVDD1}$	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V$_{LVDD2}$	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V
			Falling interrupt voltage	2.90	2.96	3.02	V
	V$_{LVDD3}$	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V
			Falling interrupt voltage	3.90	3.98	4.06	V

Absolute Maximum Ratings (T$_A$ = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I$_{OH1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	−40	mA
		Total of all pins −170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	−70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	−100	mA
	I$_{OH2}$	Per pin	P20 to P27, P150 to P156	−0.5	mA
		Total of all pins		−2	mA
Output current, low	I$_{OL1}$	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I$_{OL2}$	Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature	T$_A$	In normal operation mode		−40 to +105	°C
		In flash memory programming mode			
Storage temperature	T$_{stg}$			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.
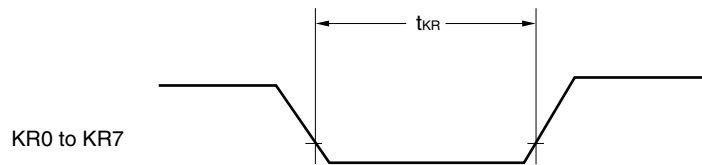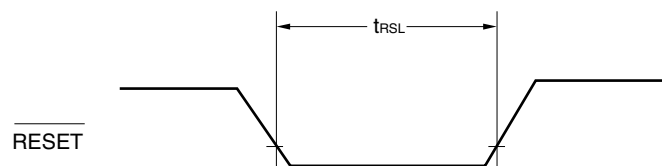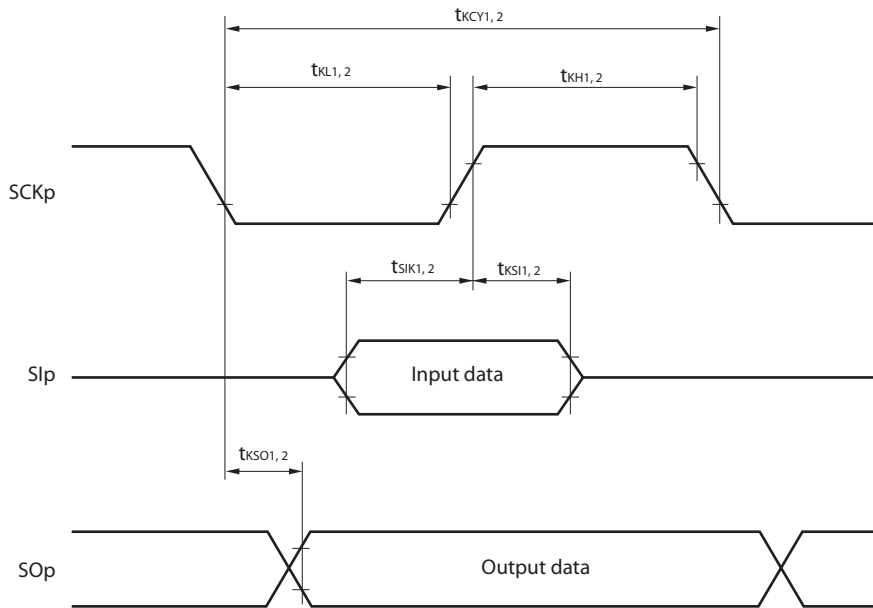
TI/TO Timing

TI00 to TI07, TI10 to TI17

t_{TIL} t_{TIH}

TO00 to TO07, TO10 to TO17

$1/f_{TO}$
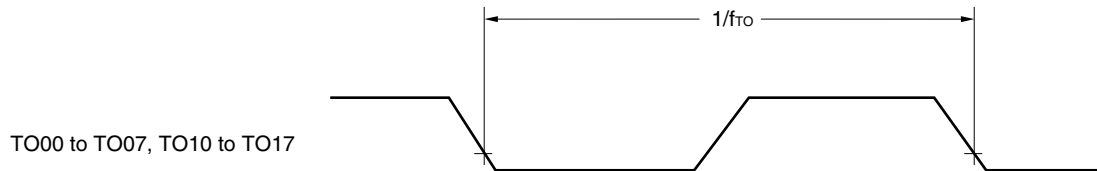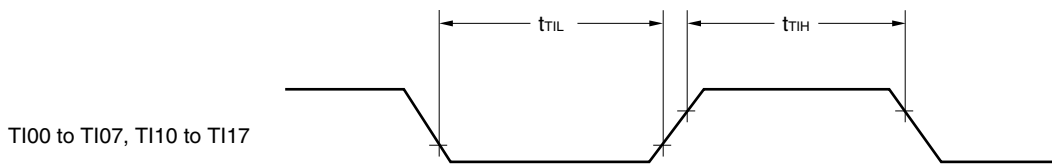
Interrupt Request Input Timing

INTP0 to INTP11

t_{INTL} t_{INTH}
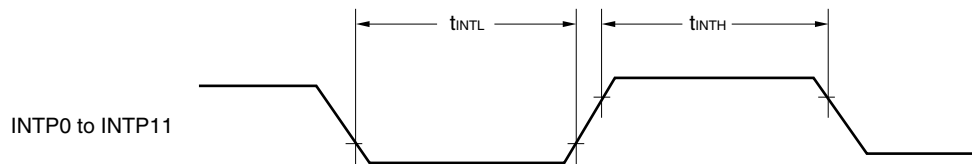
Key Interrupt Input Timing

KR0 to KR7

t_{KR}
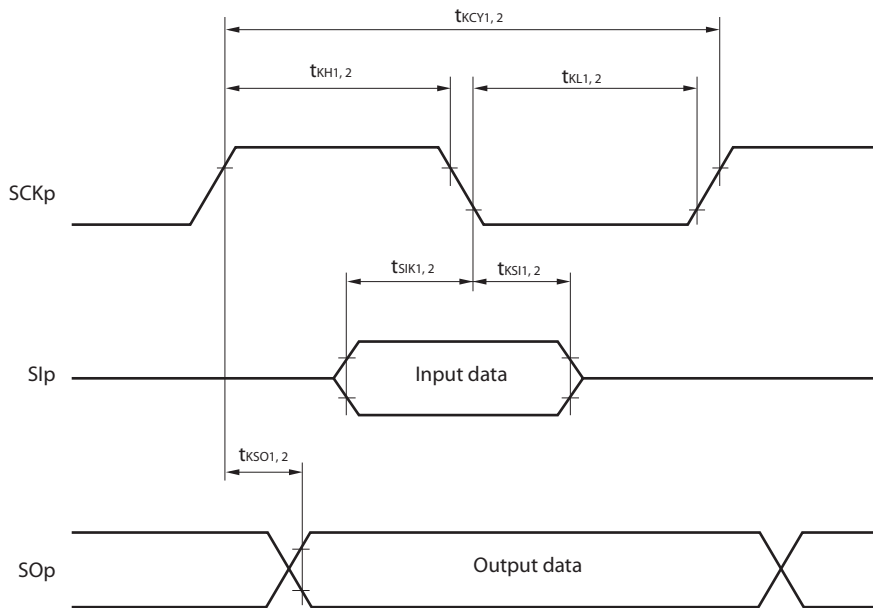
$\overline{RESET}$ Input Timing

$\overline{RESET}$

t_{RSL}

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)

Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
　　　　2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I^{2}C mode) (1/2)

(T$_A$ = –40 to +105°C, 2.4 V ≤ EV$_{DD0}$ = EV$_{DD1}$ ≤ V$_{DD}$ ≤ 5.5 V, V$_{SS}$ = EV$_{SS0}$ = EV$_{SS1}$ = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f$_{SCL}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ		400 [Note 1]	kHz
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ		100 [Note 1]	kHz
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ		100 [Note 1]	kHz
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ		100 [Note 1]	kHz
Hold time when SCLr = "L"	t$_{LOW}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	1200		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	4600		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	4600		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t$_{HIGH}$	4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	620		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 50 pF, R$_b$ = 2.7 kΩ	500		ns
		4.0 V ≤ EV$_{DD0}$ ≤ 5.5 V, 2.7 V ≤ V$_b$ ≤ 4.0 V, C$_b$ = 100 pF, R$_b$ = 2.8 kΩ	2700		ns
		2.7 V ≤ EV$_{DD0}$ < 4.0 V, 2.3 V ≤ V$_b$ ≤ 2.7 V, C$_b$ = 100 pF, R$_b$ = 2.7 kΩ	2400		ns
		2.4 V ≤ EV$_{DD0}$ < 3.3 V, 1.6 V ≤ V$_b$ ≤ 2.0 V, C$_b$ = 100 pF, R$_b$ = 5.5 kΩ	1830		ns

(**Notes** and **Caution** are listed on the next page, and **Remarks** are listed on the page after the next page.)

4.6 36-pin Products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
R5F100CAGLA, R5F100CCGLA, R5F100CDGLA, R5F100CEGLA, R5F100CFGLA, R5F100CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

DETAIL C

φb
(LAND PAD)

φ0.34±0.05
(APERTURE OF
SOLDER RESIST)

DETAIL D

0.70±0.05
0.55±0.05
0.75
0.55
R0.17±0.05
R0.12±0.05

0.55
0.75
0.55±0.05
0.70±0.05

DETAIL E

R0.17±0.05
R0.12±0.05
0.70±0.05
0.55±0.05
0.75
0.55

0.55
0.75
0.55±0.05
0.70±0.05
R0.275±0.05
R0.35±0.05
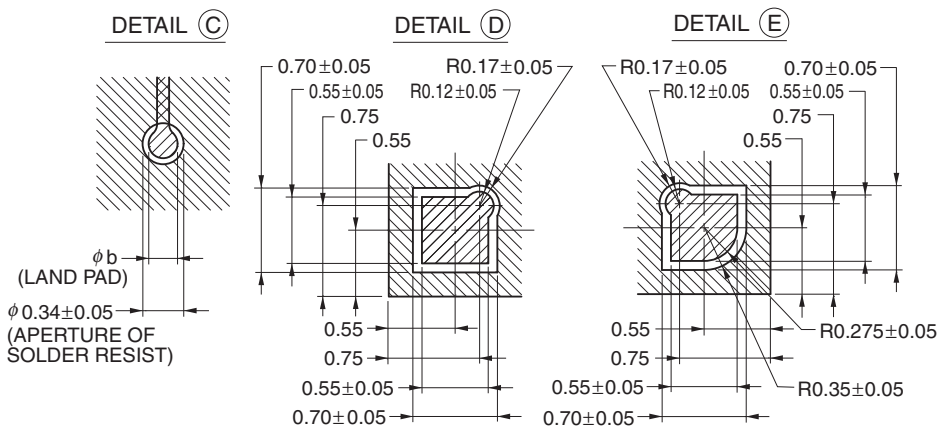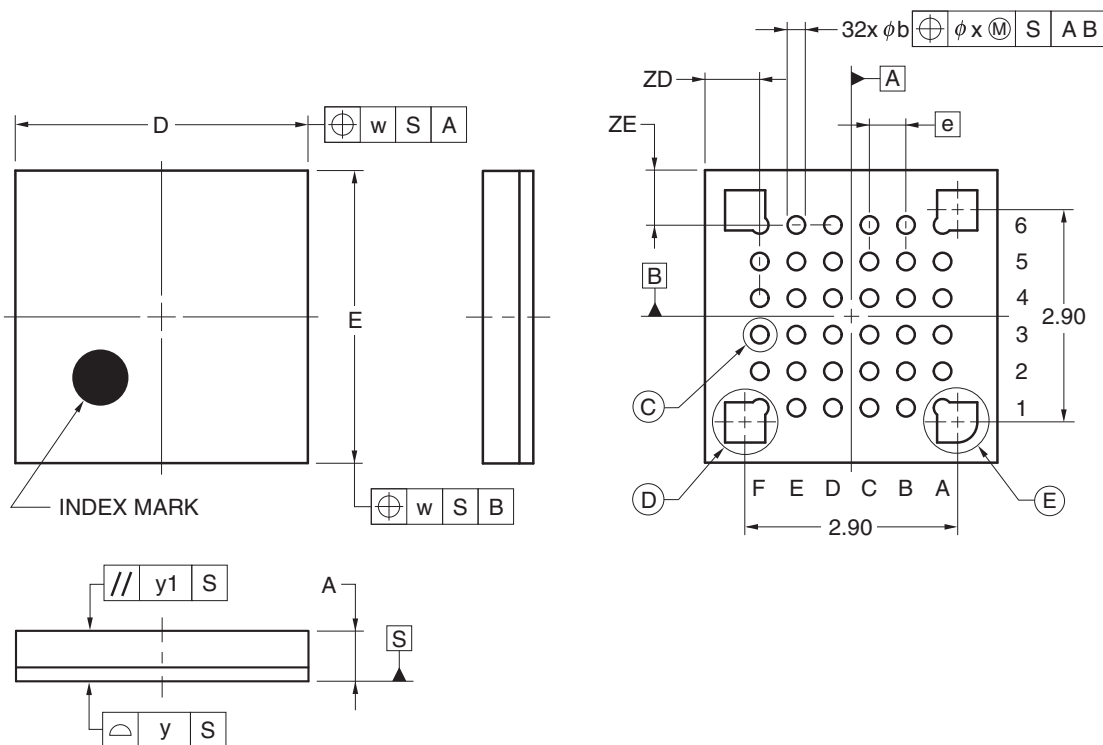
ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.75
ZE	0.75

(UNIT:mm)

4.10 52-pin Products

R5F100JCAFA, R5F100JDAFA, R5F100JEAFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJAFA, R5F100JKAFA, R5F100JLAFA

R5F101JCAFA, R5F101JDAFA, R5F101JEAFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJAFA, R5F101JKAFA, R5F101JLAFA

R5F100JCDFA, R5F100JDDFA, R5F100JEDFA, R5F100JFDFA, R5F100JGDFA, R5F100JHDFA, R5F100JJDFA, R5F100JKDFA, R5F100JLDFA

R5F101JCDFA, R5F101JDDFA, R5F101JEDFA, R5F101JFDFA, R5F101JGDFA, R5F101JHDFA, R5F101JJDFA, R5F101JKDFA, R5F101JLDFA

R5F100JCGFA, R5F100JDGFA, R5F100JEGFA, R5F100JFGFA, R5F100JGGFA, R5F100JHGFA, R5F100JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3

detail of lead end
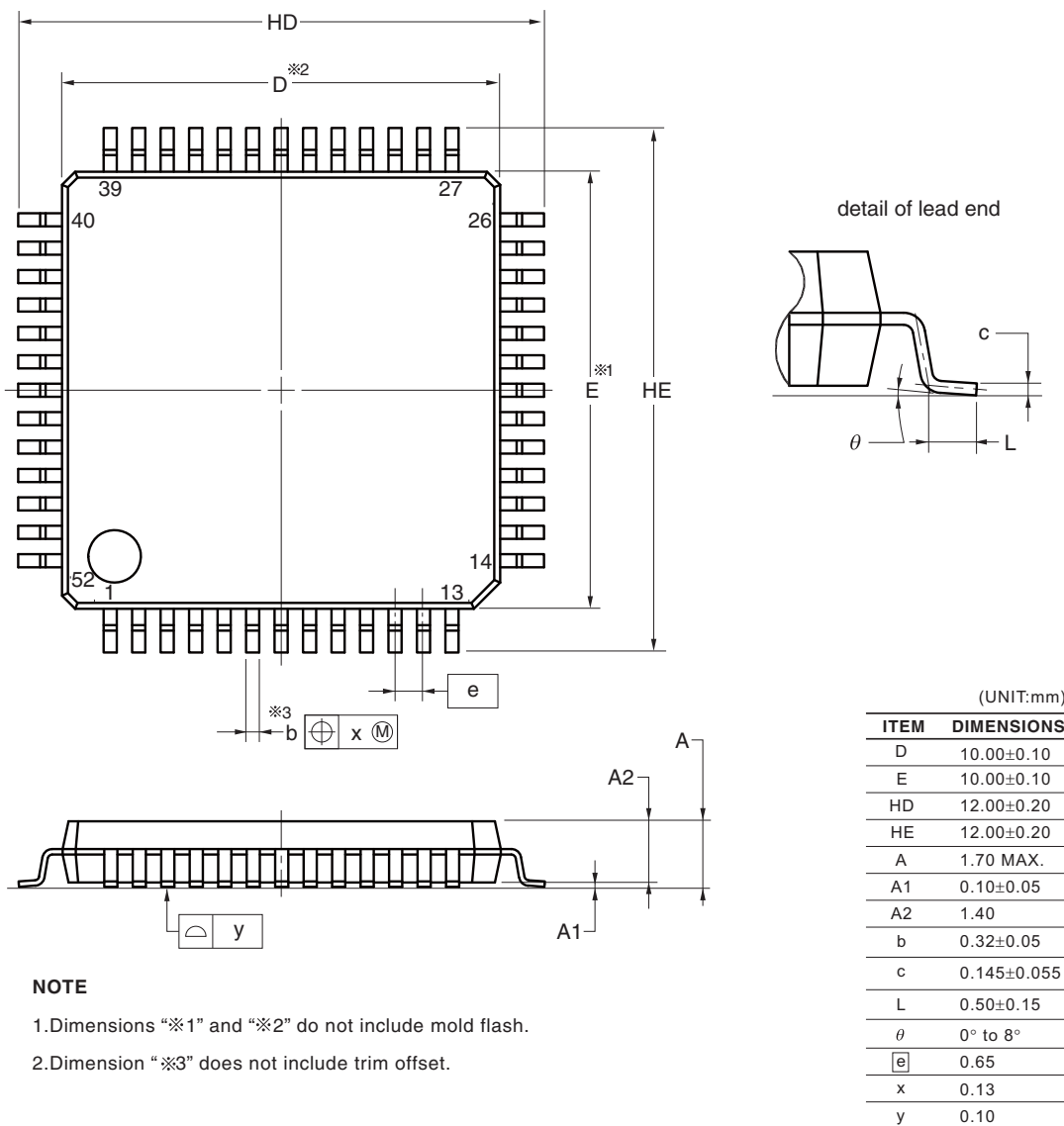
NOTE

1. Dimensions "※1" and "※2" do not include mold flash.

2. Dimension "※3" does not include trim offset.

	(UNIT:mm)
ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB
R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB
R5F100MFDFB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
R5F101MFDFB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB
R5F100MFGFB, R5F100MGGFB, R5F100MHGFB, R5F100MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	12.00±0.20
E	12.00±0.20
HD	14.00±0.20
HE	14.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145 ^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3° ^{+5°}_{-3°}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25
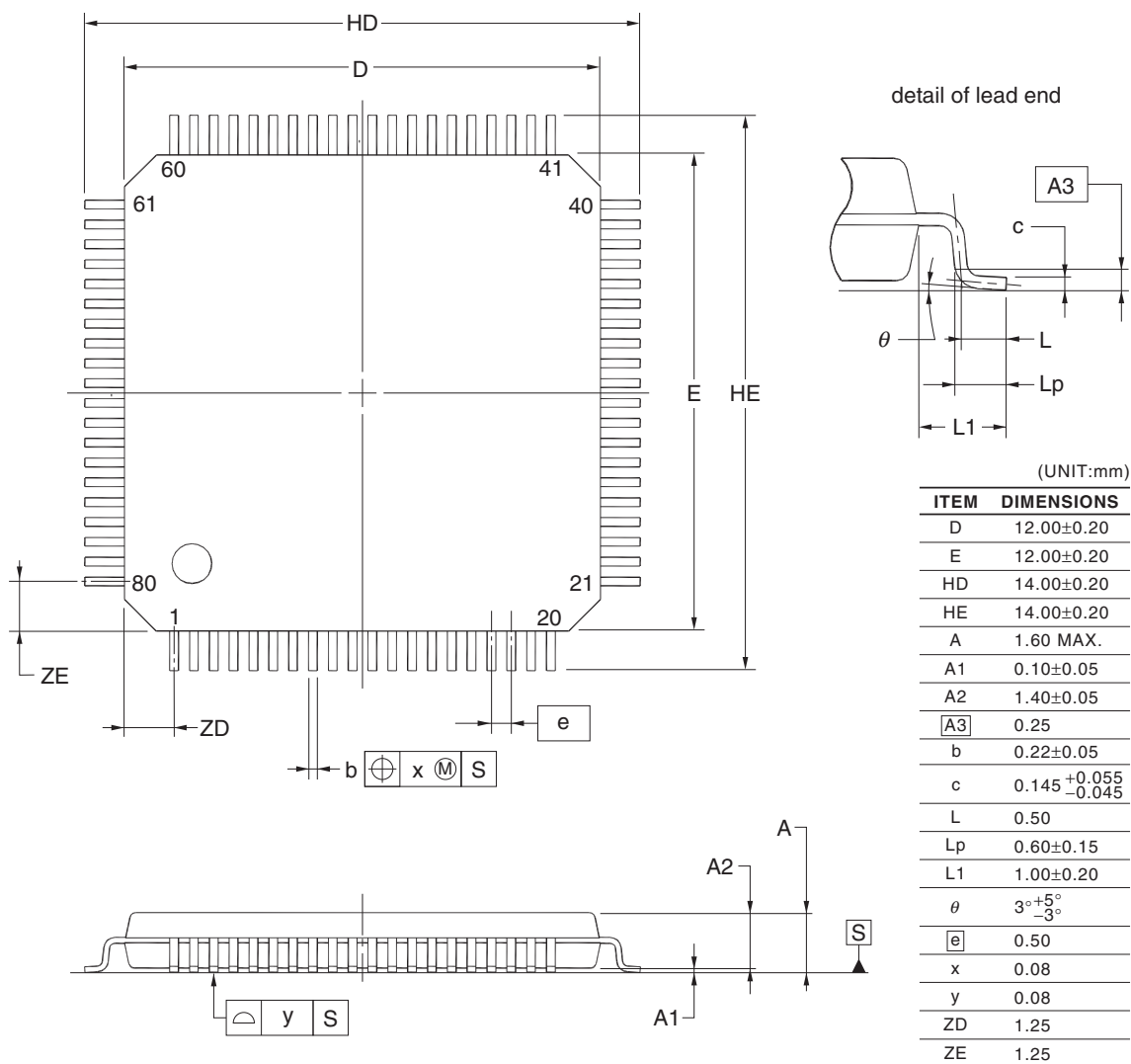
NOTE
Each lead centerline is located within 0.08 mm of
its true position at maximum material condition.